

Low Power VLSI Design of a modified Brent Kung adder based Multiply Accumulate Unit for Reverb Engines

Rakesh S, K. S. Vijula Grace

Abstract: Nowadays low power audio signal processing systems are in high demand due to its wide application in the musical industry. VLSI engineers always face many challenges in designing power efficient audio processor systems. Digital Reverb Processor is a system used to provide quality reverberation effects during stage performances. The main component used to produce the reverberation effects is a Multiply Accumulate (MAC) unit. Here the research focuses on implementing MAC unit using a modified Brent Kung Adder (BKA) that employs a 4 transistor inequality detector in the pre-processing and post-processing stages. The unit is designed using Verilog Hardware Description Language in Xilinx Vivado Design Suite 2015.2. It is synthesized for Artix-7 series Field Programmable Gate Array (FPGA). The proposed architecture has shown significant improvement in the power consumption and the figure of merit. The 16-bit design showed an improvement of 10% in the power consumption and 8.34% in the figure of merit. The applications of low power Digital Reverb Processor include Musical Instrument Amplifiers, Digital Mixers and Digital effect boxes.

Index Terms: Brent Kung adder, Digital signal processor, Modified Inequality detector, Multiply accumulate unit, Vivado design suite.

I. INTRODUCTION

The technological advancement in the field of signal processing brought revolution in the field of music industry. Nowadays there are Digital Reverb Processors available to produce the necessary high quality reverb effects that may be added to songs or other musical performances. Reverberation naturally occurs as a result of the build up and decay of several sound signal reflections and their echoes. These reverberation effects can now be generated using the Reverb Units which employ audio signal processors. There is a high demand for such a Digital Reverb Processor design which has lower power consumption. The main unit in a Digital Reverb Processor is a Multiply Accumulate (MAC) unit. The MAC unit has a multiplier, an adder and an accumulator register as shown in Figure 1. A low power MAC unit may be employed

in a Digital Reverb Processor to reduce the overall power consumption of the processor unit. The MAC unit may be used to design digital filters for the reverb generation. The applications of Digital Reverb Processor include Musical Instrument Amplifiers, Digital Mixers and Digital effect boxes.

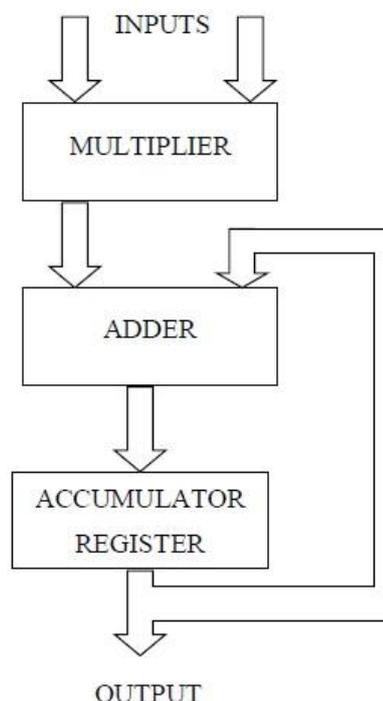


Fig. 1: General architecture of MAC unit

A design scheme is proposed here to reduce the power consumption of the MAC unit. The MAC unit is implemented using a modified Brent Kung Adder (BKA) in which the pre-processing stage and the post processing stage are modified. The Brent Kung Adder with Modified Pre-processing and Post processing stages (BKA_MPPS) is used in the multiplier stage and the adder stage of the MAC unit. The coding is done using Verilog HDL in the tool Xilinx Vivado Design Suite 2015.2. It is synthesized for Artix-7 series Field Programmable Gate Array (FPGA).

The rest of the paper is organized as follows. In Section II, the review work is explained in detail. Section III describes the design of the proposed scheme. The simulation results are discussed in Section IV and finally the concluding remarks are given in Section V.

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II. LITERATURE REVIEW

There has been extensive research going on in the area of low power digital signal processing during the past two decades. Mohamed Asan Basiri et al. introduced a different floating point MAC structure compared to the conventional one. He combined the multiplier and adder block and formed a new block called multiplier-accumulator block and used Wallace tree for multiply accumulation process [1]. Tung Thanh Hoang et al. proposed a two's complement MAC architecture which used a carry save adder as the final adder. The carry save adder contained 3:2 counters and it used shorter interconnects [2].

S Ahish et al. developed a MAC unit with a partial product reduction block and the multiplier was implemented using Brent Kung adder. The design achieved better area, delay and power performance compared to the conventional multiplier employing Booth algorithm [3]. Nithish Kumar V et al. incorporated a modified carry select adder at the multiplier stage of the MAC unit to improve the area. A digital filter is then designed using the MAC unit which achieved significant reduction in area and power [4]. Maroju Saikumar et al. introduced four different MAC architectures which employed carry save adder at the adder stage and four different multipliers. The four different multipliers used in the design were Array Multiplier, Ripple Carry Multiplier with row bypass technique, Wallace Tree Multiplier and Dadda Multiplier [5].

Narendra C.P et al. developed a partial product reduction stage using 29 compressors. Compressor architectures were also utilized in the carry propagation adder stage and accumulation stage [6]. A. Abdelgawad designed a merged architecture which combined the accumulation stage with the multiplier circuit. The speed and throughput of the MAC unit were increased and the area was decreased [7]. Suryasnata Tripathy et al. introduced a power efficient Vedic multiplier and realized using 45nm CMOS technology. He presented new design for 4-bit and 8-bit multipliers based on the URDHVA TIRYAKBHYAM (UT) sutra in Vedic Mathematics. The design was based on transmission gate logic and pass transistor logic. The design was realized using Cadence EDA tool with a 1V power supply by using several test inputs. The design showed improvement in speed, power consumed and chip area. The partial product generation unit designed using 5T AND gates helped to reduce the chip area. The UT sutra based design was responsible for the speed and power performance [8]. S.Rakesh et al. reviewed the design of different MAC unit architectures [9].

III. PROPOSED METHOD

In the proposed system a modified Brent Kung Adder (BKA) is used for adding the partial products in the vedic multiplier and also at the adder stage. The modification in this adder is done at the pre-processing and the post-processing stages. The pre-processing and post-processing stages consist of an inequality detector which performs exclusive OR operation. The inequality detector is designed here using four transistor logic. Switch level modeling is used to design the logic. The logic used is similar to the Gate Diffusion Input (GDI) logic [10].

Brent Kung Adder is a type of Parallel Prefix adder which has $(2\log_2 N - 1)$ number of stages where N is the number of bits [11]. It has high logic depth and hence has more

computational delay. It has lesser number of nodes and hence the area occupied is less [12].

Brent Kung adder consists of a Propagate bit and Generate bit block (BGP) in the pre-processing stage, Group Generate and Propagate block (GGP) and Group block in the carry computation stage and finally an inequality detector in the post processing stage for sum calculation.

BGP block generates the propagate bit

$$P_i = A_i \text{ xor } B_i \quad (1)$$

where P_i is i^{th} Propagate bit, A_i is i^{th} A input, B_i is i^{th} B input, xor is 'xor' operation in digital.

and generate bit

$$G_i = A_i \text{ and } B_i \quad (2)$$

where G_i is i^{th} Generate bit, A_i is i^{th} A input, B_i is i^{th} B input, and is 'and' operation in digital.

Figure 2 shows that GGP block generates

$$G = G_i + P_i \cdot G_{\text{previous}} \quad (3)$$

$$P = P_i \cdot P_{\text{previous}} \quad (4)$$

where G is Group Generate bit, P is Group Propagate bit, G_{previous} is Generate bit from previous stage, P_{previous} is Propagate bit from previous stage, + is 'or' operation in digital, . is 'and' operation in digital.

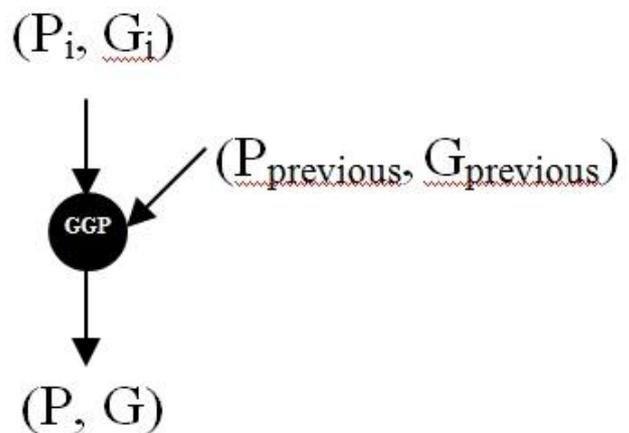


Fig. 2: Generation of Group Generate and Propagate bits

Figure 3 explains that GG block generates

$$G = G_i + P_i \cdot G_{\text{previous}} \quad (5)$$

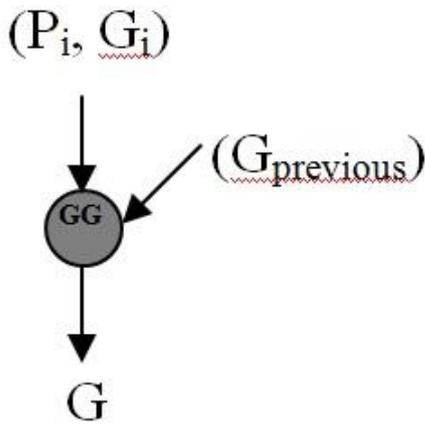


Fig. 3: Generation of Group Generate bit

Figure 4 clearly shows how the GGP block and GG blocks are used to compute the carry at different stages of BKA. The expressions for the generation of carry C_0 to C_7 are also given in (6) to (17).

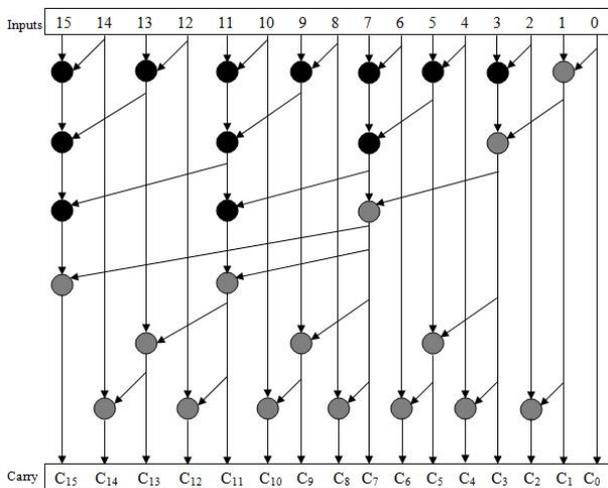


Fig. 4: Structure of a 16 bit Brent Kung Adder

$$C_0 = G_0 + P_0 C_{in} \tag{6}$$

$$C_1 = G_1 + P_1 C_0 \tag{7}$$

$$C_2 = G_2 + P_2 C_1 \tag{8}$$

$$C_3 = G_3 + P_3 G_2 + P_3 P_2 C_1 = G_{3:2} + P_{3:2} C_1 \tag{9}$$

$$C_4 = G_4 + P_4 C_3 \tag{10}$$

$$C_5 = G_5 + P_5 G_4 + P_5 P_4 C_3 \tag{11}$$

$$C_5 = G_{5:4} + P_{5:4} C_3 \tag{12}$$

$$C_6 = G_6 + P_6 C_5 \tag{13}$$

$$C_7 = G_7 + P_7 G_6 + P_7 P_6 G_5 + P_7 P_6 P_5 G_4 + P_7 P_6 P_5 P_4 C_3 \tag{14}$$

$$C_7 = G_7 + P_7 G_6 + P_7 P_6 (G_5 + P_5 G_4) + P_7 P_6 P_5 P_4 C_3 \tag{15}$$

$$C_7 = G_{7:6} + P_{7:6} G_{5:4} + P_{7:6} P_{5:4} C_3 \tag{16}$$

$$C_7 = G_{7:4} + P_{7:4} C_3 \tag{17}$$

The carry bits are used to compute the final sum using the expression,

$$S_i = P_i \text{ xor } C_{i-1} \tag{18}$$

Thus the pre-processing stage uses an inequality detector to compute the “Propagate bit, P_i ” from the input bits A_i and B_i . The post processing block also uses an inequality detector to generate the final “sum bit, S_i ”. Inequality detector performs exclusive OR operation. It gives a high output when the inputs are unequal and hence the name inequality detector. The modified inequality detector is designed using the switch level modeling in Verilog HDL code. It is implemented using 4 MOS transistors out of which there are 2 PMOS transistors and 2 NMOS transistors. The conventional transistor implementation of the inequality detector needs 12 MOS transistors out of which 6 are NMOS transistors and 6 are PMOS transistors. Figure 5 shows the circuit diagram of the modified inequality detector. Thus there is a reduction in the number of transistors in the circuit which reduces the power consumption appreciably and improves the figure of merit (power - delay product) also.

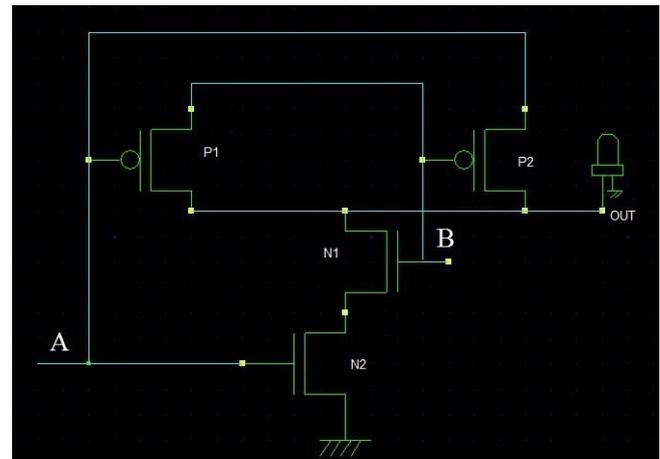


Fig. 5: Proposed Inequality detector design

The working of the proposed inequality detector is explained hereafter. When both A and B are zero, both pmos will be on and both nmos will be off. Hence the input of the pmos is transferred to the output. So output is pulled to zero. When $AB=01$, pmos P1 will be on and P2 will be off. Similarly nmos N1 will be on and N2 will be off. Hence the source voltage of P1 which is logic 1, is moved to the output. When $AB=10$, pmos P1 will be off and P2 will be on. Similarly nmos N1 will be off and N2 will be on. Here the source voltage of P2 will reach the output and hence the output becomes 1. When both the inputs are high $AB=11$, both pmos will be off and both nmos will be on. This will pull

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down the output to ground potential. Low swing can be caused at the output when A=0 and B=0. In that case we expect the output to be zero but due to the poor high to low transition characteristics of the pmos, the output will be V_{Tp} . [13-15]. The proposed architecture of the multiply accumulate unit that can be used in a Digital Signal Processor is given in Figure 6. The design may be used for several low power audio applications, for example, in a digital reverb processor. The architecture employs a modified Vedic multiplier which uses a modified Brent Kung adder to sum up the partial products. At the adder stage the modified Brent Kung adder is incorporated to add the result of multiplication and the previous result stored in the accumulator register. The accumulation process is actually taking place at the adder stage. The final result is again stored in the register. The accumulator register is basically a parallel in parallel out shift register.

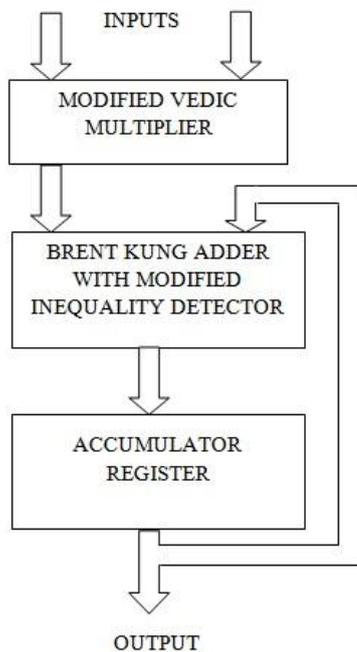


Fig. 6: Proposed MAC Architecture

IV. RESULTS AND DISCUSSION

The simulation results of the modified inequality detector and the proposed MAC unit architecture are presented in Figure 7 and 8 respectively. Also the power reports generated are shown in Figure 9 and 10. A comparison between the existing MAC design and the proposed design is given in Table 1. The comparison table clearly reveals that the proposed 16 bit MAC design using modified Brent Kung adder has given a power saving of 10% and showed an improvement of 8.34% in the power-delay product. A graphical comparison of the power and power-delay product of the two MAC architectures is presented in Figure 11 and Figure 12 respectively.

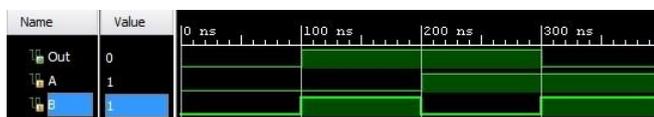


Fig. 7: Simulation result of modified inequality detector

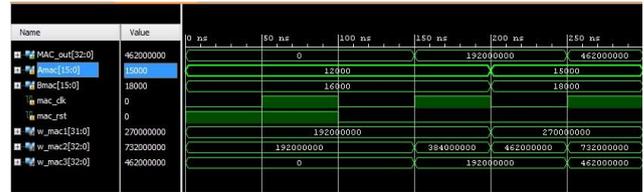


Fig. 8: Simulation result of 16 bit MAC unit with modified Brent Kung adder

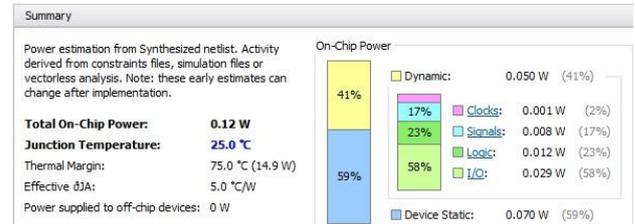


Fig. 9: Power report of 16 bit MAC unit with Brent Kung adder

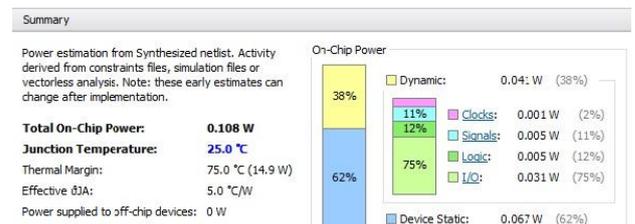


Fig. 10: Power report of 16 bit MAC unit with modified Brent Kung adder

Table 1: Comparison of MAC Architectures

Architectures	On Chip Power (W)	Power Delay Product (nJ)
16 bit MAC using Brent Kung Adder	0.12	1.798
Proposed 16 bit MAC using Modified Brent Kung Adder (BKA_MPPS)	0.108	1.648

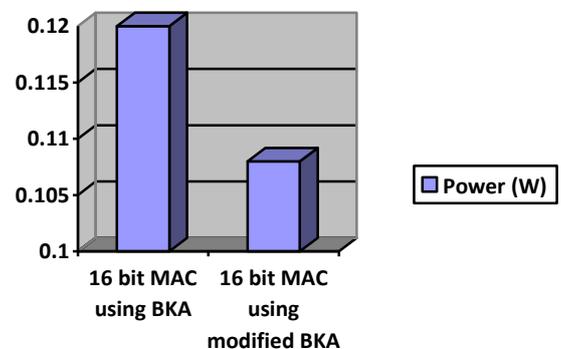


Fig. 11: Power comparison of 16 bit MAC architectures

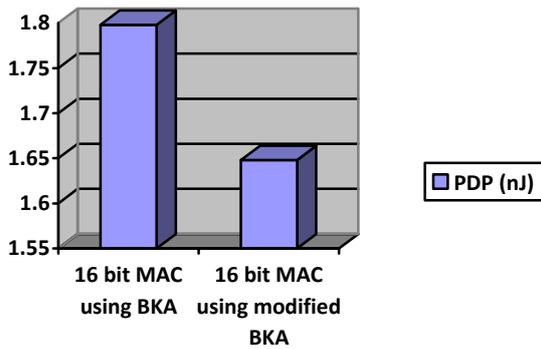


Fig. 12: PDP comparison of 16 bit MAC architectures

V. CONCLUSION

The proposed design of MAC unit using modified Brent Kung Adder which employs a modified 4 transistor inequality detector in the pre-processing and post-processing stages is found to be an efficient design in terms of power consumption and power-delay product or figure of merit. It is evident from the performance analysis that the design showed an improvement of 10% in the power consumption and 8.34% in the figure of merit. So the power efficient design may be widely used for several low power audio applications, for example, in the case of an acoustic reverb processor. In future focus may be given in reducing the delay further thereby trying to improve the speed of the system.

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