Memristor employed Accurate-Approximate Ripple Carry Adder and Ripple Borrow Subtractor Architectures

S.Muthulakshmi, A. Sivasubramanian, S.R.S. Prabaharan

Abstract: ***In today's digital era, the device size, speed and power consumption are regarded as the most sought-after design constraints of battery powered embedded gadgets. The emerging computing paradigm called "approximate computing" can be applied to fulfil the said constraints by compromising the accuracy through inexact hardware design techniques. Inherent error resilient applications viz., image, media processing etc., are well suited for approximate computing. Nevertheless, certain niche applications may demand better accuracy levels than the fully approximated output. Since adders are the basic building blocks of all arithmetic operations involving the said applications, the specific architecture involving these blocks greatly influence the efficacy of the system design. Accordingly, a new architecture is proposed in which a fusion of accurate-approximate 8-bit adder and subtractor design is developed employing memristors as both logic elements and memory components. Besides the system level validation involving the designed architecture, the standard performance metrics are deduced by employing MATLAB ™tools and the new accurate-approximate 8-bit architecture thus designed yields better accuracy as expected.***

Keywords: Memristors, Accurate-Approximate adder, Accurate-Approximate subtractor, Approximate computing, Image processing

I. INTRODUCTION

Data analytics domain is facing huge challenges in storing and handling the big data produced by the interconnected devices owing to the evolution of social networking in public eco system. Evolution of Internet of Things (IoT) facilitates the data storage in cloud and predictive analytics information based on the acquired data. The main challenge is the limitations with the CMOS storage devices like scalability, low density etc. Hence, there is a need for an alternate high density storage medium to support the storage of big data which could possibly replace the existing CMOS based storage devices along with issues centered on the computer architecture presently being used. The latter focuses on the use of von-Neumann computer architecture in which the memory unit as well as CPU are separate compartments leading to the well renowned memory wall issue that completely affects the performance of the processor. This problem becomes more severe when the data becomes a big data. Therefore, there is a need for a new computing architecture which can go beyond the von-Neumann architecture as well as the need of new device technology which supports high scalability and high density. Since Memristor is a nanoscale memory element with good scalability [1-3], it has been emerging as a plausible replacement for CMOS elements. Further, memristor can be used both as memory device as well as logic element enabling memory driven computing or Computation-In Memory (CIM) architecture that could go beyond von-Neumann architecture that obviously improves the performance of the processor. Recently, Hewlett-Packard announced the development of their proprietary 'The Machine'- the new computing system designed around the concept of memory-driven computing employing total "memristor" elements that would hit the market by 2020. The new technology is expected to disruptively improve the performance of the processor offering the solution for much sought-after memory wall problem besides changing the computing methodology [4,17]. Moreover, with an advent of memristor based universal memory as a storage medium replacing the conventional CMOS memory hierarchy, 'The Machine' is expected to further improve the performance of the processor. In addition it is estimated that around 30-75 million interconnected embedded and mobile computing devices will produce unprecedented amount of data beyond 2020 which will be uploaded to the cloud platform for further processing [5, 6]. Hence the biggest challenge lies in not only powering up the devices but also to minimize the power consumption of these devices to extend their life since most of these devices are wireless and yet battery powered devices [7]. Several low power VLSI design techniques for instance, dynamic voltage scaling, multiple threshold voltage design, energy harvesting etc., are experimented extensively by the researchers, along with the practice of nanoscale elements like CNTFET, memristor etc. to improve the power efficiency of the interconnected battery powered devices [7]. Nevertheless, another way of achieving the energy/power reduction is by introducing new computing technique that leverages performance with power consumption. This new computing technology is named as approximate computing which trades off the accuracy with performance in terms of delay and energy/power consumption [8].

Revised Manuscript Received on 30 March 2019.
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In approximate computing, owing to the nature of the data handled by the existing computers, they are likely not to generate precise output. However, some of the applications like search engine, data mining, media processing, sensor data processing etc. are tolerant to computational errors to some extent by nature, and hence accurate results are not mandatory for these category of inherent error resilient applications. For those kinds of error tolerant applications, correctness is explained by generating the results of sufficient quality rather than being accurate. Hence approximate computing can be engaged for inherent error tolerant applications that trade off the output quality with performance and energy consumption. Moreover, approximate computing is nowadays observed as one of the budding energy efficient techniques [8–14].

Approximate computing can be attained by redesigning the circuits with less number of components through functional approximation in hardware level. Another way of experimenting the approximate computing through hardware level is by voltage overscaling method where the application functions as expected in normal voltage levels and produces errored output for increase or decrease in applied voltage. To elaborate on the functional approximation, many techniques like cell replacement, logic minimization, segmentation, pruning, truncation etc. are explored widely by the research community for redesigning the hardware circuits in CMOS. With logic minimization technique, approximate circuits are designed by flipping the bits in Karnaugh map of accurate circuits which result in a simple logic function that obviously synthesizes the simple gate level circuit [15]. Another widely used technique is the cell replacement technique, in which the approximate circuits designed with less number of components replacing the accurate module of the adder architecture that introduces error in the expected output [8, 10]. Since carry propagation plays an important role in deciding the speed performance of the adder circuit, truncation technique is analyzed by the researchers by cutting short the carry propagation path which gives an approximate adder with minimal delay. While dividing the entire exact architecture into more number of segments and employing approximate logic for the least significant segment [13] to arrive at the approximate architecture is called as segmentation technique.

Since adders and multipliers are the most commonly used arithmetic circuits in computer applications, performance of these arithmetic circuits directly influence the performance of the processor [9, 22, 23]. In other words, approximate computing can be applied well on arithmetic circuits as well. This was proven in our recent paper in which memristor based adders and subtractors for approximate computing [16] is proposed for the first time and studied their operational ease for image processing application by elucidating the performance metrics. Nevertheless, all error resilient applications, as a matter of fact, do not expect to have the same level of accuracy. For instance, the security surveillance application requires the high accurate media result whereas the use of social media does suffice the less accuracy. Therefore, the approximate architecture designed for a particular error resilient application may not be suitable for the other similar applications. Hence, it is justified that redesigning the approximate architecture is found to be imperative for different applications by considering its own design constraints on the accuracy and its performance. In the present work, new *accurate-approximate* memristor based 8-bit Ripple Carry Adder (RCA) and Ripple Borrow Subtractor (RBS) architectures are proposed to improve the accuracy level of the adder and subtractors following the methodology proposed recently by Muthulakshmi et al., [16]. The new architectures proposed in the present work are verified and validated particularly in the context of image processing applications.

A. *Memristor Fundamentals*

Memristor (memory + resistor) is a fourth fundamental two terminal passive nanoscale circuit element was practically fabricated by Hewlett Packard (HP) team in 2008 demonstrating the feasibility of a memristor via resistive switching phenomenon caused by the mobility of ionic defects [18, 40] although it was mathematically conceptualized by Chua in 1971 itself. HP memristor consists of a stoichiometric layer of TiO_2 and an oxygen deficient layer of TiO_{2-x} (non-stoichiometric layer), packed between two platinum electrodes (at both ends) acting as top and bottom electrodes as shown in Figure 1(a) [18]. When the positive bias is applied across the memristor terminals, a cumulative resistive change occurs owing to the transport of mobile ions in bulk of TiO_2 layers and consequently the two terminal device achieves its Low Resistance State (LRS) which is construed as logic'1' (Write process). When the potential is reversed, the device is said to be reaching the so-called High Resistance State (HRS) by virtue of the mobile ions (vacancies) restored in their probable original state. Analogously "HRS" is regarded as logic '0' [41-44]. This behavior of ion transport across the layers brought impetus to the device characteristics as exhibiting non-volatility [44], a typical characteristic of a RAM memory device. The latter phenomenon is indicative schematically in the form of a pinched hysteresis loop (PHL), a signature of a memristor which enunciates the write (SET) and erase (RESET) operation in a cyclic fashion [18] as shown in Figure 1(b). Since HRS and LRS are analogously related to logic '0' and logic'1'of memristor respectively, it is widely used to building logic gates as well as memory applications [19-29]. Their applications are found to be useful in the following niche areas viz., analog applications, neuromorphic computing [30-34], hyper-chaotic system [35-38], approximate computing [16, 21] etc.

The first TiO_2 model devised by HP researchers in the USA [18] is named as Linear Ion drift model followed by many other models like Non-linear ion drift model, Threshold Adaptive Memristor (TEAM) model, Voltage Threshold Adaptive Memristor (VTEAM) model, etc. are reported to simulate the memristor functionality and to plausibly explain the practical device operation [45-50]. Considering the various relevant factors responsible to relate the actual device characteristics with the model parameters, VTEAM model designed by Kvatinsky et al.[48] is chosen for the simulation of our work due to its threshold characteristics.

In this paper, 8-bit approximate adder and subtractor architectures proposed with different accuracy level are designed using memristor and CMOS 180nm technology.

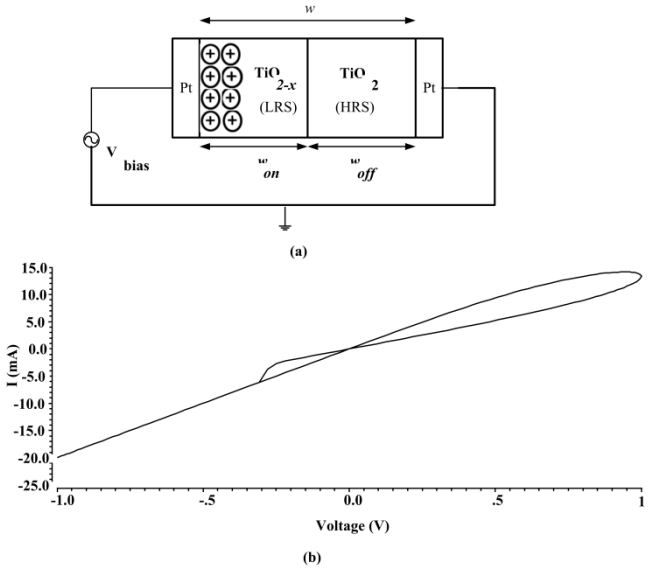


Fig. 1: The sinusoidal input signal with 50MHz frequency and 1V amplitude is applied to the memristor employed with VTEAM model. Fitting parameters that are used during simulation are $V_{off} = 0.02V$, $V_{on} = -0.2V$ $K_{off} = 5 \times 10^{-4} m/\sec$, $K_{on} = -10m/\sec$, $\alpha_{on} = 3$ and $\alpha_{off} = 1$; $w_{off} = 3nm$ and $w_{on} = 0$; $R_{on} = 50\Omega$ and $R_{off} = 1000\Omega$; $w_{init} = 0.5$. **(a)** TiO_2 based Memristor mathematical Model where w_{off} is the width of the stoichiometric region and w_{on} corresponds to the width of the non-stoichiometric region and w is the length of the active region. **(b)** Pinched Hysteresis loop defines the write/erase mechanism of memristor with threshold voltages $V_{off} = 0.02V$, $V_{on} = -0.2V$ [48].

II. PROPOSED MEMRISTOR BASED 8-BIT ACCURATE-APPROXIMATE ARCHITECTURES WITH CELL REPLACEMENT TECHNIQUE

As stated earlier, different error resilient applications expect different level of accuracy. Therefore the approximate circuits designed for one application may not be suitable for another. As the addition/ subtraction operation of all the 8-bits are approximated, the approximate adder/ subtractor architectures which we have developed already [16] are well suited for applications which can work with more approximated results. But some of the inherent error resilient applications indeed demand better accuracy. For instance, when two 8-bit numbers 10101010(170) and 10101011(171) are added, the exact adder produces 01010101 (decimal equivalent is 85) as output after neglecting the final carry whereas the designed 'complete' approximate adder produces 11111100 (decimal equivalent is 252) which is not acceptable.In order to improve the accuracy level of the adder/subtractors, we propose here memristor based *Accurate-Approximate* 8-bit Ripple Carry Adder/Ripple Borrow Subtractors as depicted in Figure2 using logic minimization technique combined with cell replacement technique as discussed elsewhere [16].

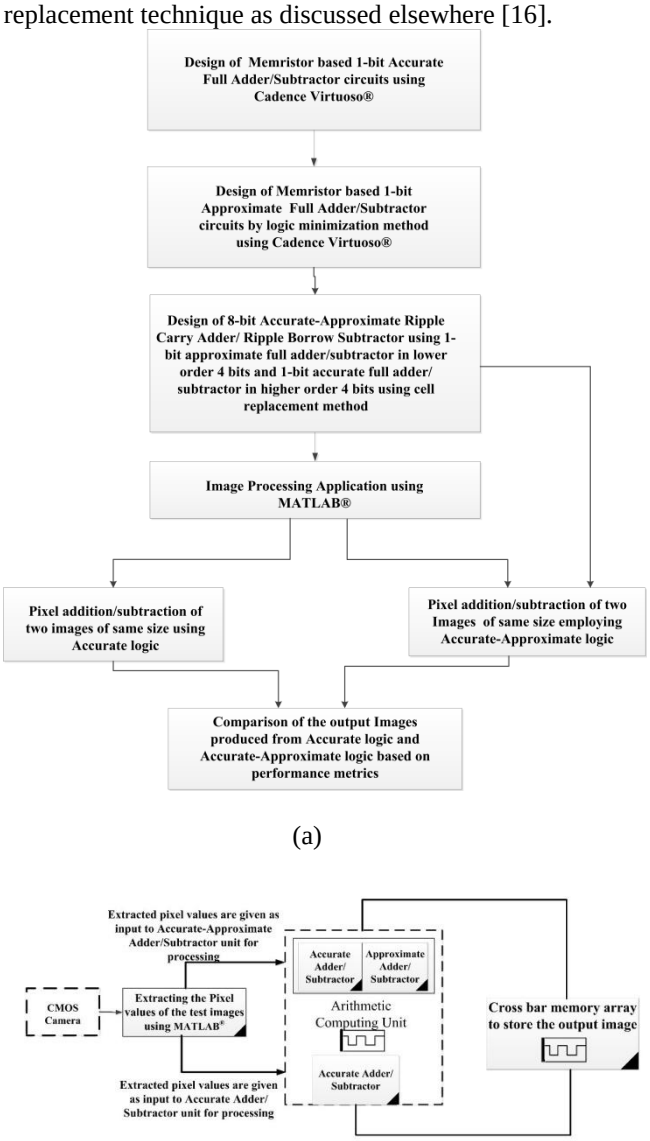


Fig. 2:(a).Methodology of our proposed *accurate-approximate* 8-bit Ripple Carry Adder/Ripple Borrow Subtractors design (b). Graphical Abstract of the entire workflow.

A. *Memristor based 8-bit Accurate-Approximate Ripple Carry Adder (MAA-RCA) Architecture*

The proposed MAA-RCA is constructed using memristors in which the entire 8 bits are divided into two parts: upper nibble of 4 bits and lower nibble of 4 bits where the addition of each bit of lower nibble is taken care by employing the memristor based 1-bit approximate full adder as shown in Figure3. As the higher order bits contribute more towards accuracy than the lower order bits, only the bits in lower nibble are replaced with memristor based 1 bit approximate full adder

cell [16] in the 8-bit memristor based exact RCA architecture. Since the lower order accurate cells are replaced by its approximated version, this design technique is termed as cell replacement technique. Further, the accurate and the approximated 1-bit full adder cell is built with 33 and 10 memristors respectively, the proposed *accurate-approximate* 8-bit RCA requires 172 memristors and produce output with the delay of 101.56ns. Compared to the '*complete*' approximate 8-bit RCA [16], the delay of the proposed *accurate-approximate* 8-bit RCA is found to be more. This increase in delay is due to the increase in number of components used for constructing the architecture. Compared to the previous work [16], this *accurate-approximate* 8-bit RCA is expected to consume more power owing to the increase in the number of components. Though the power/ energy consumption of the proposed circuit cannot be calculated exactly, it is apparent that the increase in number of components would increase the power/ energy consumption. Further the RCA output entirely depends on the carry propagation which travels from LSB to MSB, called as critical path shown (see black colored arrow) in Figure 3makes the adder to be slow that drastically affects the processing speed. Nevertheless, the proposed adder is expected to produce the output which is found to be closerto the accurate result expected;the lower order bits are approximated in this case.

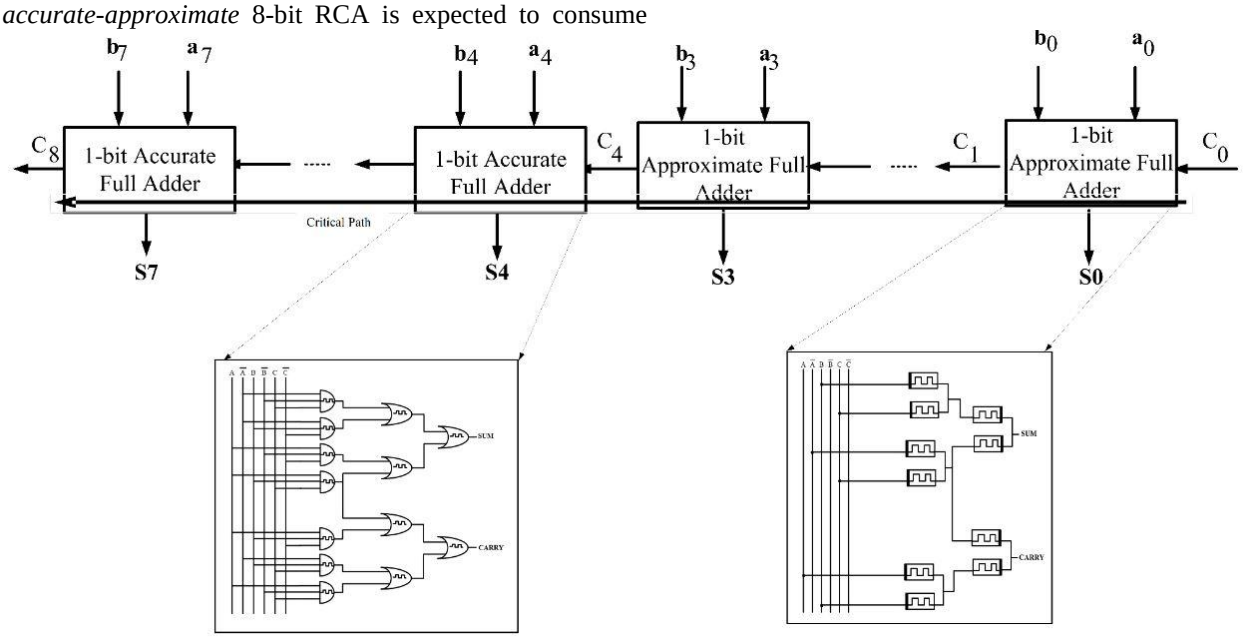


Fig. 3: Block diagram representation of the proposed memristor based a*ccurate-approximate* 8-bit Ripple Carry Adder where the addition of the higher order 4 bits are performed by employing the 1-bit exact adder designed with memristors and the addition of the lower order 4 bits are accomplished by the memristor augmented 1-bit approximate full adder designed by logic minimization technique [16].

B. *Memristor based Approximate Lower order OR Adder*

The performance of the proposed *accurate- approximate* adder is affected in terms of the required hardware area and the speed due to upsurge in number of memristors which leads to more power consumption as well. Hence, to overcome the disadvantages of the proposed MAA-RCA, we propose another *accurate-approximate* 8-bit RCA called memristor based *approximate lower order OR adder*. Here, the entire 8-bits are segmented into two parts: the accurate higher order part and the approximate lower order part, both the segments need not be of the same length. In this RCA, addition of the higher order segment is taken care by the 1-bit memristor based accurate adder and the lower order segment is performed by employing the simple memristor OR gates. The initial carry is calculated through simple memristor AND logic [51] by considering only the MSBs of the lower order segment as shown in Figure4. The carry is omitted from the lower order 4 bits where OR gates are employed.Thus the carry propagation is cut short to the length of the lower order segment. Since the critical path (highlighted in brown color) starts only from the MSB of the lower order segment which obviously decreases the delay compared to the RCA proposed earlier. In addition to that, the lower segment OR approximate RCA is designed with less number of memristors because the lower nibble is designed only with 4 OR gates for calculating the Sum and one AND gate for calculating the Carry calculations, together uses only 10 memristors, whereas the MAA-RCA uses 40 memristors. To assess the accuracy level of the proposed architectures, the two 8-bit numbers, 10101010 (170) and 10101011 (171) are considered for illustrating the result as explained in section 2. With the same example, when we added two 8-bit numbers, 10101010 and 10101011, the proposed MAA- RCA produces 01011100 (decimal equivalent is 92) as output whereas approximate lower order OR adder produces 01011011 (decimal equivalent is 91) as output. Both these outputs produce values which are considered to be close to accurate value (decimal equivalent of 85) by considering only the first 8 bits ignoring the final carry produced from MSB.

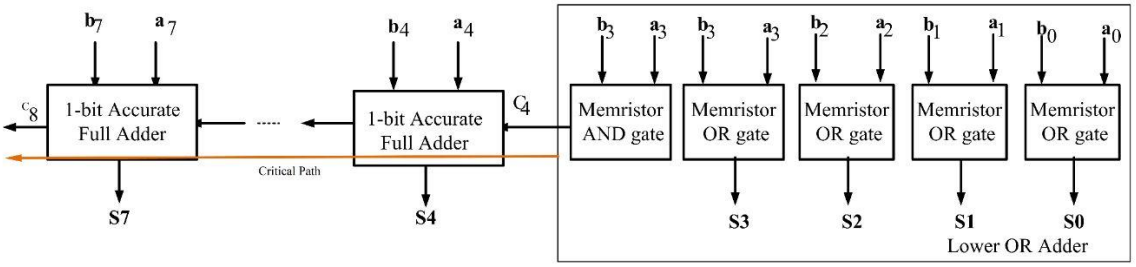


Fig. 4: Block diagram representation of approximate Lower order OR adder where lower order bits addition are taken care by simple memristor OR gates; Carry input to the higher order accurate segment is calculated by simple memristor AND gate. Carry propagation path is highlighted in orange colored arrow indicated toward S_7 starting from 5^{th} bit to 8^{th} bit.

C. *Memristor based Accurate-Approximate Ripple Borrow Subtractor (MAA-RBS)*

In the same way, when the designed memristor augmented approximate subtractor [16] is verified on foreground detection, though the images obtained from approximate subtraction process looks similar to the output image of the exact subtraction, there is a question on its accuracy level to explore the approximate subtractors on simple arithmetic calculation as subtraction of all the 8 bits are approximated [16]. For instance, when 01111101 (125) is subtracted from 11111010 (250) through exact subtraction process, it produces 01111101 (125) as output whereas the approximate subtractor1 (*ApXs1)* produces 01111000 (120) as output and approximate subtractor2 (*ApXs2)* produces 11111111 (255). Likewise, 01111101 (125) is subtracted from 10101001 (169) through exact subtraction gives out 00101100 (44) whereas *ApXs1* produces 00101001 (41) and *ApXs2* produces 11111101 (253) as output. It is observed that *ApXs2* deviates very much from the accuracy in both the cases. Hence the 'complete' RBS designed with *ApXs2* as a basic cell is not suitable for arithmetic applications though the approximated image is acceptable.

Table 1: Proposed approximate subtractor truth table

Input			Actual`		Approximation III *(ApXs3)*	
X	Y	Z	D	B	D	B
0	0	0	0	0	0	0
0	0	1	1	1	1	1
0	1	0	1	1	0 ×	0 ×
0	1	1	0	1	1 ×	1
1	0	0	1	0	0 ×	0
1	0	1	0	0	0	0
1	1	0	0	0	1 ×	0
1	1	1	1	1	1	1

x denotes the flipped bits.

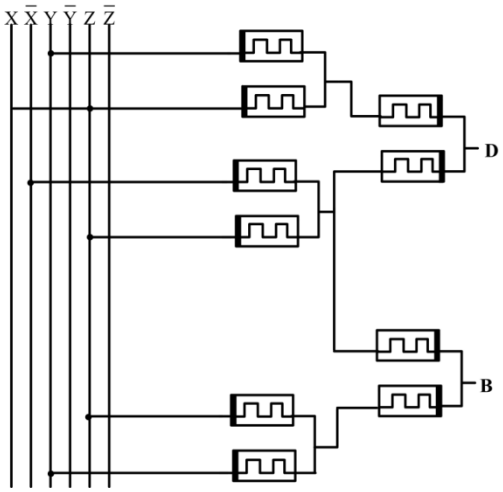
Hence to find out another suitable approximate subtractor which can further diminish the number of components with better accuracy, we propose *ApXs3* with 50% error rate[10-12] in difference and 12.5% error rate in borrow in exact subtractor truth table using logic minimization technique[16] to derive the corresponding approximate subtractor truth table (refer Table 1). The SOP functions (1a &1b) for difference and borrow are derived using K-map reduction. Figure 5a represents the circuit diagram of *ApXs3* and its output waveform simulated in cadence virtuoso® is shown in Figure5b**.**

The SOP functions for difference and borrow for ***ApXs3*** is given by,

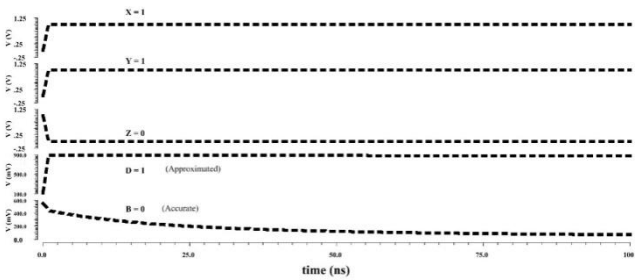
$$D = \bar{X}Z + XY \quad (1a)$$

$$B = \bar{X}Z + YZ \quad (1b)$$

Since the proposed *ApXs3* is constructed only with 10 memristors, it occupies less hardware area along with other known benefits such as less delay and low power consumption.



(a)



(b)

Fig. 5(a). Schematic representation of *ApXs3* with 50% error rate in difference and 12.5% error rate in borrow.**(b).**Output waveform of *ApXs3* for the input combination X = 1, Y = 1, Z= 0, the generated difference D = 1 (approximated) and the borrow B = 0 (accurate) as expected. Figure 6depicts the critical circuit parameters such as number of memristors, delay (assigned to the left side vertical Y1 axis) and cumulative error rate (Assigned to Y2 axis) of all the 1-bit exact/approximate adder and subtractor circuits.

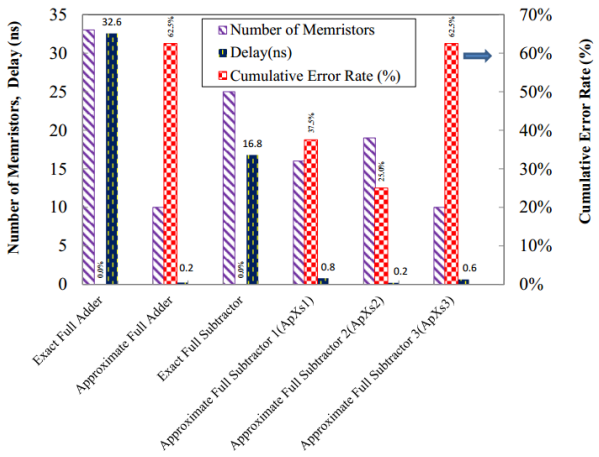


Fig. 6: Comparison of Critical Circuit parameters involving 1 bit approximate adder/subtractors designed using memristors in the present study. Here, Cumulative Error Rate indicates the error rate of Sum + the error rate of Carry in case of full adder and the error rate of Difference + the error rate of Borrow for full subtractor. The total number of memristors used for realizing the circuit depends on the error rate.

The *'complete'* approximate RBS built using *ApXs3* is applied on subtracting two 8-bit numbers as mentioned above. This approximate subtractor produces 01111000 (120) as output when 01111101 (125) is subtracted from 11111010 (250) and 00101001 (41) as output when 01111101 (125) is subtracted from 10101001 (169). *ApXs3* produces output with the same level of accuracy of *ApXs1* with an error distance [10-12] of 2.

Hence, to improve the accuracy of the designed subtractors further, we propose here a new memristor based *accurate-approximate* 8-bit RBS using 1-bit exact and approximate subtractors realized with AND & OR gates by using MRL circuit protocol [16, 51]. As described in the adder section, the lower 4 bits of 8-bit RBS are replaced by the approximate subtractors (*ApXs1/ApXs2/ApXs3*) as shown in Figure 7**.**

Based on the analysis we have summarized the total number of memristors used for designing the 'complete' approximate and *accurate-approximate* 8-bit architectures and their respective propagation delay in table 2.

Table 2: Comparison of Critical Circuit parameters involving 8-bit *accurate-approximate* architectures designed using Memristors.

	Number of Memristors	**Delay (ns)**
***Complete* 8-bit approximate RCA[16]**	80	5.48
***Complete* 8-bit approximate RBS(ApXs1)[16]**	128	24.45
***Complete* 8-bit approximate RBS(ApXs2)[16]**	152	53.65
***Accurate- Approximate* 8- bit RCA**	172	101.90
***Approximate lower OR adder* 8-bit RCA**	140	101.60
***Accurate-Approximate* 8-bit RBS (ApXs1)**	164	106.50
***Accurate-Approximate* 8-bit RBS (ApXs3)**	140	105.76

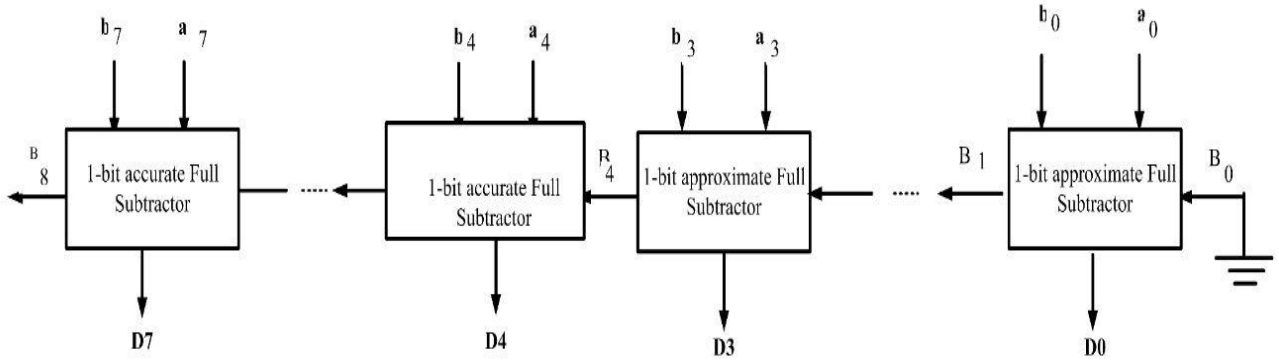


Fig. 7: Block diagram representation of the proposed *Accurate-Approximate* 8-bit Ripple Borrow Subtractor where lower 4 bits are replaced by 1-bit memristor based approximate subtractors *ApXs1/ApXs2/ApXs3* highlighted in red color blocks. Here the critical path delay originates from LSB to MSB because the subtraction of each bit depends on the borrow signal of the previous bit.

It must be noted that in the proposed new 8-bit *accurate-approximate* architectures designed with memristors, it is inevitable to have inverters, buffers, and CMOS logic gates in the intermediate states as part of the entire architecture in order to have magnified input signal wherever required.

D. *Verification of the proposed architectures on Image processing application*

- **Image addition**

As proposed by Xiao Fang et al. [52], the crossbar memory array realized with memristor can be used to store the image in the form of pixels. The stored data can be accessed via the processor control unit through proper address location to write/read the data. The images of bigger size can be stored by simply increasing the rows and columns of the crossbar array. The crossbar array can be used to store the binary as well as the grayscale values. The storing of grayscale pixel values are facilitated by the presence of the copious resistance states of the memristor. The HRS state of the memristor denotes the grayscale value '0' and the LRS corresponds to the grayscale value '255'. The intermediate resistance states represent the interim grayscale values which can be accomplished by varying the pulse width of the applied signal keeping the constant voltage level.

Further, the performance of the proposed *accurate-approximate* RCA and *the approximate lower order OR adder* RCA is evaluated on image addition where two images of the equal size (i x j) are added by employing the proposed *accurate-approximate* adders which generate an output image of the same size (i x j) as shown in Figure 8. A *Lena* image of 512 x 512 size is added with 512 x 512 size image of *Bright Dark circles* using the proposed *accurate-approximate* adder as well as with the exact adder and found that the image generated through *accurate-approximated* addition looks similar to the output image attained through the accurate addition process as presented in Figure 8.

- **Foreground detection**

In image processing application foreground detection is one of the important processes since many applications need to elucidate only the changes in the image/video sequence, they do not need to provide all the details concerning the evolution of movement in an image/video sequence. Hence, the proposed *accurate-approximate* 8-bit RBS designed is employed on subtracting the pixels of two images namely, Image 1 and Image 2, which are in equal size. Similarly both the images are subtracted using the exact subtractor as well. It is observed that the output image of *accurate-approximated* subtraction resembles the output image produced through the exact subtraction process as shown in Figure 9.

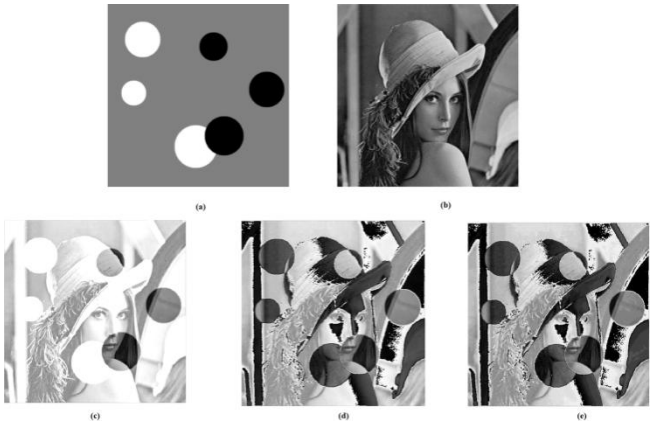


Fig. 8: Image addition using proposed *accurate-approximate* adder and lower order OR approximate adder. (a). Input image 1(bright and dark circles image) (b). Input image 2 (*Lena*) (c). Resultant image obtained using exact adder (d). Resultant image attained through *accurate-approximate* adder (e). Resultant image obtained using lower order OR adder.

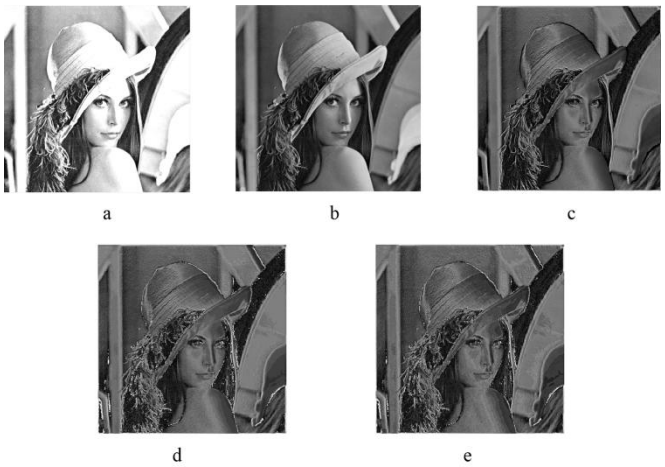


Fig. 9: Foreground detection using proposed accurate-approximate subtractors. (a). Input image1 (b). Input image2 (c). output image after exact subtraction (d). Output image using *ApXs1* (e). Output image using *ApXs3.*

III. RESULTS AND DISCUSSION

From the literature [10-12] it is understood that the quality of the resultant images can be determined by computing the performance metrics for the image. Hence various performance metrics suggested in [16] have been carried out to validate the above observation using MATLAB™ and the results are summarized in Tables 3 and 4 for the proposed *accurate-approximate*adders and subtractors.

Table 3: Performance metrics of proposed memristor based *accurate-approximate* adder and *lower order OR adder.*

Parameters	*Accurate-Approximate* 8-bit RCA	*Lower order OR Adder*
AD	72.340	70.4927
MAD	255	255

MAE	72.340	70.4927
MSE	1.46×10^4	1.525×10^4
NAE	0.0019	0.0015
SC	1.5373	1.7823

Upon analyzing the values of the deduced performance metrics, it is understood that these values are very low. But compared to the previous work [16] the values of these parametershave improved for the proposed *accurate-approximate* adder as well as for the lower order OR adder because of the presence of accurate modules in higher order bits. Furthermore, it is noted that the value of MSE has been found to be 51% and 53% less for the proposed *accurate-approximate* adder and *lower part OR adder* respectively. PSNR is indirectly proportional to MSE[16]. From the results, it is understood that the visibility of an image cannot be judged by the PSNR values: sometimes image having low PSNR value may look better than the image with high PSNR [53].

Table 4: Performance metrics of proposed memristor based *accurate-approximate* subtractors

Parameters	***ApXs1***	***ApXs3***
AD	1.0757	2.3758
MAD	10	15
MAE	1.0757	2.3758
MSE	5.6119	21.8267
NAE	1.0×10^{-4}	2.968×10^{-4}
SC	0.8060	0.8505

On the other hand, the PSNR value of the approximated image obtained through MSE for the *accurate-approximate* subtractor constructed by employing *ApXs1/ApXs3* is in the acceptable range of 30dB-50dB whereas the PSNR value deduced for *accurate–approximate* RBS constructed using ApXs2 is '0'; hence this is not suitable for applications fairly demanding accurate results. As expected, the proposed new *accurate-approximate* architectures achieved better accuracy which can be applied on applications requiring better accurate results in its output.

IV. CONCLUSION

In this paper, we have designed and described the operation and performance of new types of memristor augmented 8-bit *accurate–approximate* adder and subtractor architectures using logic minimization technique combined with a cell replacement technique for the first time. Owing to the characteristics of non-volatility, scalability and low power consumption, memristors are employed as memory device as well as logic element to explore an approximate computing technique in the presentwork. Further, the designed *accurate-approximate* architectures are compared with the critical circuit parameters such as the number of memristors and delay. Apart from that, the process of storing and retrieving the image in memristor based crossbar memory array has been studied. In addition, the performance of the designed *accurate-approximate* adder and subtractor architectures have been analysed on image addition and foreground detection technique respectively by adding/subtracting two greyscale images of the same size. The proposed *accurate-approximate* architectures rendered the enhanced output images compared to our previous work [16] owing to the presence of accurate modules in the higher order bits. Moreover, the proposed architectures have been found to be versatile as it can be used for arithmetic operationsin general since the obtained results are closure to accurate results.

ACKNOWLEDGEMENT

Authors (S.M and A.S) would like to thank VIT for the computational provisions extended to carry out this work.

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