

Network on Chip: A Survey on Router Design and Algorithms

Krutthika H.K, Rajashekara



Abstract: The increase in the applications for the innovative technologies has further increased the computing resources in a single chip. In such scenario, different application desires computing resources to build on a Single Chip. Therefore, interconnection between the IP cores becomes another challenging task. So, this led to the innovation of the Network on Chip as a novel platform those networks inside the System on Chip. There are many disadvantages of the traditional bus based architectures, as it blocks the traffic. The network topologies, routing algorithms and router architectures are the utmost critical part of any network structure. The execution of the system is measured by throughput. The throughput and effectiveness of interconnect depends on the system parameters. In this paper, we are reviewing the previous methods and approaches of routing algorithms and router architectures of NoC.

Index Terms: Network on Chip (NoC), System on Chip (SoC), Routing, Intellectual Property (IP), Network Interface (NI).

I. INTRODUCTION

Recently NoC is playing a vital role in development in VLSI design. Many applications were developed due to increasing levels of integration. Since the introduction of VLSI, the die area, power and dictated clock speed dominated during the communication of processors within the chip. The main features of NoC is to establish the communication, it can be intra chip or inter chip communication.

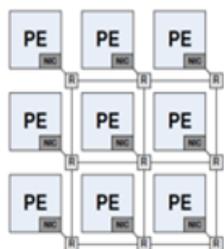


Figure.1 NoC architectures

All links in NoC can be concurrently used for data transmission, which provides a high level of parallelism and it overcomes the drawbacks of traditional bus based architectures. NoC platform is a scalable architecture, as it

reduces congestion in the routing, power efficient and operates at higher frequencies. Figure.1 shows the NoC architecture [1]. It has nodes, processing elements and the links which are connected to the PEs. Each PE is attached to NI and NI is connected to PE to a local router. The packets are sent based in the routing information which is present in the routing table. For designing any communication network, router is an important component. The router performs hop to hop delivery of packets. Designing a router is a challenging task as it depends on many factors such as implementation cost, power and area.

II. SCOPE AND PURPOSE OF THE WORK

There are many routing algorithms and router architectures for NoC and based on the traffic conditions, different routing algorithms are used. This paper reviews different types of routing algorithms, router architectures and switching methods used for routing the packets from one terminal to another terminal. This paper also discusses the current challenging issues in the NoC.

III. ROUTING ALGORITHMS

A routing algorithm is a conventional procedure used to direct the traffic proficiently. When the packet leaves the source terminal, the best path is chosen from the routing table and then it is forwarded to the destination. The routing decisions are taken whenever there are changes in the network topology or traffic load. The calculation of the optimal path relies upon some possibly contradictory metrics [2].

- Reduces the power required for routing.
- Delay and exploitation of the traffic in the network are the key performance parameters.
- Dynamic change of path when there is link failure.

The routing techniques is classified into different types,

- Static or dynamic routing
- Distributed or source routing
- Minimal or non-minimal routing

A. Static and Dynamic routing

Static routing:

In static routing, the path is stationary from source terminal to the destination. The path for routing is determined by the network administrator and is implemented where the network parameters and the environment are static [7].

Dynamic routing:

The adaptive path in the dynamic routing is considered based on the traffic on links and also on the real-time traffic.

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The router is responsible for the construction, maintenance and updating of the dynamic routing table by adding or deleting the terminals stations.

B. Minimal and non-minimal routing

Minimal routing:

One of the most frequently used and simplest algorithms in NoC is the XY routing. This routing algorithm is deterministic, static and deadlock free routing algorithm. In XY routing, the packet is routed first through X-axis and then Y axis till it reaches the destination. The router attains deadlock when more number of packets attempt to use the same route and the routers do not releases the resources so the routing is locked state.

Non-minimal routing:

If minimal path is not available, then the packet takes longer route to reach the destination. As the number of alternate paths gets increase, the congestion in the network can be avoided. The main drawback is overhead of extra power consumption.

C. Switching Techniques

Circuit Switching

In this technique, the route to the destination is reserved between source and destination before transmission of data. The latency and packet loss will be reduced and the links are occupied for the considerable amount of time.

Packet Switching

This is the most universally used switching technique in the NoC. Here the packets are transmitted from the source and they reach destination independently through different paths. So, a variable amount of delay is introduced due to conflict in the router along the path.

Packet switching is further classified as,

- Store and forward.
- Wormhole
- Virtual Cut-through

(i) Store-and-Forward switching:

Store-and-Forward switching will wait until the entire frame has arrived prior to forwarding it. This method stores the entire frame in the memory. Once the frame arrives into the memory, the switch checks the destination address, source address, and the CRC. If no errors are present, the frame is forwarded to the appropriate port. This process ensures that the destination network is not corrupted or duplicated.

(ii) Wormhole Switching:

In this switching technique, the packets are divided into small units called flits. Each router is assigned number a flits in its buffer. The header flit carries the address of the route and all the other flit uses to address to reach the destination. If their is congestion in the transmission path then, the flits are blocked.

(iii) Virtual Cut-through Switching:

In this method, the switch starts to forward the packet before receiving the whole packet. The main advantage of this switching technique is, it reduces the latency and error. This technique is achieved successfully, if the clocks of both the sending and receiving terminals are synchronized.

IV. ROUTER ARCHITECTURES

A. VIRTUAL CHANNEL ROUTER (VCR)

In this router architecture, the source routing algorithm and wormhole flow control with virtual channels are used. The

architecture design is shown in the Figure 2. This router comprises of five inputs and outputs, and 4 inputs are connected to the router in its PE and the last input is connected to the local router core. Each input port has 4 virtual channels and they are de-multiplexed and buffered in FIFOs. The VCHs are multiplexed over again and it drives the

channel to the crossbar. The forwarding of the packets in the crossbar unit is controlled by an Arbitration Unit (AU). Here

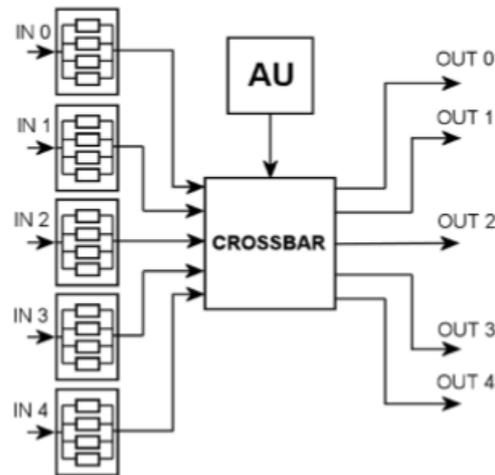


Figure 2. Router architecture of VCR.

the main function of the AU is to avoid conflicts between the VCHs and ensures rational arbitration. The arbitration is deterministic and rational, and therefore the conflicts can occur only at the output ports. Therefore this router architecture attains a 100% throughput.

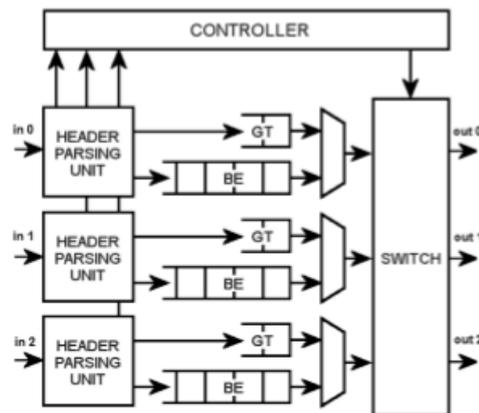


Figure 3. Router architecture of VCR.

B. ÆTHEREAL

This router architecture [1] combines guaranteed throughput (GT) and Best Effort (BE) routing. It uses the wormhole network flow control and the contention free source routing algorithm. The router architecture is shown in the Figure 3.

The \AE thernet uses virtual channels and the other shared channels, and they are connected by Time division multiplexing. Before the packet transmission, the header flit (i.e., first flit) stores the whole routing path. The header analyzing unit extracts the first flit and it moves the flit to a

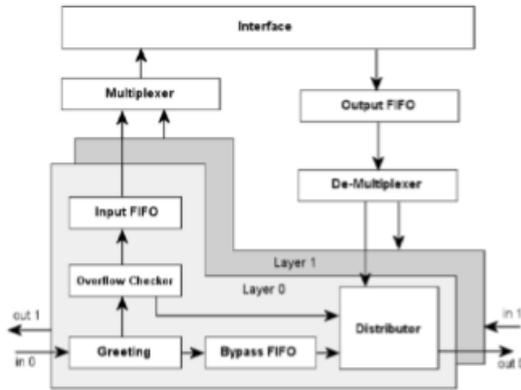


Fig 4 : prototype architecture of router.

GT or BE FIFO. The basic operation of the controller is to schedules the flits for the next flit. After scheduling to the GT-flits, the remaining destination ports can assist the BE-flits.

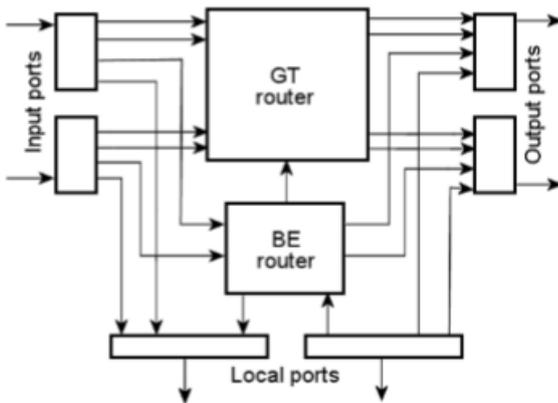


Figure 5. \AE THEREAL router architecture

C.XPIPES

This router architecture [1] uses wormhole network flow control and source routing algorithms. Routing is deterministic, so the switch has simple structure and routing decisions are made at the beginning before the transmission of the packet. Different parameters has to considered while designing the router architecture- the arbiter techniques, network topologies, number of Inputs/Outputs and routing algorithms.

D.PROTEO

This router architecture [16] the bridges connect many networks as shown in the Figure 4. This architecture has two types of routers, the initiators and the targets. The main functionality of the initiator is to generate requests to the

target router, while targets can just react to these requests. The header of the packet consists of the destination address and the reception block, which is at the input port. The reception block detects the packets destination address and it compares with the local core address. If the addresses of both

the local core and destination address are same, then the reception block writes the packet to the input FIFO through the overflow checker or else the packet is written to the bypass FIFO.

E.MANGO

This router architecture is a clockless Network on Chip system architecture is shown in the Figure 5. The Guaranteed Throughput and Best Effort (BE) routing is achieved by using Wormhole Network flow with controlled channels. For Clockless router architecture, the TDM cannot be used. The advantages of the clockless system are it provides maximum speed and zero idle power. The separate GT and BE router elements, I/O ports which are connected to the nearest router and the local port to the processing element. The routing of the packet is done by analyzing the packets header by the BE. [20]

F.SPIN

The SPIN architecture [3] is a highly scalable and uses wormhole network flow control. The topology used in this architecture is fat tree and the nodes are the routers and leaves are terminals. The packet routing is realized as follows. The packet moves up to the node i.e., the router, along any accessible path, which is a common predecessor with the terminal, then the packet is forwarded to the destination along the only probable path. There is a 4-flit buffer on each input port and two 18-flit output buffers shared between output ports. To reduce the congestion, the highest priority is given to the output buffers [17].

Table 1. Analysis of different Router architectures

ROUTER	ALGORITHM	FLOW CONTROL	TOPOLOGY
VIRTUAL CHANNEL ROUTER	Source routing	Wormhole	2D
\AE THEREAL	Source routing	Wormhole	Mesh
XPIPES	Contention free source routing	Wormhole	Any
PROTEO	Destination address is stored in the packet header	Wormhole	Ring
MANGO	Source routing	Wormhole	Mesh
SPIN	Turn around	Wormhole	Fat Tree

V.CURRENT WORKS IN NoC ROUTER ARCHITECTURES

As different NoC router architectures have attracted a significant amount of research attention, many router architectural designs have been proposed in the past decades.

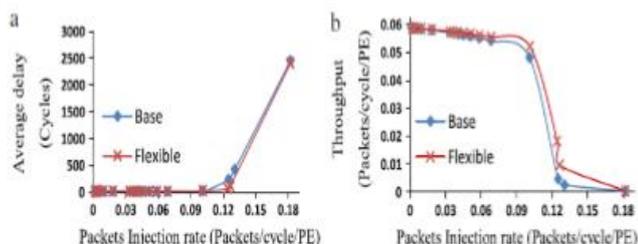


Figure 6. Delay (a) and throughput (b) characteristics versus injection rate under Nearest-Neighbor traffic.

However, the enlarging network structure makes router

designs more complex and is a challenging task. In paper[11] Mostafa S. Sayed proposed Flexible router architecture. The high power consumption, area and complex logic [6] can be reduced by decreasing the size of the buffer and the VCHs. The router performance can be improved by the cumulative increase in the saturation rate for Hotspot, Uniform and nearest neighbor traffic pattern cases, But, as the rate of arrival is packets increases, the delay will gradually increases.

In [12] S.Karthikeyan proposed a Low power NoC router architecture design, which reduces the data transferring time between source and destination. It uses weighted distance based Virtual circuit switching technique and this technique optimizes the path selection work which intern increases the system speed level and reduces the latency. But as the network size and traffic increases, the energy consumed will also get increases.

In the paper [13], the author proposes Router design with buffer stealing. Buffer- stealing mechanism is proposed where the input channels uses the unused buffer space from the other input channels at the run-time. The proposed mechanism has increased the average throughput by 23.47% and 22% overhead by hardware resources. But this router does not support reconfigurable system and also real-world applications.

VI. RESEARCH CHALLENGES IN NoC

Some of the challenges encountered in Network on Chip are,

- Deadlock and Livelock freedom in Routing is a major issue.
- As the traffic increases, handling the traffic will become the challenging task and are more prone to failures. These failures may disrupt the topology under certain circumstances.
- Real time transmission of multiple data with high data rate
- Security of data stored and also while routing is a major concern.
- Efficient usage of resources.
- Single router architectural design does not support different traffic cases.

VII. CONCLUSION AND FUTURE WORK

This paper summarizes the current issues in NoC router architectures and design. We have identified the current gaps and open research areas. Our future research will focus on these open problems and propose effective solution for the same.

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