Different Approaches to Achieve high SNDR in Low Power Sigma Delta ADC

Veerayya Javvaji, Sarada Musala

Abstract*— Analog to digital converter is an essential block in any on-chip digital circuit. Out of different ADC's oversampling ADC's uses sampling frequency more than the Nyquist rate which eliminates abrupt cutoff in anti-aliasing filter. A sigma-delta ADC is a type of oversampling ADC which uses a noise shaping circuit to achieve high resolution. The performance metrics such as Figure of Merit (FOM), Signal to noise distortion ratio (SNDR), bandwidth, the sampling frequency of sigma-delta ADC are important in the design of ADC. Different approaches to achieve high SNDR are discussed in this paper as SNDR is one of the primary factors of ADC.

***Keywords*—ADC, SNDR, FOM, Capacitive-Coupled Chopper Instrumentation Amplifier (CCIA).**

I. INTRODUCTION

The need for prosthetic devices in medical science brought revolution in the use of low power consumption and high SNDR circuits in portable medical devices, which create demand in the design of high SNDR analog to digital converters. Sigma Delta ADC's are well suited for digitizing low-frequency signals with high precision.

Sigma Delta ADC consists of Loop Filter, Delta modulator and Digital Filter. The performance of ADC such as SNDR can increase by using CIFB topology and power can be reduced by CIFF topology in Loop Filter.

Different proposals have been proposed for the past decades for solving challenges in the design of high-SNDR low power sigma-delta ADC's. In this paper, different approaches to get high SNDR in sigma-delta ADC's are reviewed. A comparison is done for different parameters such as supply voltage, bandwidth, sampling frequency, power consumption, SNDR, FOM and area.

This paper is organized as follows – various techniques and methods used in different papers to improve circuit parameters are described in section-II. Then a comparison between different topologies is given section-III. Finally, conclusion is given in section-IV.

II. DIFFERENT APPROACHES

Different proposals have been proposed for the past decades for solving challenges in the design of high-SNDR low power sigma-delta ADC's. In this paper, different approaches to get high SNDR in sigma-delta ADC's are reviewed. A comparison is done for different parameters such as supply voltage, bandwidth, sampling frequency, power consumption, SNDR, FOM and area.

In-channel Sigma-Delta ADC

A sigma-delta ADC [1] is employed on behalf of SAR ADC [2] as it offers high precision which is suitable for neural recordings. Here a dedicated SigmaDelta ADC is used for each channel rather than using multiplexed ADC. This circuit is designed to operate at low power supply voltage about 0.6V. Taking the advantage of low supply voltage and passive integrator power consumption can be reduced. Here switched capacitor resistors are used in the design of subtractor and integrator, which reduces power consumption but the capacitor-based voltage divider provides attenuation by a factor of 1/19 on input signal. This small input at comparator translates small SNR. The differential pair transistors exhibit non-linearity under small voltages, so a feed-forward circuit is employed to minimize the effects. Noise Shaping circuit improves the SNDR of a signal [3]. Noise shaping order is directly proportional to the number of integrators. So, a first-order noise shaping topology is employed for less power consumption as shown in Fig. 1.

The performance of the proposed circuit can be analyzed by SNDR.

$$SNDR = \frac{P_{signal}}{P_{Noise} + P_{Distortion}} \tag{1}$$

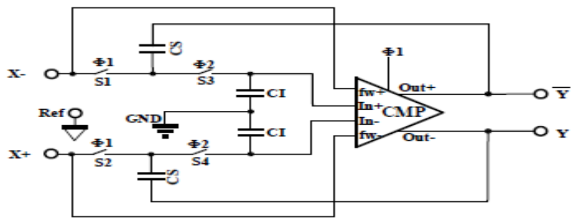

Fig.1 In-Channel Sigma-Delta ADC

This type of ADC can be used in neural recording applications. The main advantage of this method is power consumption is less when compared with all other circuits [2], [3], [4], [5], but low SNDR due to use of only first order noise shaping circuit. SNDR increases as the order of the noise shaping circuit increases by reducing quantization noise [4].

Sigma-Delta ADC using Non-Linear DAC

This circuit is used at the front end of transmitter in hearing aid applications. The main criteria for hearing aid are Dynamic range(DR) and area. DR of normal hearing

Revised Manuscript Received on February 11,2019.

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person is about 120dB and 60 dB for hearing loss person it may vary from person to person. Using of non-linear DAC in feedback takes advantage of trade-off between Dynamic Range and distortion. The architecture of Sigma-Delta ADC using non-linear DAC is shown in Fig.2

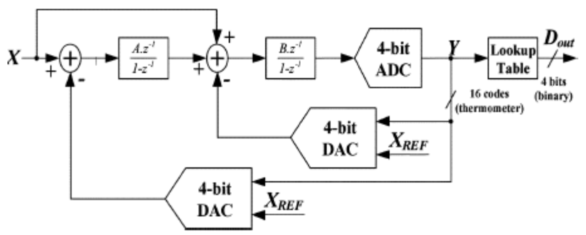

Fig.2 2nd order Sigma-Delta ADC using non-linear DAC

The non-linear DAC is implemented using a switched capacitor circuit. Due to non-linear characteristics of DAC, the signal from ADC is distorted which is corrected by a digital lookup table. The non-linear character sticks of DAC also reduce quantization noise power for small input signals, as a result Dynamic range is increased [5] which is not the case with linear DAC. Reduction in noise power improves SNDR.

This type of ADC can be used in hearing aid applications. Compared with previous method [1] SNDR is increased but power consumption is increased.

Incremental 3rd order Sigma-Delta ADC

Multi-channel biosensor applications need low power and high SNDR, ADCs. Incremental Sigma Delta ADC are attractive for medium-to-high resolution applications. Limitation of Incremental Sigma Delta ADC when compared with conventional Sigma Delta ADC is low SNDR at very low Over Sampling Ratio (OSR).

In this circuit an 3rd order incremental Sigma-Delta ADC is used as shown in Fig. 3. This structure is more useful in Bio-sensing applications. This circuit uses CIFF configuration to minimize the degradation of performance. As the name indicates 3rd order it use three integrators, the first integrator uses telescopic structure to lower the noise where as second and third uses folded cascode for marginal increment of signal swing [6].

This type of ADC can be used in multi channel applications. The main drawback of this method is power consumption is more when compared with circuits [1], [5] with an improvement in SNDR.

VCO based Sigma-Delta ADC

This circuit is used in voice recognition applications. Time domain encoding is employed as an alternative for voltage or current encoding. In this circuit a sigma-delta ADC is implemented without an operational amplifier. An operational amplifier is replaced with a VCO and additional digital circuitry [7] which operates as time domain integrator. Single-bit or Multi-bit [8] can be used in interconnection of integrator stages. A single-bit interconnection is compatible for MEMS microphone.

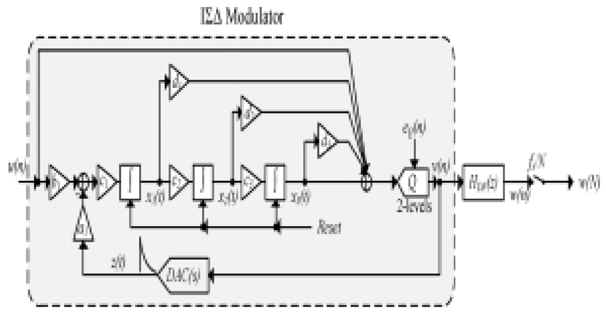

Fig. 3 3rd order Incremental Sigma-Delta ADC

This configuration can be used in low sensing applications. The VCO based sigma-delta modulator consists of two single-ended branches which are configured as pseudo differential architecture as shown in Fig. 4. This architecture confines the level of distortion within acceptable range without any linearity correction.

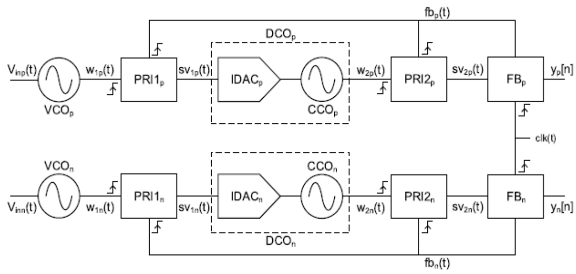

Fig. 4 Pseudo differential 2nd order VCO based Sigma-Delta ADC

The main drawback of this method is power consumption is more when compared with circuits [1], [5], [6] with an improvement in SNDR.

Incremental Sigma-Delta ADC

This circuit is used in Multi-Site Neural Recording systems. An 2nd order CT incremental Delta sigma ADC proposed in is shown in Fig. 5 is having some passive components which occupy large area on the IC. Fig. 5 shows that it contains two amplifier stages.

In this circuit area optimization techniques are employed in different blocks such as feed forward path from first modulator to input of second modulator and in feedback DAC. Looking in to the circuit R_2 and C_{ff} offers large resistance. To reduce the resistance R_2 is spitted into R_{2a} and R_{2b}.

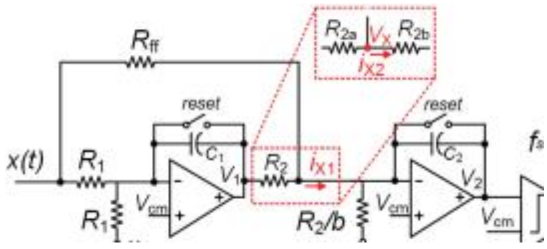

Fig.5 2nd Order incremental Sigma-Delta ADC

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Before splitting the current is given by

From the analysis the initial and final values of R_{ff} and R_2 reduced by 45%[5]. Another component in the circuit is feedback DAC, its area is optimized by using current steering circuit.

This type of ADC can be used in neural recording applications. This circuit consumes less power than [3], [4] and has more SNDR when compared with circuits [1], [5], [6], [7], [9] ADC.

F. Chopped CT Sigma-Delta ADC

This circuit uses CCIA shown in Fig. 6. This structure is more useful in neural recordings [10]. To reduce the power consumption an Gm-C integrator is employed. Open loop structure of Gm-C integrator increases non linearity. A source degeneration circuit is used to overcome the linearity problem. Taking the advantage of low power Gm-C, adding source degeneration will not increase the power consumption of overall circuit.

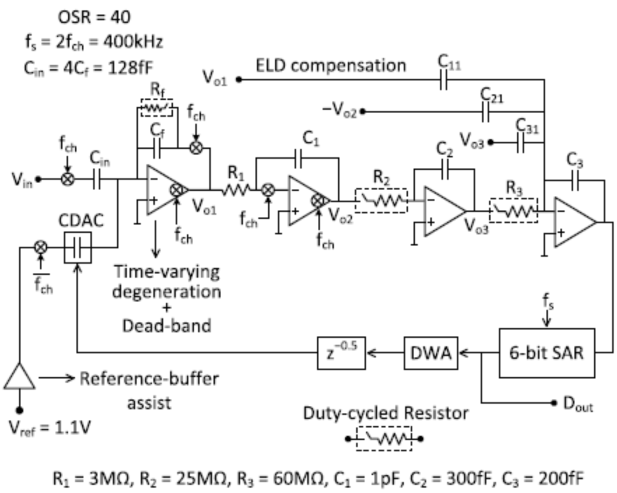

Fig. 6 Chopped CT Sigma-Delta ADC

This type of ADC can be used in applications where low power and high SNDR are required such as neural recordings, EEG. Compared with [1], [5], [6], [7], [9] this circuit has SNDR of 93.5dB.

III. COMPARISION RESULTS

Table.1 summarizes the performance of different circuits. It shows that Chopped Sigma-Delta ADC is having highest SNDR when compared with remaining circuits.

TABLE I. COMPARISION RESULTS

	[1]	[5]	[11]	[12]	[15]	[16]
Type	DT	CT	CT	CT	CT	CT
Band Width f_s in (KHz)	10	-	2	20	10	5
Sampling Frequency f_s in (mhz)	-	1.25	0.320	20	2.56	-
SNDR(dB)	**55.2**	**61.5**	**64**	**69.6**	**70.8**	**93.5**
Dynamic Range(dB)	-	-	68.2	93.5	77.6	-
Power (µW)	0.11	14	96	280	16.6	4.5
Supply Voltage (V)	0.6	1.2	1.6	1.8	1.8	1.2
Process(µm)	0.18	0.13	0.15	0.13	0.18	0.04
Area(mm^2)	-	-	1.02	0.02	0.0045	0.035
FOM(dB)	11	172.2	18.5	172	165.4	184

IV. CONCLUSION

Review of different *Sigma – Delta ADC's* in regard to low power, high SNDR applications are discussed in this paper. This paper brings an idea how sigma-delta ADC's are suitable in different biomedical applications

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