Design of 9-T QSTCAM using LECTOR Low Power Technique in 45nm CMOS Technology

S Aruna, K. Sravan, K.Srinivasa Naik

Abstract: ***Hardware search engine constitutes of an important role to enhance the speed of the process towards search of the high speed appliances. TCAM is that sort of a hardware which completes the search cycle in a single clock and it uses different mask storage and content storage. A 128*32 bit TCAM is implemented with selective match line evaluation scheme in predictive 45nm CMOS process and in this paper a TCAM is designed using LECTOR low power technique.***

Keywords— TCAM, LECTOR, 45nm CMOS process

I. INTRODUCTION

Depending on the response time of the data in the computer it distinguishes the memory into a order. Since feedback time, density, and quantity are interconnected, the phases may also be distinguished by its working and regulating technologies.

Memory order alters the performance in computer design, algorithm approximations and lower level of program writing units connecting the area of reference. Making the design for high-performances requires the knowledge of limitations in the order of memory, i.e. the abilities and range of each and every single type. Every type is seen as the fragment of the order of memories as shown if figure 1.1.

In which each member is lesser and quicker to forthcoming extreme member $M_{i+1}$with in the order. To lessen the making time for advanced levels, The reaction in lower stages will be by reacting to it in the way of complete loading a buffer and then transferring data by initiating the handover.

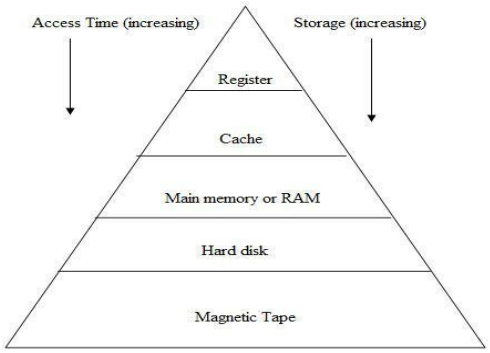

Figure 1.1: Order of memory diagram

Cache is designed for memory that is repeatedly utilised over and over again by the CPU. Rather than calling that for all times from the main memory, it is put in cache in order achieve high speed utilisation[2]-[4].Cache was altogether divided into C1, C2 &C3. C1 cache retrieving is done by not having any delay.C2 cache requires few additional clock cycles to retrieve compared to C1 cache.C3 cache requires few additional clock cycles to retrieve compared to C2 cache.

Main Memory is a hardware component and computer memory. Computer memory can be enhanced if the operating system used meets it requirements. Now a days PCs use 8GB of RAM. When compared to cache it reads slowly.

Internal register is designed for storing temporary results and variables. They have a very small storage they are easy to read. reading information as of the internal register will be the quickest means to utilise memory.

Hard disk is where data is saved forever it is a hardware unit where the memory is stored in a computer. Memory in hard disk is slower since it is not directly opened by the CPU. Comparing the RAM and hard disk, hard disk is cheaper per bit.Retrieval time for the memory is sluggish in Magnetic tape. Retrieving data from a tape takes very less time. Magnetic tape is generally used for storing big data.

In a PC the memory units RAM and CPU gives the addresses of the information put away in the Register which is utilized to query information from that memory area. If there should arise an occurrence of CAM, as the name recommends the memory is content addressable. Which means you don't have to give the memory address, rather the substance or a word in the memory to be looked. It is substantially quicker than RAM since it permits parallel inquiry, which turns out to be considerably quicker with the utilization of TLBs (Translation Look aside Buffers). Changes utilize CAM to store MAC Address Table

CAM is an uncommon sort of PC memory utilized in certain high speed applications. Or else this is called associative memory or associative array, despite the detail that the final stretch is more regularly operated for a programming. (It thinks about information seek information (tag) against a table of put away information, and returns the location of coordinating information or on account of acquainted memory, the coordinating information). A few convention PCs, similar to the Goodyear STARAN, are operated to execute CAM. Network Processing Forum created the Look Aside Interface (LA-1 and LA-1B) which is more prominent and trustworthy definition for the CAM later the network processing forum has joined hands with the OIF Further Various Gadgets Have been developed by many companies based on this understanding.

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CAM is intended to look through its whole memory as if solitary task, significantly quicker compared to RAM in essentially entire identifying tasks. Somewhere also cost detriments to CAM be that as it may. Not at all like RAM, said to be withholding straightforward capacity compartments, should every separate memory bit in a completely matching CAM essentially have its individual related correlation course for distinguishing a contest among put away piece to info bit. Also, coordinate yields on or after every phone information term must be joined to yield a total information term coordinate flag. Extra hardware determines the area of chip based on its density of the CAM chip which thus expands producing price, and in addition control dissemination since each examination circuit is dynamic by each bit cycle. Thus, CAM will just be utilized in specific interventions where seeking speed should not came for proficient utilizing a less expensive strategy

Conventional CAM can just match only (0 or 1). TCAM can coordinate dependent on 3 inputs, '0', '1' and 'X' where X indicates don't care state. Along these lines, you don't have to coordinate the correct location in, say, an ACL (Access Control List). TCAM passages have 3, in particular Value, Mask and Result (VMR). For instance, To coordinate an approaching bundle with an ACL, the switch coordinates the esteem and cover match and contrasts it and the outcome.

Information correspondences organize courses bundles of information by keeping up a look up table (LUT), where data in regards to the parcels goal is kept up. A reserve memory is utilized for capacity and quicker access (wire-speed get to). Customary direct mapped reserve, there is a likelihood To More store failure-rate because of some nonstop revivals inside store supervisor. Register and level 1 (L1) cache are quickest execution debases for the level 2 (L2) cache and the principle memory. The estimated L2 cache will be regularly used for getting to much of the time looked data. Traditional probing, Cache Controller gives location in every now and again sought information to the reserve memory, than the primary memory for quicker information get to.

A completely acquainted cache should be utilized by which area of fundamental memory is related with the store and issue of conflict for reserve areas can be fathomed, however it results in necessity of whole store label look (sequential). The product coordinate routine is slower regardless of utilizing quicker coordinating calculations. Thus, a content addressable memory (CAM) is regularly utilized instead of programming reserve tag frequently called as equipment store label which plays out the hunt in a solitary time cycle however at the expense of extra stockpiling territory. In contrast to an RAM, CAM provides quickened information seek by contrasting the pursuit information and prestored substance in a solitary clock cycle. Notwithstanding the essential CAM, a ternary CAM(TCAM) likewise as triple memory which utilizes an advantageous don't care (X). Based on inquiry activity, input is pre-fetched to match the record& synchronous correlation will be done along beforehand stacked information.

TerenaryCAM is an effective web index &reasonable in offbeat exchange state &quick querying the system steering [5]-[9]. Other than the quick looking, expansive number of capacity cells and interconnections involve considerable plan territory and making TCAM high on power utility. Hence, proficient low power procedures and high density packing method essentially be utilized for outlining TerenaryCAM. Algorithmic methodologies are actualized to diminish the TerenaryCAM query [10]-[11].

Dynamic plans have been displayed for high thickness stockpiling with low spillage necessities however an appropriate synchronization between information maintenance and invigorate cycle is excessively perplexing and builds the vitality dissipation [13]-[16]. NAND type circuit is apportioned in two sections by various limits work successively, bringing about lesser power utilization. In any case, the coordinating likelihood and outline of the pre-calculation hardware choose the power utilization as mentioned in the method above. Low control plans are anticipated dependent on Power decrease during max capacitive match lines [19]-[23]. ML plot is utilized in NAND &NOR. Interfacing rationale is utilized in the sections for keep away from short out current. The Voltage finder Currents are reused to energize ML in decreasing energy [21]. A productive high thickness store label is composed that plays out the Match line coordinate in close to no time.

The best handy solution for the talked about issue is a dynamic CAM (DCAM), yet information maintenance needs a legitimate harmonization in invigorate and hunt sequence for working.

The ill effects of this issue however don't effect the High-thickness of StaticCAMs (SCAMs) the power utilization is significant [24]. Interesting plans in the ordinary TCAMs have been completed to decrease the vitality dispersal. The Mask bits having just logic1 values have been isolated from those having just logic 0 value. Every single other cell aside from the limit cells various portions have been self gated. The non-fragmented models confront the test of high spillage control consumption [28],[29]. The portioned architecture settles it however cell total continues as before.

1.1. Memory Organization of CPU

Individual TCAM cells are associated in a composed cluster structure framing a prerequisite size of memory Block or Cache tag. Bigger memory state is required –in order attain the capacity to enormous measures of information.

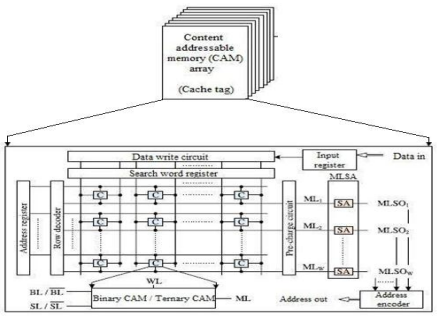

Figure 1.1.1: division of Memory in CAM

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The memory square is intended to reach compulsory size &length according to desired request. All the memory composes were clarified according to memory order it separates diverse kinds of memory in the phases to clarify obviously the reason and utilization of memory type the detailed division of memory in CAM is shown in above figure 1.1.1.

II. DESIGN OF CONVENTIONAL 9T-TCAM

The word ternary alludes to the quantity of information sources that the memory can store and inquiry: 0, 1 and X or trump card. Then again, secondly CAMs can just question utilizing 0s. Terenary substance addressable memory (TC is which that permits a third condition of don't care or then again "X" in at least one of the bits of put away information, adding adaptability to the inquiry.

TCAM which is considered inverse of RAM as it doesn't get to information similarly by giving a particular memory deliver to where the information is put away. The information put away by CAM must be gotten to by questioning the particular information that is required and it recovers the addresses where the questioned information is kept.

CAM is utilized for putting away and seeking on settled length information, which makes it ideal for putting away MAC addresses as they have a settled length. It is likewise quicker than RAM since it permits parallel looking. Normal CAM or double CAM can just hunt with 0s, yet ternary CAM includes a "X" to the blend so information does not have to coordinate precisely, adding to its adaptability. This makes it perfect for putting away Access Control Lists (ACL) in big business review switches and routers. Since, it tends to be looked by a more extensive field, as the inquiry turns out to be more adaptable. For instance, a whole scope of IP addresses can be sought at an occurrence, without contrasting all the substance one by one. This is valuable for expanding the speed of course query, route lookup, packet forwarding, packet order and ACL based directions.

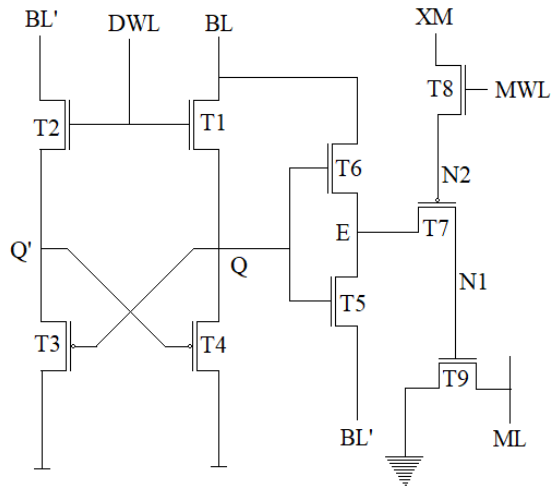

Figure 2.1: A 9Transistor TerenaryCAM

Outline of Semi static ternary content addressable memory utilizing the 9Transistors is appeared in the figure 2.1 and trailed by the clarification task. Reproduced outcomes, usefulness &Inter-connected schematics are shown

A coupled information and inquiry line (BL/BLB) has been given to the sources of transistors T5 and T6. Information word line (DWL) is utilized to compose information esteems (BL and BLB) utilizing transistors T1 and T2 and mask word line (MW L) is given for composing the mask (XM) by T8. The Dynamic mask approach is utilized for mask stockpiling net (N1) which was dangerous yet isolated MWL is initiated at a different time by not altering the capacity hub (Q& QB) values. MWL is initiated a tevery precharge stage so it guarantees a substantial masks in N1 and the search operation is controlled by the mask line drivers as stated in table I.

TABLE I: State Table For 9-Transistor TCAM

Proposed QSTCAM (this work)							Match state
XM	Q	BL	$\overline{BL}$	E	N_1	N_2	
0	0	0	1	L	0	L	Match
0	1	1	0	0	0	L	Match
0	0	1	0	1	0	1	Mismatch
0	1	0	1	H	0	H	Mismatch
1	X	X	X	X	1	0	Local match
0	X	0	0	L	0	L	Global match

III. MATCH LINE SENSE AMPLIFIER

The precharging circuit present in the MLSA charges the ML or else Capacitor in the process of correlation and after wards faculties the ML voltage drop to produce the result. The precharging activity is executed before correlation. This sort of MLSAs can without much of a stretch lessen the power utilization by restricting the voltage precharged in the precharging circuit. Be that as it may, the precharging configuration has experienced the charge-sharing impact among CAM cells.

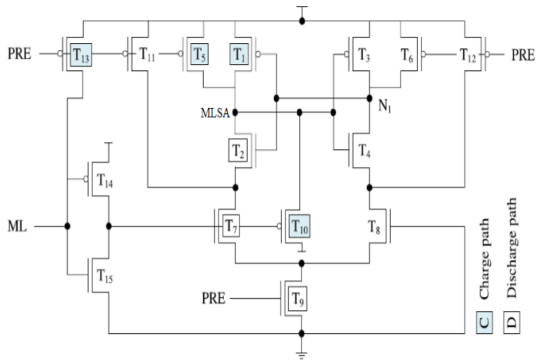

Figure 3.1: charge-up Match line sense amplifier.

PRE – Precharge signal
ML – Match line
MLSO – Match line Sense output

The above amplifier in the figure is taken to sense TerenaryCAM. Traditional detecting, ML will gets charged up to VDD at first later full column coordinate releases match line to earth. MLSO is charged up to VDD amid precharge stage by T3 &T5. ML has been precharged at the same time through T13 to give a low contribution at T7 and T10. Transistors T11 and T12 are utilized for decreasing

immediate release in Match Line SO amid stage alters by precharge to search. Amid hunt if a confuse happens, MLSO releases to earth by way T2 – T7 – T9

At the point when a match happens, T10 gives an additional charge way to the yield consequently obstructing its release because of feeble N1.

The amount of release of MLSO amid to stage alteration from precharge to look very influential to the dynamic power utilization because of the swift releasing and increasing current. T2 and T3 constructs solid (0)at the output of MLSO amid mistake state during which solid T10 and powerless T1 by which N1 holds the MLSO charge in a same state. T8 stayed at cut-off constantly however it is critical for giving disconnection between transistors T9 and T12.

XM	Q	BL	BLB	E	N1	N2	Match State
0	0	0	1	L	0	L	Match
0	1	1	0	0	0	L	Match
0	0	1	0	1	0	1	Mismatch
0	1	0	1	H	0	H	Mismatch
1	X	X	X	X	1	0	Local match
0	X	0	0	L	0	L	Global match

Table II: State Table Comparison Of TCAM Architecture

The separation is vital for taking the precharge MLSO when precharge state and stage alteration among precharge &seek. The Proposed detecting plan is extremely valuable in High density TCAMs where the match line control Transistors were determined with frail signals. The match and mismatch state conditions are mentioned in above Table II.

IV. PROPOSED TCAM WITH A LOW POWER TECHNIQUE

A 9 – Transistor QSTCAM circuit which is observed before has been adjusted to decrease the power utilization where extra transistors are associated with the gate& source pins T1, T2, T3 &T4 to get the Vgs = 0 during the estimations as IN = 0 & INB = 1.

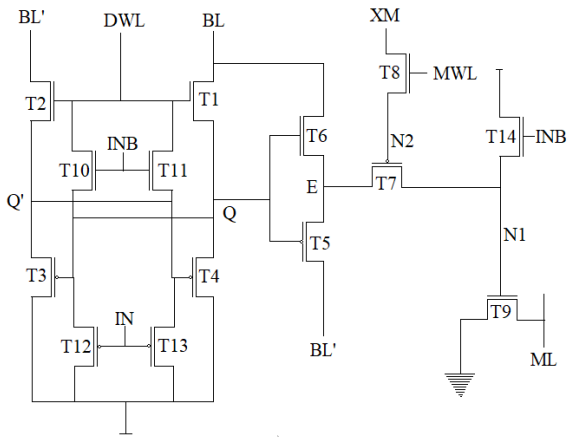

Figure 4.1: Proposed TCAM circuit to obtain low power consumption

Search line (BL/BLB) is connected to T5 &T6 sources. The data word line(DWL) is utilized for composing information esteems (BL and BLB) utilizing transistors T1 and T2 and veil word line (MWL) has been given the task to mask (XM) through transistor T8 as shown below in the figure 4.1.

The power utilization in this circuit is less when contrasted with the current 9 – Transistor TCAM cell.

For IN = 1 and INB = 0 the TCAM cell works according to the predesigned functionality (the PMOS switches are in cut off region for Vgs > Vth and NMOS switches are in cut off region for Vgs < Vth) and works in normal mode.

At the point when IN = 0 and INB = 1 the TCAM cell will be in off state (as Vgs = 0 for the values).

XM	IN	INB	Q	BL	BLB	E	N1	N2	Match State
0	1	0	0	0	1	L	0	L	Match
0	1	0	1	1	0	0	0	L	Match
0	1	0	0	1	0	1	0	1	Mismatch
0	1	0	1	0	1	H	0	H	Mismatch
0	1	0	X	X	X	X	1	0	Global match
1	1	0	X	X	X	X	1	0	Local match
0	1	0	X	0	0	L	0	L	Global match
0	0	1	X	X	X	X	X	X	Global mismatch
1	0	1	X	X	X	X	X	X	Local mismatch
1	1	0	X	X	X	X	X	X	Local match

Table – III: State Table Comparison Of Proposed TCAM Architecture

Finally, the required signal isn't going outward and TCAM cell will be OFF with the goal that the power utilization will be lessened as the perfect TCAM cells will be in OFF state. Subsequently, the Match State shifts according to the indicated values from table – III

V. RESULTS AND PERFORMANCE ANALYSIS

5.1. SCHEMATICS

9Transistor Conventional TCAM

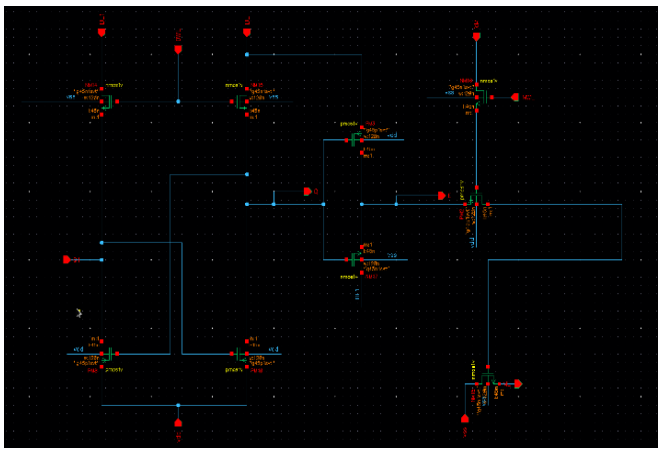

Figure 5.1.1: Schematic for 9Transistor Conventional TCAM

Match Line Sense Amplifier (MLSA)

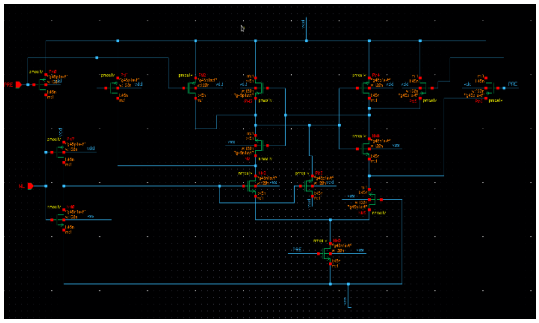

Figure 5.1.2: Schematic for Match Line Sense Amplifier(MLSA)

PROPOSED Low Power TCAM

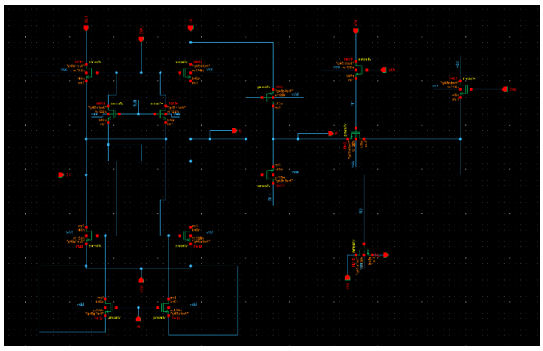

Figure 5.1.3: Schematic for PROPOSED Low Power TCAM

5.2. Output Waveforms

9Transistor Conventional TCAM

Figure 5.2.1: Output Waveforms for 9Transistor Conventional TCAM

PROPOSED Low Power TCAM

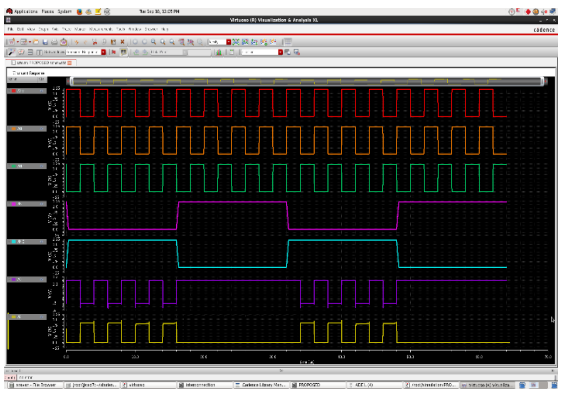

Figure 5.2.2: Output Waveforms for PROPOSED Low Power TCAM

5.3. LAYOUTS

9Transistor Conventional TCAM

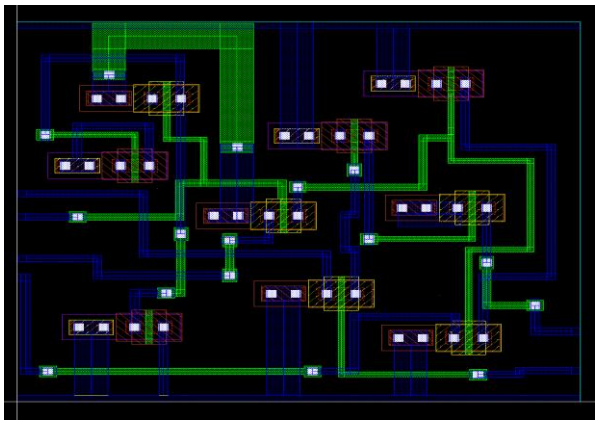

Figure 5.3.1: LAYOUTS for 9Transistor Conventional TCAM

PROPOSED Low Power TCAM

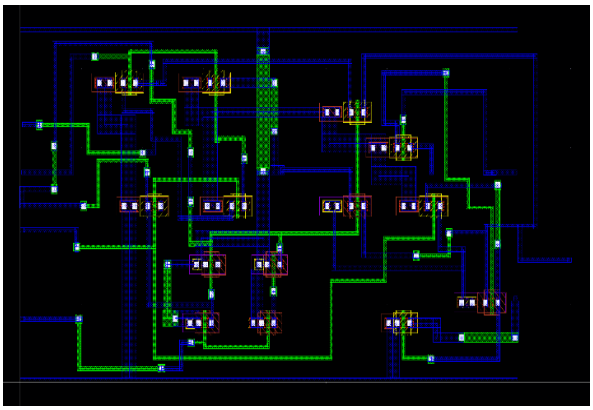

Figure 5.3.2:LAYOUTS for PROPOSED Low Power TCAM

Match Line Sense Amplifier(MLSA)

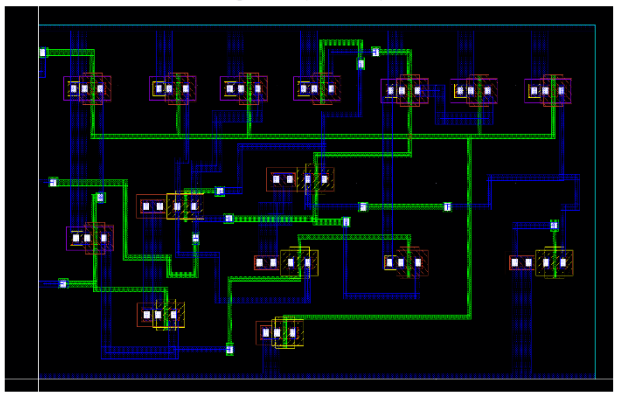

Figure 5.3.3:LAYOUTS for Match Line Sense Amplifier (MLSA)

Table – IV:

The GPDK Representing the Threshold Voltages [V] At Various Corners for Predictive Models

Model		FF	FS	SF	SS	TT
45nm	nMOS	0.26	0.31	0.41	0.46	0.36
45nm	pMOS	-0.31	-0.45	-0.36	-0.49	-0.4

Table – V:

The GPDK Representing the Device Sizes [Nm] for Predictive Models

Device size	45nm	90nm	180nm
Channel width	120	210	420
Channel length	45	90	180

Table – VI: RESULTS COMPARISION TABLE

Parameters	9-T TCAM	Proposed TCAM
Average power(μW)	146.37	69.32
Time delay(ps)	17.35	24.3
Energy(fJ)	2.5395	1.6841

VI. CONCLUSION

This paper has proposed a 9 -Transistor Ternary CAM is designed and its output wave forms are observed and an MLSA circuit is designed and implemented TCAM and MLSA are interconnected and output is observed. A TCAM Circuit is implemented using a low power LECTOR and the output is observed that there is an reduction in the energy consumption by 42% of the original energy consumption of the conventional TCAM has been achieved over the compared architectures. The proposed TCAM can be used in applications with low-power and high-density storage requirements

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