Finfet Based Two Stage Dynamic Comparators for Low Power High Speed Adcs

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ABSTRACT – This paper proposes two stage dynamic comparators. These are designed for high speed low power ADC's. Comparator is a device which compares the two input signals and provides differential outputs. It is used in the devices which measure and digitize the analog signals i.e., ADCs, Zero crossing detectors, relaxation oscillators and level shifters. These are used in front end designs of biomedical, digital imaging, communication and digital signal processing applications. In the proposed designs, dynamic latch circuit is used to reduce the area and delay because dynamic logic circuits require less area with high speed than the static designs. Depending on the clock signal, the dynamic latch is evaluated in pre-charge and evaluation phases. The proposed designs have been simulated in Cadence using 180 nm CMOS and 18 nm FINFET technologies. These designs offer low power with high speed and better PDP.

Index terms - Dynamic comparator, ADC, dynamic latch, CMOS technology, FINFET technology, PDP.

1. INTRODUCTION

Comparator is used to compare two input signals and produce differential outputs. Comparator consists of pre-amplifier and a latch circuit which operates based on clock signals. It is operated in two phases i.e., reset phase and latch phase. Comparators are used in window detectors, level shifters, absolute value detectors, ADC's. It is one of the important block whose parameters define performance of the ADC. Analog to digital converter is used to convert the analog input to digital data for noise & error reduction and long distance transmission. ADC's are used to process, store the analog signal in digital form and digitizing the pixels. ADC's are used in front end designs of bio-medical, RF & microwave, DSP applications. In this paper, dynamic comparators are proposed. These circuits benefit from low power, high speed and better PDP when compared with the existing designs. This paper consists of three sections i.e., existing designs, Proposed Designs, Simulation results and summary.

2. EXISTING DESIGNS

The conventional two stage dynamic comparator [1] is shown in Figure 1. It contains two stages i.e., pre-amplifier and latch. The clk1 and clk2 are the two inverting clock signals. Vn and Vp are output nodes for the first stage. The Voutp and Voutn are the outputs for the design. If clk1 is high, clk2 is low then the transistors M1 is turned OFF and M4, M5 M6, and M11 are turned ON. The output nodes Vn and Vp are pulled down to zero and Voutp and Voutn are charges to Vdd. If clk1 is low and clk2 is high then the M1 is turned ON. If Vinp > Vinn then M3 is turned ON. The node Vp is charged up to Vdd which turns on the transistor M12 then the output Voutn is pulled down to zero and Voutp equals to Vdd. If Vinn > Vinp then M2 is turned ON. The node Vn is charged to Vdd which turns on the transistor M8 then the output Voutp is pulled down to zero and Voutn equals to Vdd.

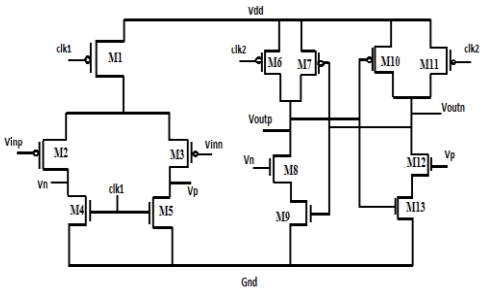

Figure 1: Conventional two stage CMOS dynamic comparator

The energy-efficient two-stage dynamic comparator [2] is shown in Figure 2. In this comparator, the inputs are given to the nMOS transistors instead of pMOS transistors in the pre-amplifier stage. In the latch, NOR gates are used instead of NAND gates [1] to reduce the power drawn by the comparator**.**

If clk1 is low, clk2 is high then the transistors M5 is turned OFF and M1, M2, M8 and M13 are turned ON. The output nodes Vn and Vp are charged to Vdd and Voutp and Voutn are pulled down to Ground.

If clk1 is high and clk2 is low then the transistors M1, M2 will be turned OFF and M5 will be turned ON. If Vinp > Vinn then M3 is turned ON. The node Vn is pulled down to zero which turns on the transistor M7 then the output Voutp is pulled up to Vdd and Voutn equals to zero.

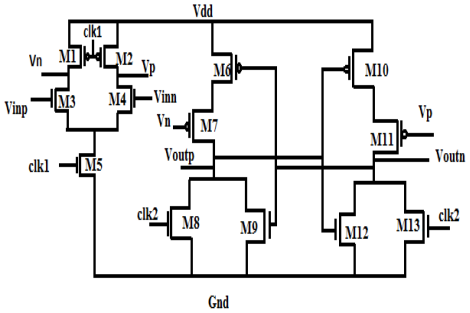

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Figure 2: Energy efficient two stage CMOS dynamic comparator

If Vinn > Vinp then M4 is turned ON. The node Vp is pulled down to zero which turns on the transistor M11 then the output Voutn is pulled up to zero and Voutp equals to zero. This design is better than two stage conventional dynamic comparator in terms of power, but the delay is increased.

3. PROPOSED DESIGNS

The Proposed dynamic comparator 1 is shown in Figure 3. In this design, the NOR based latch is placed instead NAND based latch in conventional two stage dynamic comparator (Figure 1). when clk1 is high, it enters into reset phase which turns ON the transistors M4, M5 and M1 is turned OFF then the output nodes Vn, Vp, Voutp, Voutn are pulled down to zero.

When clk1 is low, it enters into latch phase which turns ON the transistor M1. If Vinp > Vinn, then the transistor M4 is turned ON and the output node Vp is charged to Vdd, Vn equals to Zero which turns on the transistor M6 and Voutp is pulled up to Vdd.

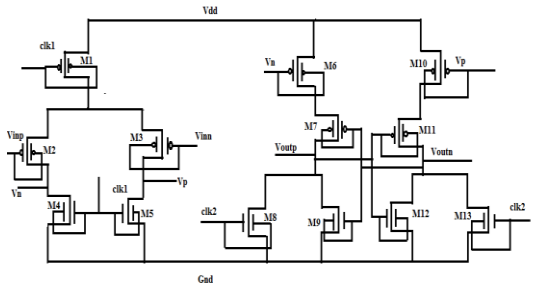

Figure 3: Proposed FINFET dynamic comparator-1

If Vinn > Vinp, then the transistor M3 is turned ON and the output node Vn is charged to Vdd, Vp equals to Zero which turns on the transistor M10 and Voutn is pulled up to Vdd, Voutp pulled down to Zero.

To reduce the transistor count, power and delay, the latch is replaced with dynamic latch in the energy efficient two stage dynamic comparator is shown in Figure 2. The Proposed dynamic comparator 2 is shown in Figure 4. It consists of pre-amplifier and dynamic latch with NAND logic.

To increase the speed of the Figure 3, the pMOS transistors are replaced with nMOS transistors in both pre-amplifier and latch stages. If clk1 is low, clk2 is high then the outputs Vn, Vp charges to Vdd and depends on the feedback path the outputs Voutp, Voutn are either pulled to Vdd or Ground.

If clk1 is high, clk2 is low then it enters into latch phase and which turns on the transistor M5.

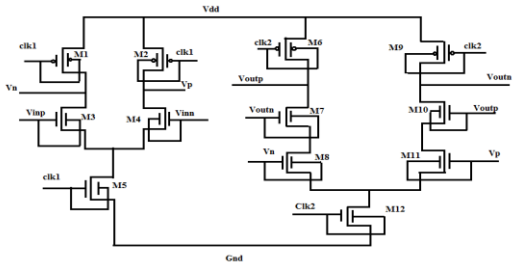

Figure 4: Proposed FINFET dynamic comparator-2

If Vinp > Vinn, then the output node Vn is pulled down to zero which changes the outputs Voutn to 0, Voutp to Vdd. If Vinn > Vinp, then the output node Vp is pulled down to zero which changes the outputs Voutp to 0, Voutn to Vdd.

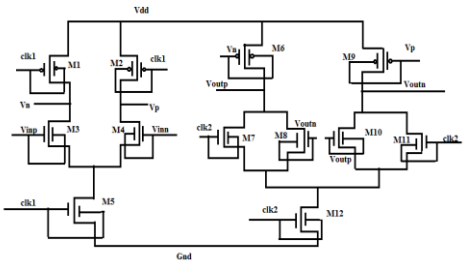

Figure 5: Proposed FINFET dynamic comparator-3

The Proposed dynamic comparator 3 is shown in Figure 5. It consists of pre-amplifier and dynamic latch with NOR logic to enhance the speed and power. If clk1 is low, clk2 is high then the outputs Vn, Vp charges to Vdd and the outputs Voutp, Voutn are discharged to Ground.

If clk1 is high, clk2 is low then it enters into latch phase. If Vinp > Vinn, then the output node Vn is pulled down to zero and the Voutp is charged to Vdd. If Vinn > Vinp, then the output node Vp is pulled down to zero and Voutn is charged to Vdd, Voutp is pulled down to zero. The power and delay are less for the proposed dynamic comparator 3 by comparing with the existing and proposed designs.

4. SIMULATION RESULTS

The results are simulated in Cadence using 180 nm CMOS and 18 nm FINFET technologies. The transient responses for dynamic comparators are shown in Figure 6 - 10. The response of dynamic comparators are analyzed at 1.8 V power supply for CMOS technology and 0.2 V supply voltage for FINFET technology at 10 MHz Frequency.

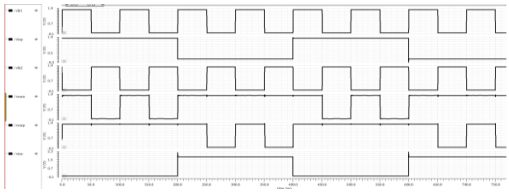

Figure 6: Transient response of conventional two stage dynamic comparator

The power and delay are less for the proposed designs by comparing with existing designs. The comparison is tabulated in Table.1 & 2. In latch circuit, NOR gates are used instead of NAND gates to reduce the unnecessary power drawn in reset phase and to increase the speed.

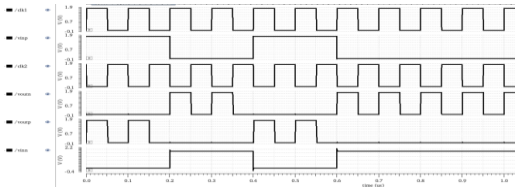

Figure 7: Transient response of energy efficient two stage dynamic comparator

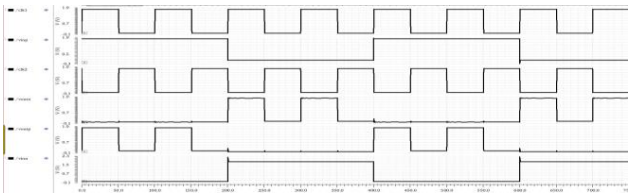

Figure 8: Transient response of proposed dynamic comparator 1

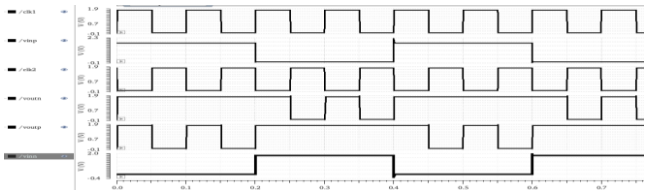

Figure 9: Transient response of proposed dynamic comparator 2

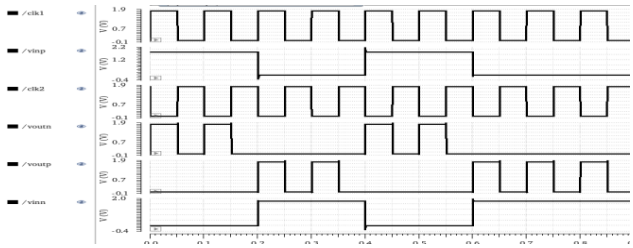

Figure 10: Transient response of proposed dynamic comparator 3

To avoid redundancy, only CMOS based results are shown in Figure 6 to Figure10 for the circuits Figure 1 to Figure 5 respectively. Table.1 shows that the proposed designs are better than the existing designs for CMOS technology. Table 2 shows that FINFET based designs are better than CMOS designs and these have less power, less delay and better PDP than the CMOS circuits.

Table 1: Performance Summary of Dynamic Comparators using CMOS

Parameter		Power (n W)	Delay (p s)	PDP * 10^{-21}
[1]		425.38	530.42	255630.1
[2]		12.84	699.52	8981.8
This work	1	62.98	509.05	32059.9
	2	13.45	460.58	6194.8
	3	13.45	437.67	5886.6

Table 2: Performance Summary of Dynamic Comparators using FINFET

Parameter		Power (p W)	Delay(s)	PDP * 10^{-21}
[1]		286.998	1.978 n	567.99
[2]		733.313	2.891 n	2853.3
This work	1	770.207	834.75 p	642.93
	2	93.005	522.21 p	48.568
	3	143.58	359.42 p	51.606

5. CONCLUSION

The two stage dynamic comparators are proposed for the high speed, low power ADCs in this paper. The proposed dynamic comparators offer low power, high speed and better PDP. The Performance of these comparators shows that dynamic NOR Based latch is preferable compared to the dynamic NAND based latch and dynamic NOR based latch is better than the static NOR based latch because the power and delay are less. These designs are suitable for front end designs of biomedical, DSP, Communication applications.

REFERENCES

[1] *Tzu-Yun Wang, Hao-Yu Li, Zong-Yu Ma, Yang-Jing Huang and Sheng-Yu Peng*, "A bypass - switching SAR ADC with a dynamic proximity comparator for biomedical applications," IEEE Journal of Solid-State Circuits, Jun. 2018, Vol. 53, no. 6, pp. 1743 – 1754.

[2] *M. V. Elzakker, E. V. Tujil, P. Geraedts, D. Schinkel, E. A. M. Klumerink and B. Nauta*, " A 10- bit charge- redistribution ADC consuming 1.9 µW at MS/s," IEEE Journal of Solid-State Circuits, May 2010, Vol. 45, no. 5, pp. 1007-1015.

[3] *P. Harpe, E. Cantatore and A. Van Roermund*, "A 10b/12b 40KS/s SAR ADC with data-driven noise reduction achieving up to 0.1b ENOB at 2.2 fJ/conversion step," IEEE Journal of Solid-State Circuits, Dec. 2013, Vol. 48, no. 12, pp. 3011-3018.

[4] *F. M. Yaul and A. P. Chandrakasan*," A 10 bit SAR ADC with data dependent energy reduction using LSB-first successive approximation," IEEE Journal of Solid-State Circuits, Dec. 2014, Vol. 49, no.12, pp. 2825-2834.

[5] *H. Tang, Z. C. Sun, K. W. R. Chew, and L. Siek*," A 1.33 µW 8.02 ENOB 100 Ks/s successive approximation ADC with supply reduction technique for implantable retinal prosthesis," IEEE Transactions Biomedical Circuits Systems, Dec. 2014, Vol. 8, no. 6, pp. 844-856.

[6] *G. Y. Huang, S. J. Chang, C. C. Liu, and Y. Z. Lin*, "A 1-µW 10-bit 200-kS/s SAR ADC with a bypass window for biomedical applications," IEEE Journal of Solid–State Circuits, Nov. 2012, Vol. 47, no. 11, pp. 2783–2795.

[7] *M. Yip and A. P. Chandrakasan*, "A resolution-reconfigurable 5-to-10-bit 0.4-to-1 V power scalable SAR ADC for sensor applications", IEEE Journal of Solid-State Circuits, Jun. 2013, Vol. 48, no. 6, pp. 1453–1464.

[8] *Z. Zhu and Y. Liang*, "A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-µm CMOS for medical implant devices", IEEE Transactions of Circuits Systems I, Fundamental Theory Applications, Sep. 2015, Vol. 62, no. 9, pp. 2167–2176.

[9] *Y. Tao and Y. Lian*, "A 0.8-V, 1-MS/s, 10-bit SAR ADC for multichannel neural recording," IEEE Transactions of Circuits Systems I, Regular Papers, Feb. 2015, Vol. 62, no. 2, pp. 366–375.

[10] *D. Zhang, A. Bhide, and A. Alvandpour*, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-µm CMOS for medical implant devices," IEEE Journal of Solid–State Circuits, Jul. 2012, Vol. 47, no. 7, pp. 1585–1593.

[11] *D. Gangopadhyay, E. G. Allstot, A. M. R. Dixon, K. Natarajan, S. Gupta, and D. J. Allstot*, "Compressed sensing analog front-end for bio-sensor applications," IEEE Journal of Solid-State Circuits, Feb. 2014, Vol. 49, no. 2, pp. 426–438.

[12] *H. Lee, S. Park, C. Lim, and C. Kim*, "A 100-nW 9.1-ENOB 20-kS/s SAR ADC for Portable Pulse Oximeter," IEEE Trans. Circuits Syst. II, Exp. Briefs, Apr. 2015, Vol. 62, no. 4, pp. 357–361.

[13] *C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin*, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," IEEE J. Solid-State Circuits, Apr. 2010, Vol. 45, no. 4, pp. 731–740.

[14] *H. Y. Tai, Y. S. Hu, H. W. Chen, and H. S. Chen*, "A 0.85 fJ/conversion step 10b 200 kS/s sub-ranging SAR ADC in 40 nm CMOS," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2014, pp. 196–198.

[15] *S. Liu, Y. Shen, and Z. Zhu*, "A 12-bit 10 MS/s SAR ADC with high linearity and energy-efficient switching," IEEE Trans. Circuits Syst. I, Reg. Papers, Oct. 2016, Vol. 63, no. 10, pp. 1616–1627.

[16] *Y. Song, Z. Xue, Y. Xie, L. Geng, and S. Fan*, "A 0.6-V 10-bit 200-kS/s fully differential SAR ADC with incremental converting algorithm for energy efficient applications," IEEE Trans. Circuits Syst. I, Reg. Papers, Apr. 2016, Vol. 63, no. 4, pp. 449–458.

[17] *A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro*, "A 0.5 V 1.1 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," IEEE J. Solid-State Circuits, Apr. 2012, Vol. 47, no. 4, pp. 1022–1030.

[18] *Z. Zhu, Z. Qiu, M. Liu, and R. Ding*, "A 6 to 10-Bit 0.5 V to 0.9 V reconfigurable 2 MS/s power scalable SAR ADC in 0.18 μm CMOS," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., Mar. 2015, Vol. 62, no. 3, pp. 689–696.