A Double Tail Dynamic Latched Comparator for Pipelined ADC

K. Lokesh Krishna, A. Krishna Mohan, Yahya Mohammed Ali Al-Naamani

Abstract*— Data converter circuits are very essential circuit blocks in the implementation of low power and moderate speed electronic systems. In recent years, with more and more portable electronic systems being designed, developed and available in the market, it becomes essential to include more features in these systems. One of the main blocks in these systems is analog to digital converter, which uses a comparator inside it. With the purpose of improving the functionality of ADC circuit, a complete design and simulation. The comparators use regenerative feedback to convert the output to a full scale digital signal. The main parameters considered are power dissipation, gain, propagation delay, offset voltage and slew rate. The simulation is carried out in CMOS 90nm technology using spectre of cadence EDA tool. The simulation results permit the analog circuit designer to completely explore the tradeoffs such as operating speed and power consumption for flash ADC architecture. The power dissipation of the designed comparator circuit is 136µW, when operated at supply voltage of 1.2V and delay is simulated to be 526ps. The simulated results show that it can be used for a pipelined ADC architecture.

Keywords*— CMOS; low offset; low power; mixed signal circuit and slew rate.

I. INTRODUCTION

Recent progresses in execution of integrated circuit systems have directed in the advancement of several novel cordless portable practices that are electronic to produce at an fashion this is certainly unmatched. The use of wireless programs which are lightweight is more prevalent inside our tasks that are day-to-day. The main specifications include such as longer battery operating time, high speed, moderate resolution levels, less noise, a reduced amount of silicon area and low power. In order to design such wireless portable systems, a data converter circuit Analog to Digital Converter (ADC) circuit is very much indispensable. These ADCs are desired circuits to interface the analog to digital domains and vice versa. Several design such as Sigma-Delta (Σ-Δ) type, Folding type, Flash circuit, Two-Step flash, Subranging based, Pipelined, Dual-slope circuit, Successive approximation register type and Time-interleaved are available in the literature to perform analog to digital conversion. In general for Software defined radio and data acquisition systems; Pipelined architecture is preferred to other ADC architectures.

Pipelined architectures can be operated at supply voltages just under or just larger than 1V, have potential for low power consumption, and are easily standardized to obtain a higher level of resolution, and can be fabricated with CMOS or bipolar processes. Comparator circuits are the crucial circuits in the operating design of pipelined ADC architecture. The architecture of comparator circuit plays a major role in ADC design and moreover it influences the performance of whole portable system in a direct manner. The important specifications considered in the design of comparator circuit are input voltage range, resolution, power consumption, conversion rate and area

A comparator circuit in its form that is simplest consists of a usual MOS transistor linked in differential pair configuration with a NMOS or PMOS current mirror circuit as an active load, a typical source amplifier stage and one or more CMOS based inverter circuits which then act as an extra amplification phase. The performance of a CMOS comparator circuit such as for instance propagation wait, energy consumption, speed and occupied area that is silicon be improved by scaling the dimensions of MOS transistors. However, the scaling technique of CMOS transistors are not realized directly, as it necessitates. Reducing dimensions i.e. (W/L) ratio of the MOS transistor leads to degradation of several important specifications of the comparator circuit. Also it accounts for the increased offset voltage and major changes in the (1/f) noise levels. One of technique to lessen the power consumption of a CMOS transistor circuit is to use power supply voltage reduction technique. The power relation in a CMOS circuit is proportional to the square of V_{DD}. However, reducing the power supply voltage will severely increase the delay time. Also to compensate for the reduction in power supply voltages, transistor sizes are further increased and this would cause increased power consumption and large silicon area.

A comparator circuit of known amplitude and produces a logical stage output, which specifies whether at a discrete point of time. Type of analog to digital converter for a particular application. The block diagram of a high-speed comparator circuit is shown in fig. 1. It comprises of namely the preamplifier circuit, the decision circuit and lastly an output buffer circuit [6]. The preamplifier circuit basically consists of a differential circuit pair connected using NMOS with PMOS active load. The size of the input MOS differential transistor pair is chosen in accordance with the transconductance (g_m) and input impedance of the NMOS differential pair. The operating voltage gain of the preamplifier circuit can be enhanced further by resizing the widths of PMOS transistors at the output side. The next stage is a decision circuit and it should be able to discriminate very low amplitude signals of the range (µV to few mV). By introducing hysteresis in the circuit, the circuit

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is able to discriminate noisy outputs. Also positive feedback is employed in decision circuit which is achieved by cross coupling of two NMOS transistors. The output stage is an output buffer circuit. This stage is employed to produce an output logic signal (either high or low). The output buffer circuit must receive a differential signal at its input side and must not suffer from high operating speed limitations.

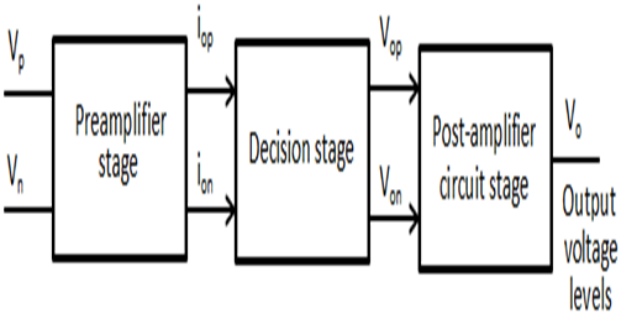

Fig. 1: Block diagram of comparator circuit

G.Sun et al. proposed a threshold control design technique for optimizing area and power efficiency of a CMOS comparator design [1]. A comparator with reduced kickback noise which results in overall power reduction by 50% is described in [2]. Krishna.K.L. et al. presents a differential amplifier-based CMOS comparator operating at 180nm technology with high resolution [3]. E.Shirai et al. presents the design of multistage preamplifiers for use in high speed comparators [4]. L. Kouhalvandi et al. describes a comparator circuit with offset voltage cancellation technique, which results in reduced kick-back noise [5]. A preamplifier less based CMOS comparator circuit is presented in [7]. The created comparator operates at 5.1GS/s. The double tail dynamic latched comparator is simulated in 90nm CMOS technology and finally contrast table is presented highlighting its important specifications accomplished in this proposed work.

This presented work is planned as follows: the block diagram of n-bit pipelined ADC architecture is discussed in Section-II, while the working design of the proposed double tail dynamic latch circuit is shown in Section-III. Section-IV shows the simulated results of the comparator circuit and Section-V gives the conclusions.

II. PIPELINED ADC ARCHITECTURE

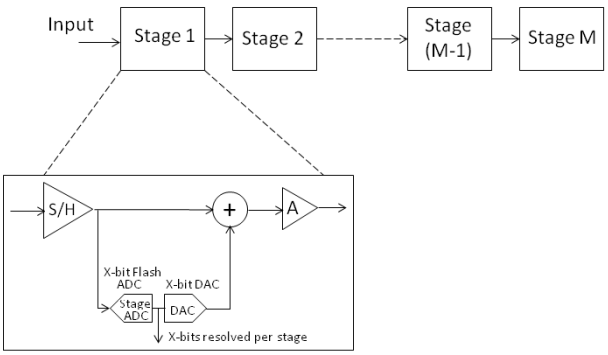

Fig. 2: n-bit pipelined ADC architecture

A pipelined architecture comprises of a series of identical stages and digital error correction logic implemented using combinational circuits and a bit aligner stage that produces the final digital output bits. Each sub-converter stage of a pipeline ADC consists of n-bit flash architecture that is used to transform directly the inward input signal; an n-bit DAC circuit, continuous signal, and an amplifier to amplify the signal to a desired value and sent to the next stage as shown in fig. 2. Here all the stages function simultaneously, i.e., when the first stage functions sample [9]. At last, digital latch circuits are used to synchronize the output signals from the different stages of the converter architecture.

III. IMPLEMENTATION OF DOUBLE TAIL DYNAMIC LATCH COMPARATOR ROUTE

The most utilized used for converting the given continuous input signals to output digital logic. When the comparator circuit calculates the exact difference between two input signal voltages, simultaneously an internal offset voltage (V_{io}) is added to the voltage difference [8]. Consequently, when the two input voltages are near to each other, then the comparator may produce an unstable output and incorrect output code is generated. Thus, the design of comparator circuit is critical in the design electronic systems. The speed of the entire portable electronic system is dependent on the proper dimensional design of a transistor in a CMOS comparator circuit. In this section architecture designed, explained, taking into account the important specifications such as power dissipation, resolution, conversion rate, die size, slew rate and input voltage range.

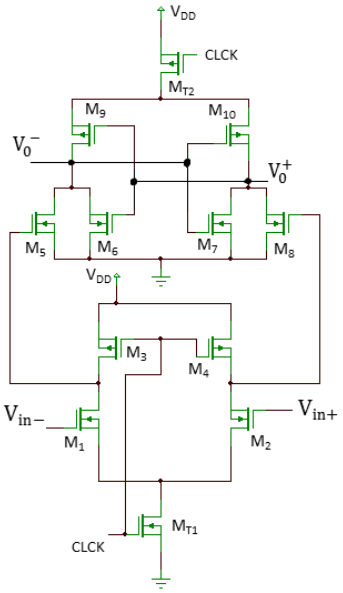

Fig. 3: Schematic diagram of double tail dynamic latch circuit

The end that is double latched comparator circuit shown in fig. 3, consists of two stages with two tail that is present. The stage that is first a tiny tail current to realize low offset voltage, whereas the second phase has a large tail current to establish extremely smaller delay time. If the clock signal are at low level (i.e. reset phase), the transistors MT1 and MT2 are deterred, make sure that there's absolutely no power that is static in this period. However, during the time

that is same the transistors M3 and M4 are switched on and pulling the source terminals of M3 and M4 to supply voltage VDD. Hence the transistors M5 and M8 are turned on and the voltages and are reset to ground. Whenever clock sign is at high level (i.e. set phase), the transistors M3 and M4 are deterred. The source nodes of transistors M3 and M4 will discharge at different rate, that will be proportional to their corresponding input voltages applied at transistors M1 and M2. When any one of the outputs of the stage that is first below the threshold voltages of M5 and M8, then the transistors of M5 and M8 are switched down. The feedback that is positive in the circuit functions, pushing among the production voltages to VDD and the other output terminal voltage to zero voltage.

IV. RESULTS & SUMMARY

A comparator structure tail that is particularly dual latch comparator circuit is designed and simulated in CMOS 90nm technology utilizing spectre of cadence EDA. The simulated response that is transient of latch comparator circuit is presented in fig. 4, correspondingly. The running supply voltage is set at 1.2V. The parameters such as offset voltage, propagation delay, running speed, energy consumption and slew price had been calculated using analysis that is transient. The power that is static for the comparators is calculated mathematically by the product of bias currents in the circuit and the used supply voltage VDD. The calculation of dynamic energy dissipation is based on the currents flowing through the transistors, when they are switched between off and on states and vice-versa.

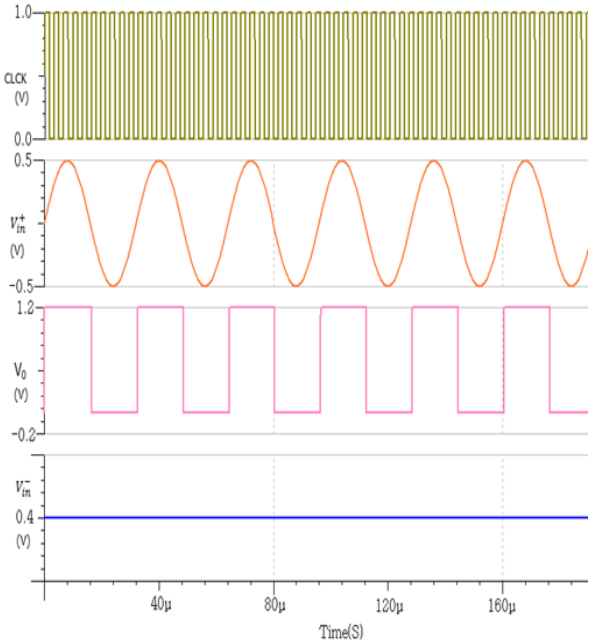

Fig. 4: Simulated transient response

The simulated offset voltage waveform is presented in fig. 5, and offset voltage is measured to be 7.34mV.

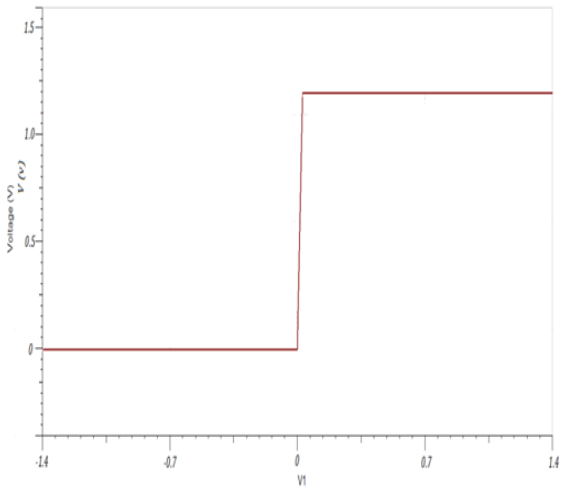

Fig. 5: Simulated offset voltage response

Fig. 6, shows the simulated response of propagation delay versus V_{DD} for various values of offset voltages. (for V_{id}=10mV, 20mV and 30mV)

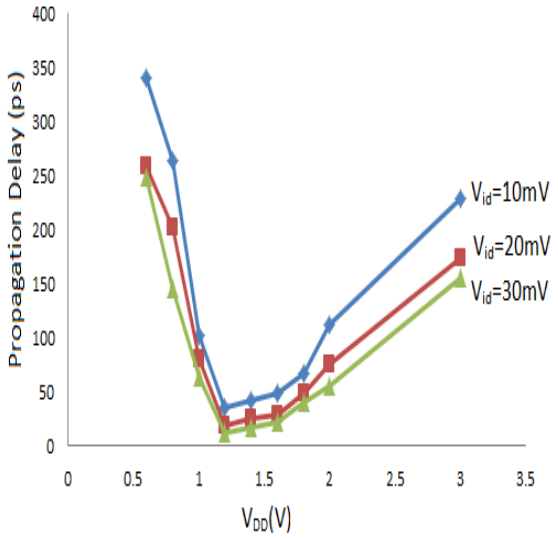

Fig. 6: Simulated curves for propagation delay

Table 1, shows the end result summary of the double tail latch comparator circuit that is dynamic. The specifications considered in this work are offset voltage, energy dissipation, occupied area, gain, propagation wait and slew rate. The proposed comparator circuit architecture exhibits higher speed that is operating low power consumption and less offset voltage in comparison with the previous architectures.

Table 1: Summary of comparator circuit

S.No	Parameter	Value
1	Offset voltage (mV)	7.34
2	Power dissipation (µW)	136
3	Gain (dB)	57
4	Propagation delay (ps)	526

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5	Speed (Hz)	1.9G
6	Power Delay product(fJ)	71.536
7	Area (μm^2)	162

V. CONCLUSION

The design and simulation of a speed that is high low offset double tail dynamic latch comparator circuit to be used in a pipelined ADC architecture is presented in this paper. The proposed design exhibits less power consumption, high speed and occupies less area because for the non-presence of preamplifier circuit stage. The comparator circuit is simulated spectre that is utilizing of EDA tool in 90nmCMOS technology, uses a power of 136µW when powered from a 1.2V voltage. It also exhibits a wait and offset voltage of 526ps and 7.34mV respectively. The obtained parameter values of double tail dynamic comparator that is latched it favorable for use in pipelined ADC where speed and energy are of utmost importance.

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