Design of 1-V, 12-Bit Low Power Incremental Delta Sigma ADC for CMOS Image Sensor Applications

D.S. Shylu Sam, S. Radha, D. Jackuline Moni, P. Sam Paul, J. Jecintha

Abstract--- This work describes a 12-bit low power incremental delta sigma analog to digital converter (ADC) suitable for CMOS image sensor applications. The resolution of the delta sigma ADC is improved by sharing an op-amp between two stages of the modulators. Op-amp is the main building block of delta sigma ADC and the power consumption is reduced by self-biasing amplifier. The prime conversion is done by using comparator. The 12-bit incremental delta sigma ADC is designed in 90nm CMOS process. Simulation result shows that the power consumption for 12-bit incremental delta sigma ADC is 0.001mW.

Keywords--- Delta-sigma ADC, op-amp sharing, self-biased amplifier, low power, comparator.

I. INTRODUCTION

In recent trends the importance of CMOS image sensors because of its low power, low cost and high resolution has been increased[1]-[3].These sensors can be used in many devices like mp3, digital cameras, etc. These applications require low power and small area ADC with 12-bit resolution [4]-[7]. Two step incremental sigma delta ADC with fully floating double sampling integrator which results in less number of clock cycles. However, the power consumption of this technique is very high [8]. Moreover, biasing thousands of operating transconduction amplifier is not an insignificant task [9]-[10]. Fig.1 shows the architecture of incremental sigma delta ADC.

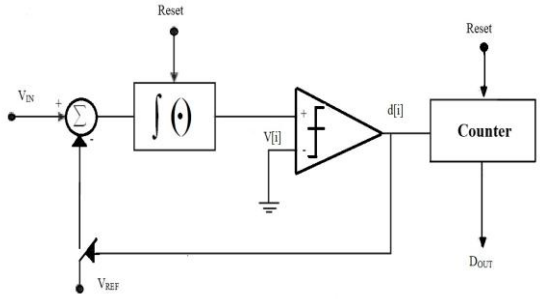

Fig.1: Architecture of Incremental delta-sigma ADC

The delta-sigma modulator comprises of self-biased amplifier and dynamic comparator. Operational Transconductance amplifiers need more power and bandwidth requirements for the delta sigma ADCs. In order to enhance the performance of switches in low supply voltages, voltage boosting technique is used[11]. In [12] second order sigma delta modulator an inverter was used as an amplifier. But the inverter creates two potential issues. Firstly, the amount of current flowing through the inverter cannot be determined. Secondly, there is a requirement for additional switches and capacitors to define the input common mode voltage of the inverter which is used in switched capacitor integrator. In brief the amplifier proposed in [13] has been modified in order to reduce the biasing issue.

Comparator is one of the elementary building blocks in majority of the analog to digital converters. In order to meet the difficulties in developing low voltage design, many techniques including supply boosting methods[14],[15] techniques employing body driven transistors[16],[17] are used. Though these techniques are very effective there still exist issues on reliability.

These issues of reliability are addressed through the techniques used in this paper.

This also gives better results in power savings when compared to other types of comparator.

In this work, a self-based amplifier which is more suitable for operating at low power condition is introduced, of which the principle of operation is discussed in the following sections. Section II & III mentions the self-biased amplifier with switches, design of the comparator and Delta Sigma Modulator. Section IV discusses the computed results and the conclusion is mentioned in Section V.

II. CIRCUIT DESIGN

A. *Review Stage*

As concisely explained in the introduction, the circuits of self-biased amplifier with switches and the double tail dynamic comparator is discussed in this section. As explained earlier, biasing more no. of amplifiers is not an insignificant task.

The above mentioned problems can be reduced by using self-biasing phenomena. Fig.2(a) shows the conventional self-biased amplifier.

The amplifier has two inverters which are connected in parallel and the current of these inverters is generated by the upper PMOS and lower NMOS transistors. The operation of this circuit is while one inverter amplifies an input signal the next inverter

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generates the biasing conditions of the amplifier.

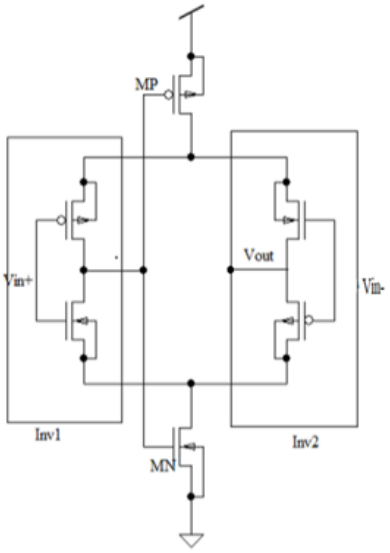

Fig.2: (a) Conventional self-biased amplifier

In short, as in Fig.2(b) the inverters are allowed to exchange the roles by addition of two switches which are driven by two-phase non overlapping clocks.

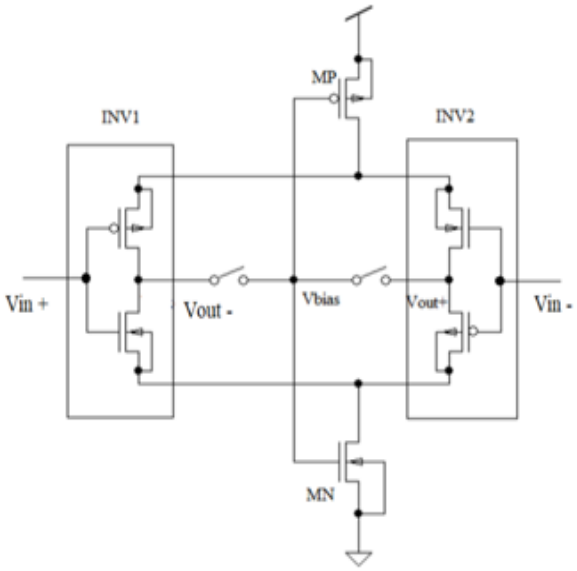

Fig.2: (b) Self-biased amplifier with switches

While inv1 acts as an amplifier for the first integrator, inv2 places the bias current (ϕ_2). In the next phase, inv2 merges the charge from the first integrator and inv1 places the bias current(ϕ_1). One of the sub blocks of delta sigma modulator is comparator. Double tail dynamic comparator is used in the delta sigma modulator.Fig.3 shows the circuit diagram of the double tail dynamic comparator [17].

The principle of this comparator is to increase ΔV f_n/f_p which in turn increases the latch regeneration speed. The speed is increased by two control transistors MC_1 and MC_2 which is connected in cross coupled manner. MC_1 transistor is connected in parallel with M_3 transistor and MC_2 transistor is connected in parallel with M_4 transistor. For this purpose, are the two added in a cross coupled manner to the first stage in parallel to M_3/ M_4 transistors. The operation of this comparator is as follows.

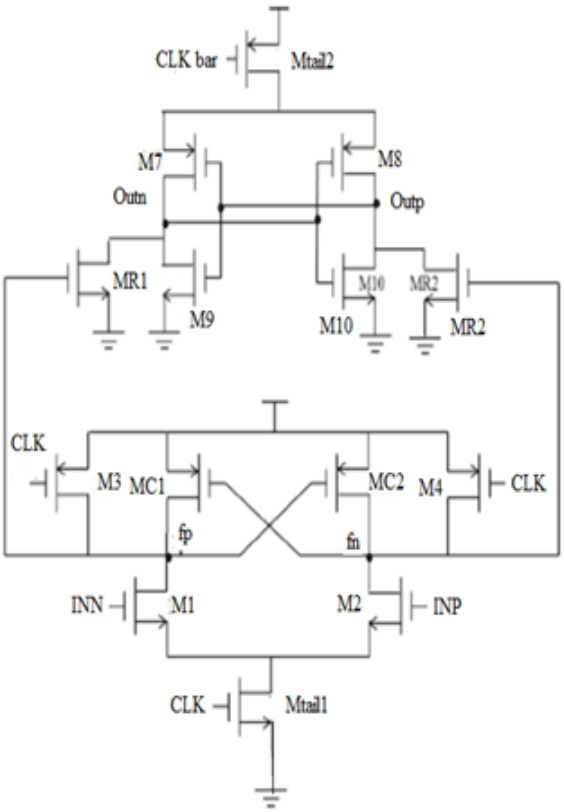

Fig.3: Double tail Dynamic Comparator

When the clk input is 0, the M_{tail1} and M_{tail2} NMOS transistors are OFF and the pull-up transistors M_3 and M_4 transistors pulls up both the nodes f_n and f_p nodes to $V_{DD.}$ Therefore both the PMOS transistors M_{C1} and M_{C2} are OFF. The both transistors M_{R1} and M_{R2} conduct and bring the latch outputs to zero. When the clk input is 1, the M_{tail1} and M_{tail2} NMOS transistors are ON and both the PMOS transistors M_3 and M_4 are in OFF state. There may be change in the voltages at the f_n and f_p nodes based on changes in the input voltage. If the INP> INN, the voltage in the node f_n drops faster than $f_{p.}$ This turns ON the M_{C1} PMOS transistor, which pulls the f_p node to V_{DD}. The M_{C2} NMOS transistor is OFF and the voltage across the node f_n discharges, which turns ON the PMOS transistor. This PMOS transistor pulls up the node f_p to $V_{DD.}$ This increases the potential difference between the nodes f_p and f_n and reduces the regeneration time of latch.

III. DELTA SIGMA MODULATOR

Two-phase non overlapping clock pulses are used to operate the modulator. Fig. 4 shows the circuit diagram of delta sigma modulator and the timing diagram of the same. During phase ϕ_1 sampling capacitor C_{11} of the first modulator samples the input signal. Meanwhile the second modulator completes signal integration. During phase ϕ_1 and ϕ_2 the voltages across the capacitors are shifted using the level shifting technique which performs the summation of first and second modulator outputs.

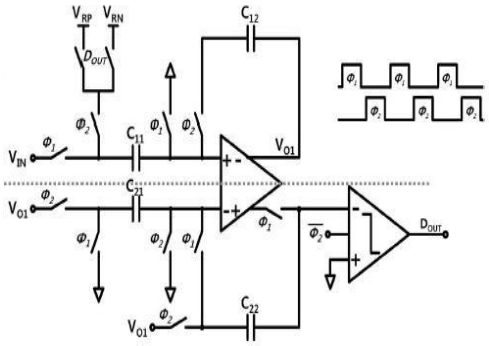

Fig. 4: Circuit Diagram of Delta Sigma Modulator

IV. RESULTS AND DISCUSSION

The self-biased amplifier with switches and double tail dynamic comparator is established in 90nm CMOS technology. The schematic of the self-biased amplifier is shown in Fig.5 which is suitable for sigma delta ADC's. In order to minimize the short circuit current the values of the transistors are chosen carefully.

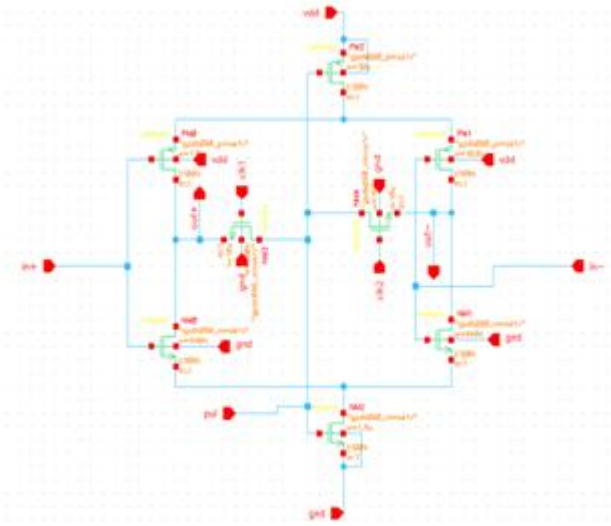

Fig.5: Schematic of self-biased amplifier with switches

Fig.6 shows the transient output of self-biased amplifier for 0.6*V* V_{p-p} analog input signal with 1GHz frequency. The output of the self-biased amplifier is the amplified analog signal.

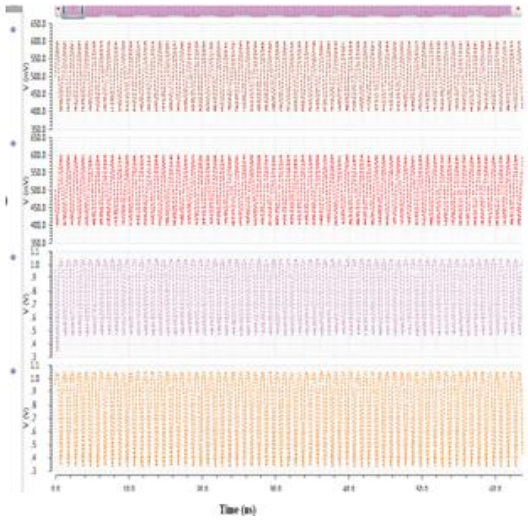

Fig.6: Transient output of self biased amplifier

Fig.7 shows the gain of the self-biased amplifier for 20MS/s. The gain obtained is 41.13dB for 0.6$VP-P$ signal.

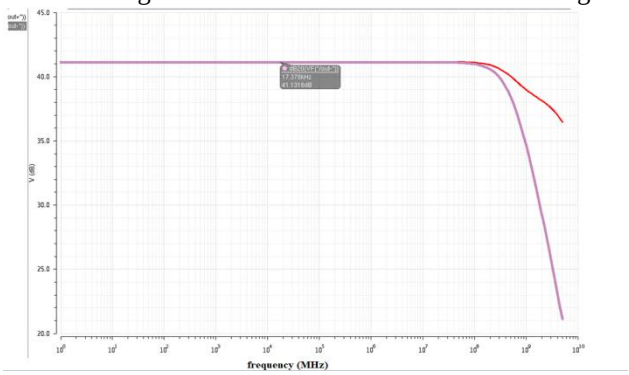

Fig.7 Gain of self-biased amplifier with switches

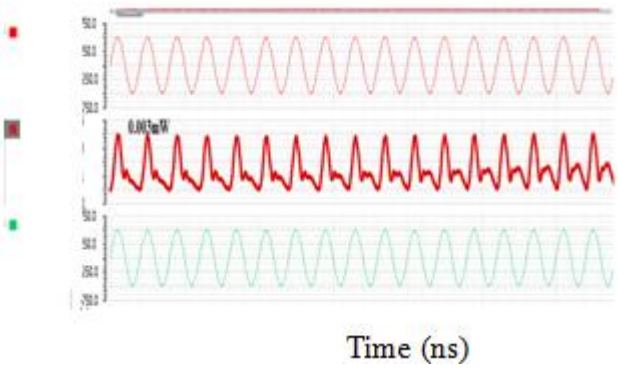

Fig.8: Power obtained for self-biased amplifier with switches

Fig.8 shows the power consumption of self-biased amplifier. The power consumption of this amplifier is 0.003mW.Fig.9 shows the schematic of Double tail Dynamic Comparator.

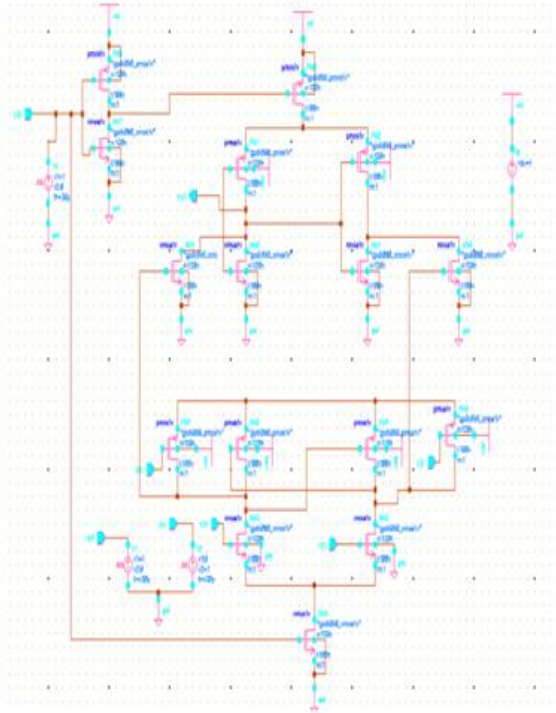

Fig.9: Schematic of Double tail dynamic comparator

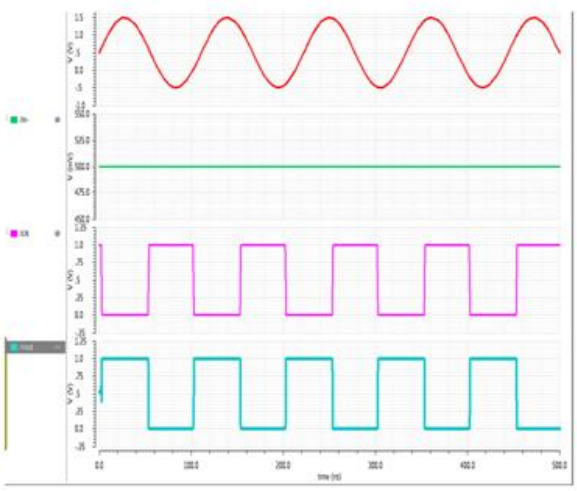

Fig.10: Transient response of Double tail dynamic comparator

Fig.10 shows the transient response of double tail dynamic comparator. The inputs given to the comparator are analog in nature which is of $1VP-P$. The comparator compares two inputs and if the positive input is greater than the reference input the output is logic 1 otherwise it becomes logic 0.

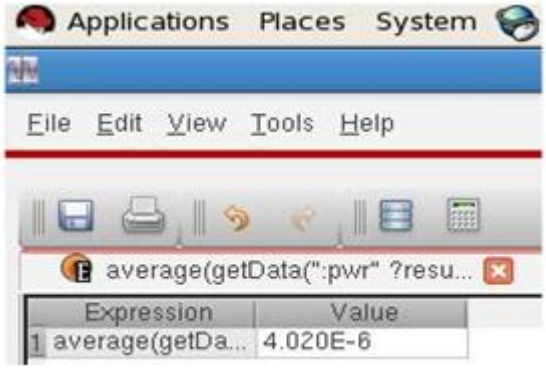

Fig.11: Power obtained from double tail dynamic comparator

Fig.11 shows the average power obtained from double tail dynamic comparator from 1V power supply. Table 1 shows the comparison between different types of comparator. When compared to all the conventional type comparators, the designed double tail dynamic comparator suitable for delta sigma ADC consumes less power of 0.4µW.

Table I: Comparison of different types of comparator

Architecture	Technology (nm)	Power (mW)
Self-calibrating Dynamic Comparator [18]	90	0.4
Dynamic Comparator with offset calibration [19]	90	0.61
Preamplifier based Dynamic comparator [21]	90	0.17
Clocked comparator [20]	65	0.6
This work	90	0.4 (µW)

The schematic of 12-bit incremental delta-sigma ADC is shown in Fig.12.The power consumption of 14- bit delta sigma ADC is shown in Fig.13. This output is taken for 0.6Vp-p analog input.

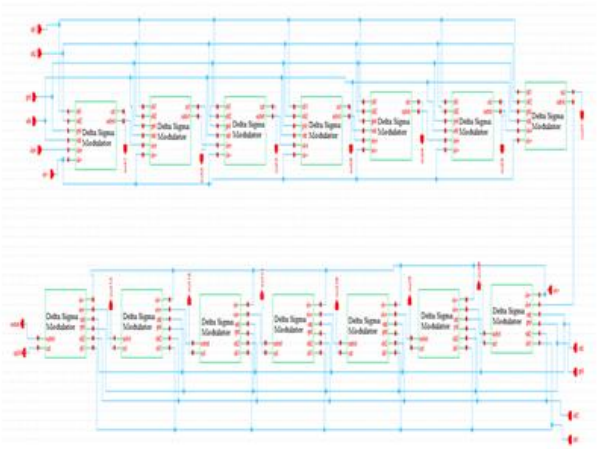

Fig.12: Schematic of 12-bit delta-sigma ADC

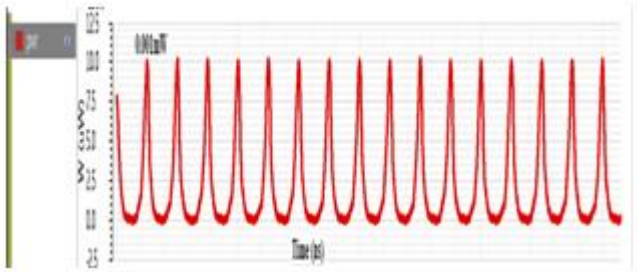

Fig.13: Power consumption of 12-bit delta-sigma ADC

The power consumption of 12-bit incremental delta-sigma ADC is 0.001mW.Fig.14 shows the spectrum analysis window for 14-bit delta sigma ADC. Table II shows the Performance Summary of 14-bit delta sigma ADC.

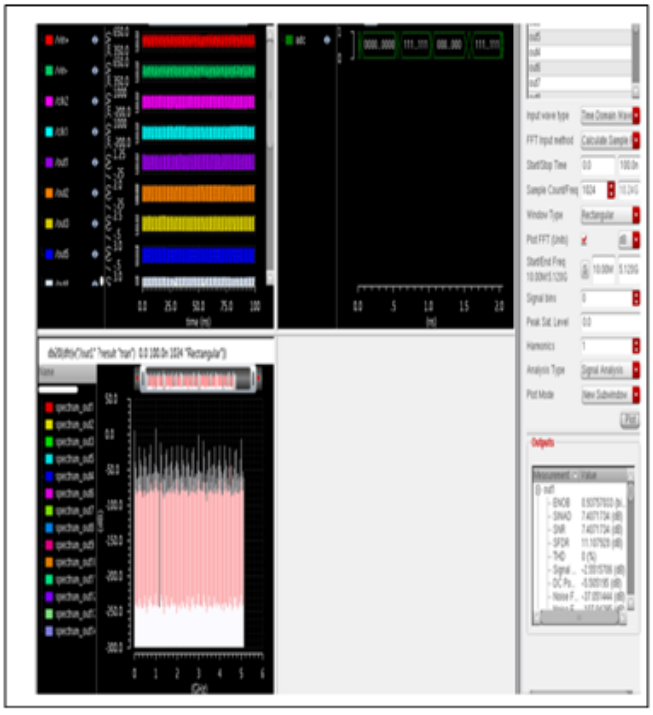

Fig.14: Spectrum analysis Window for delta sigma ADC

Table II: performance summary of 14-bit delta sigma adc

Parameters	Values
Technology	90nm
Resolution	14 bits
Power Supply	1V
Sampling Rate	20MS/s
ENOB	12.85 bits
SNR	76.71dB
SFDR	97.51dB
Conversion Time	0.07ps
Total Power Consumption	0.001mW

V. CONCLUSION

The self-biased amplifier with switches and double tail dynamic comparator circuits are simulated using 90nm CMOS process. The power of self-biased amplifier with switches and double tail dynamic compactor are 0.003mW and 0.004mW respectively. The gain of the amplifier is 41.14dB at 20MS/s. Simulation results shows that the power consumption of 12-bit incremental delta-sigma ADC is 0.001mW. Since the designed 14-bit incremental delta sigma ADC consumes less power it is suitable for low power applications such as CMOS image sensor applications.

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