Design and Implementation of Novel controllers in Digital Circuits Using GDI Technology

L. Prabhavathi, S. Baskar

Abstract--- A New model of an approach presents GDI full adder based on the reflected binary gray code design of multiplexer. The Weighted Code Approach has been Existed to generate Gray Code that Gray code is basically reflected binary code in which two successive values differ in only one bit. In general there are different methods of converting as a decimal number to Gray code is performed by converting decimal to binary and then binary to Gray code.. In this proposed Design and Implementation of Novel controllers in digital circuits using GDI technology is consist of three novel circuits one is gray code conversion of "multiplexer circuit" and other one is" logic circuit " and last one is" reflected binary code circuit" and all novel circuits produce gray code output. Low complexity of GDI technology to be suitable design for power-efficient as well as for power-delay products and also used to reduce power consumption in area of digital circuits .All simulations are done by Tanner using TSMC BSIM 0.25um technology. This approach is proposed for fast design, low power circuits, improve power characteristics.

Keywords--- GDI(gate diffusion input),low power, shift right operation, delay, digital circuits,, XOR-gate, AND- gate , OR -gate, gray code conversion 2x1 MUX.

I. INTRODUCTION

The Novel controller consists of the following three section such as, Multiplexer, Logic circuit, Reflection binary code.

In digital circuits using GDI technology such as Reflected binary code (RBC), also known just as reflected binary (RB) or Gray code after Frank Gray, is an ordering of the binary numeral system such that two successive values differ in only one bit binary ,The reflected binary code (RBC), also known as Gray code after Frank Gray, is a binary numeral system where two successive values differ in only one bit (binary digit). Another one is Multiplexing is the generic term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speed and as such, the device we use to do just that is called a Multiplexer. The multiplexer, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple lines called "channels" one at a time to the output.

II. BASIC GDI CELL

[1]The GDI can be constructed based on the basic GDI cell in different type of digital circuits and also in VLSI circuits. power consumption and delay are major issues. Fig 1. Shows one way to built a GDI technology . it consists of three inputs namely

1. G- common input to the gate of NMOS and PMOS
2. N- input to the source/ drain of NMOS
3. P- Input to the source /drain of PMOS

The GDI cell is same as that of CMOS inverter structure. But in CMOS inverter the source of the PMOS is connected to VDD and the source of NMOS ground.

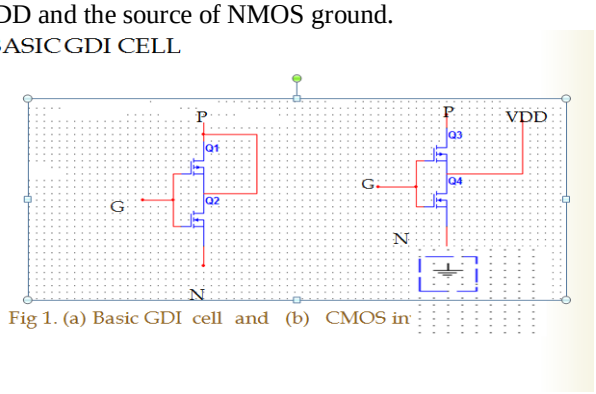

Fig 1: (a) Basic GDI cell and (b) CMOS inverter

Table I: Functional table using GDI cell

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

III. EXISTED SYSTEM

A). Previous Existed Weighted code Approach for generation of gray code.

[4]More formally, a Gray code is a code assigning to each of a contiguous set of integers, or to each member of a circular list, a word of symbols such that each two adjacent code words differ by one symbol. These codes are also known as single-distance codes, reflecting the Hamming distance of 1 between adjacent codes.

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There can be more than one Gray code for a given word length, but the term was first applied to a particular binary code for the non-negative integers, the binary-reflected Gray code, or BRGC, the three-bit version of which is shown above. . Last one is Weighted Code Approach to Generate Gray Code outputs. Weighted code approach for development of gray code conversion output through pulse code communication by F.GRAY in the year of 1953,March17.

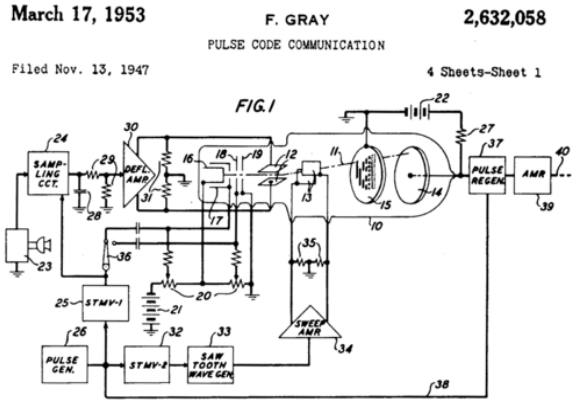


Fig. 2: Weighted code Approach for generation of gray code

B). Previous Existed gray code 2x1 mux design for generation of gray code

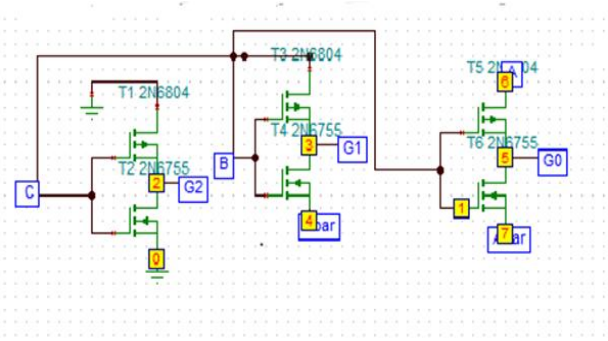


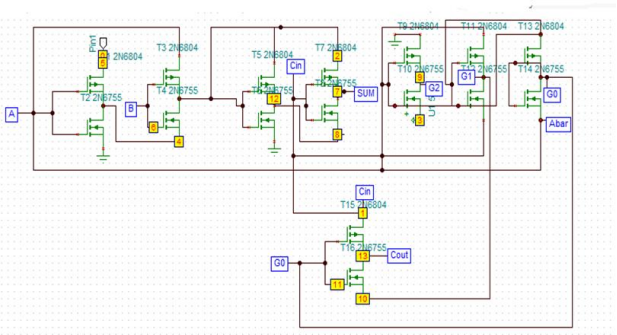
Fig. 2: Existed gray code 2X1 mux

The above Existed block diagram of gray code 2x1 mux design for generation of gray code conversion output that conversion output has been observed with consists of the source of the PMOS is connected to VDD and the source of NMOS ground logic gates and also with the multiplexer blocks. Its outputs are Go, G1,G2 ,inputs are A, B, Ci .

Table 2: Existed gray code output conversion using 2X1 multiplexer

Ci	B	A	G2	G1	G0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

III. Block Diagram of Proposed Gray code Conversion using GDI technology in Full Adder:



The Fig 3. is block diagram of proposed design of GDI full adder is consists of the following elements

1. Reflected binary code
2. logic operation circuit

3.1. Reflected binary code

[7] Reflected binary code for generation of gray code is also known as reflected binary or Gray code is an ordering of the binary numeral system such that two successive values differ in only one bit .The reflected binary code , also known just as reflected binary (RB) or Gray code after Frank Gray, is an ordering of the binary numeral system such that two successive values differ in only one bit . reflected binary code (RBC), also known as Gray code after Frank Gray

Single stage of Reflected binary code

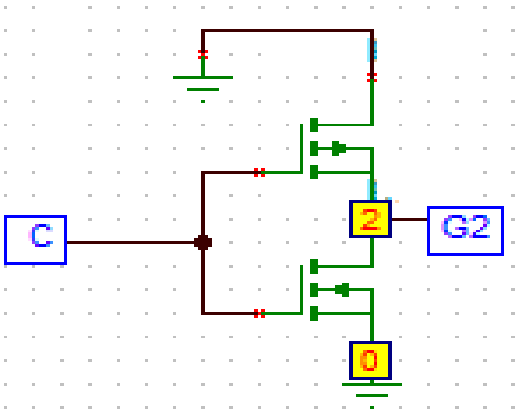


Fig. 3.1: Single stage 2X1mux

[6] Reflected binary code in 2x1 mux the logic is implemented using 2x1 multiplexers which has two inputs and one output for each multiplexer with a select line in its structure. The output is generated depending on the selection line only .These multiplexers can be designed with help of logic circuits that uses PMOS and NMOS transistors. 2x1 mux contains PMOS and NMOS transistors are arranged alternatively in three stages first stage output is G0 and corresponding stages out puts are G1 and G2 as shown in below figure .In this method GO,G1,G2 outputs .The logic is implemented using 2x1 multiplexer which has two inputs and one outputs G0,G1,G2 respectively.

Three stage of Reflected binary code in 2×1 mux

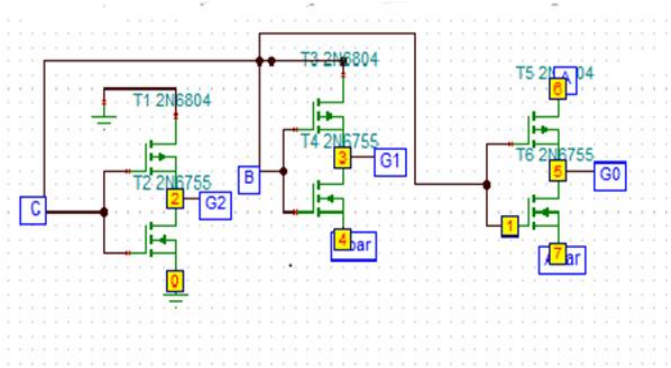


Fig. 3.2: Three stage 2X1mux

[7] We can have three stage of reflected binary code circuit when three set of single stage reflected binary code circuits are arranged alternatively to produce gray code conversion output. The proposed GDI technology is being used in digital circuits But the proposed GDI technology is processed with the gray code mux circuit and along with the logic circuit operation. Actually the proposed GDI gray code design of full adder is similar to Full adder using GDI technology except gray code mux and shift right circuit .The GDI gray code mux which is designed with inputs of "a" and" b" and ,"ci" and it's outputs are SUM and" C_{OUT}" of full adder.

$$Cout=(Go)C+AB$$

$$Go= A \oplus B,$$

$$G1= B \oplus C,$$

Using above equation, G1 can be calculated. G1 values are showed in table 4

$$G2=C,,\text{and } Go=A \oplus B$$

Similarly, G1 and G2 are calculated by using above equations

The equation represents the equation of a GDI full adder , therefore the values of G0and G1 and G2 are provided to 2X1 MUX circuit to get "Cout " which is the out put of Graded GDI full adder design

$$Cout=(Go)C+ AB$$

Logic operation circuit (XOR/XNOR)

[2] If we use graded design to represent position of error due to improper alignment can be reduced. This is because the gray code design assures that only one bit will change each time. Other two bits positions of two adjacent are always same and hence there is no possibility of error.

This GDI technology consist of two xor and one Graded design of 2×1 MUX and right shift operation block. GDI technology is recently developed and proposed with graded design 2×1 MUX, it is efficient technology for standard CMOS technology.

In this block diagram 5 blocks are there Cout is output from block 3,block 4 ,inputs are transmitted to block 1 and block 2.graded design of 2×1mux is being designed using GDI technology which is associated with the XOR and AND/OR operations to develop of accuracy result of Cout ,[3]

$$S = \overline{A}.\overline{B}.C_{in} + \overline{A}.B.\overline{C}_{in} + A.\overline{B}.\overline{C}_{in} + A.B.C_{in}$$

$$C_{out} = \overline{A}.B.C_{in} + A.\overline{B}.C_{in} + A.B.\overline{C}_{in} + A.B.C_{in}$$

$$G2=C,\ G1= B \oplus C,\quad Go=A \oplus B$$

$$Cout= (A \oplus B)C+ AB,$$

$$(or)\quad Cout= (Go)C+ AB$$

C_{out} is determined from resultant values of G0,G1,G2 through 2X1 MUX circuit

Table 3: Proposed gray code output with novel controllers using GDI technology in Full Adder

Decimals	C	B	A	G2	G1	G0	Sum	Cout
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	0
2	0	1	0	0	1	1	1	0
3	0	1	1	0	1	0	0	1
4	1	0	0	1	1	0	1	0
5	1	0	1	1	1	1	0	1
6	1	1	0	1	0	1	0	1
7	1	1	1	1	0	0	1	1

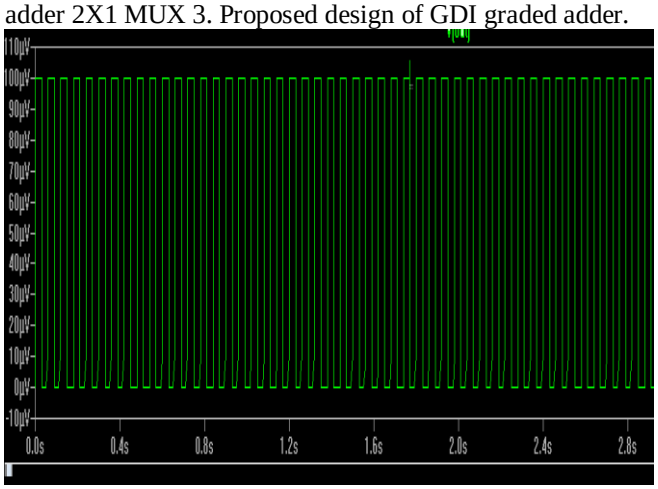
Table 4. shows the outputs of gray code design mux are G0, G1, G2 those values are obtained by the graded design of 2X1 mux. Each and every graded 2X1 mux produces the corresponding out put of G1 and G2, the certain value of G0 is obtained at the A and A bar of 2 x 1 mux and correspondingly G2 at C and G1 by the C and B C bar points .

$$Cout= (A \oplus B)C+ AB,\quad (or)$$

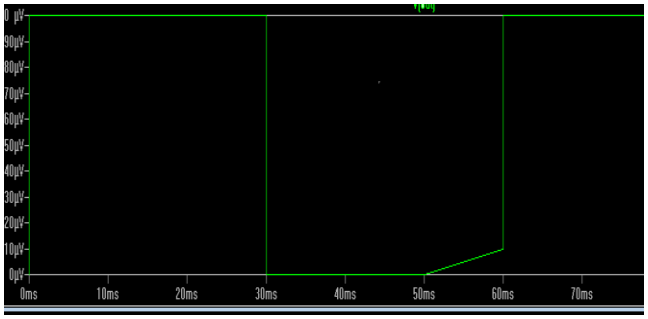
$$Cout= (Go)C+ AB$$

IV. SIMULATION AND RESULT

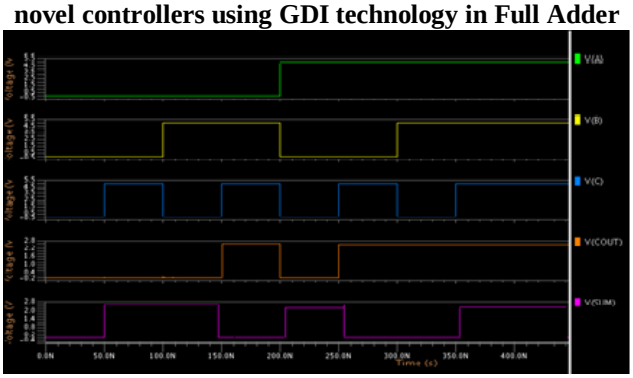
the design of GDI graded adder has been simulated using SPICE and simulation out puts are obtained by SPICE and output waveforms are shown in above. The simulation result can be done for following figures such that1.GDI graded adder 2X1 MUX 3. Proposed design of GDI graded adder.



(IV-i) Output Waveform of Proposed gray code with novel controllers using GDI technology in Full Adder



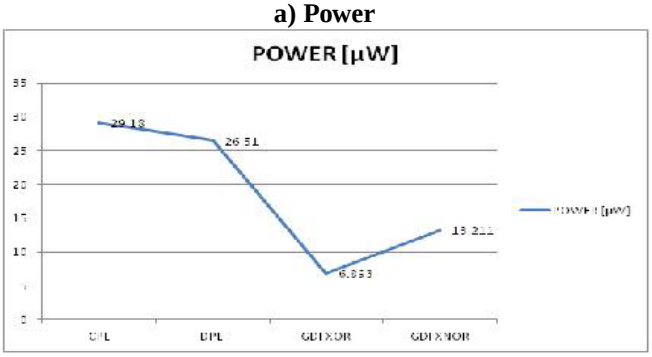
IV-ii) Output Waveform of three stage gray code with novel controllers using GDI technology in Full Adder



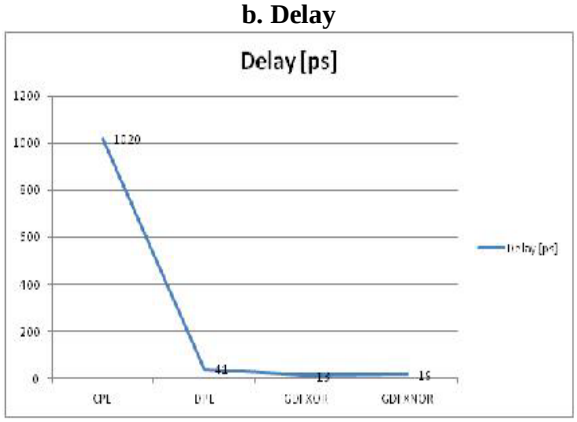
(IV-iii) Output Waveform of gray Code design of GDI in full adder

The GDI is an acronym for the digital circuits using Xor/Xnor gates.GDI has been verified from full adder circuits with different methods but proposed novel controller is completely different over existed GDI full adder circuits. The above showed waveforms are the output of proposed Graded GDI full adder circuits. Proposed gray code GDI for analysis of Power, Delay.

a) Power



b. Delay



V. CONCLUSION

The GDI is an acronym type technology for low power design and also for low power consumption.GDI technique for power-delay products were verified. The implementation of GDI graded adder circuit was improved significantly with efficient parameters. The design of GDI technology is simple and high reliability which proves the power–delay product performance Here proposed GDI graded design of full adder for analysis of reducing power and power delay product and efficiency of area power delay product and also for accuracy measurement of important parameters are designed with logic gates delay is performed by right shift operation .Graded design of full adder is more significant over different GDI techniques .

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