Comparative Study of Fault Mitigation Techniques of Level Three Neutral Clamped Inverter Fed Induction Motor Drive

Y. Krishna Priya, M. Vijaya Kumar

Abstract--- For power applications having high voltages multi-level inverters gain more attentiveness in comparison to conventional two level power converters due to less harmonic deformation, elevated DC link voltage, low EMI. But faults can affect the performance of multi-level inverters. By the large, 70% of the occuring faults in multi-level inverter circuits are open circuit faults. When faults exist in the system, fault mitigation is also a prior important task for the efficient operation of the system. In this paper, a comparison between two fault mitigation techniques, former the conventional asymmetrical PWM and latter the leg four implementation were provided which were simulated in the software MATLAB/SIMULINK and the results were shown at the instants of prior to fault, during fault and fault after mitigation.

Keywords--- Neutral Clamped Multi level inverter, induction motor drive, open fault, asymmetrical sinusoidal pulse width modulation, mitigation.

I. INTRODUCTION

Electrical machines are the electro-mechanical devices which convert either mechanical energy to electrical or vice-versa. Electric engine is a machine which converts electrical form of energy to mechanical. These machines are developed to diminish the human efforts and interference. Motors can be broadly classified depending upon the input electrical supply – DC motors and AC motors.

In industrial applications of motors, AC motors are more preferred due to available of AC supply eliminates additional rectifier circuits, robust construction, and efficiency, low cost. Widespread of power electronics also make AC machines more flexible than DC motors. Synchronous motors and Asynchronous motors are the types of AC motors. Need of additional starting methods and slip-ring and brush assembly makes synchronous motors inferior to induction motors. Also are of robust and simple in construction, efficient and will have good speed regulation. Thus induction motors are preferred in a good number of the industrial applications.

For industrial applications, Voltage sourced converter (VSC) is mostly used at a front end connection for induction motor drive owing to its simplicity and easy control, the main object of voltage sourced inverter is providing variable voltage, variable frequency for the drive to maintain its speed at desired value [1-3]. Conventionally induction motor drives supplying from a voltage sourced inverter are extremely popular because of its low cost and low maintenance. Multi-level inverters [4-7] plays vital role in this regard as conventional 2- level inverter faces problem with high harmonic distortions and electro-magnetic interference.

Also due to high rate of change in voltage common mode voltage might be occurred inside the motor windings. Multi-level inverter requires high number of switches and produces the output in tiny steps [8-10].

Sinusoidal Pulse width modulation technique be used for frequency and voltage variation of the induction motor drive, but as the drives power rating increases due to high dv/dt the motor winding insulation life span decreases, to reduce this effect neutral clamped inverter is used in which increase in count of levels decreases the dv/dt rating but it increases the amount of switches due to which fault mitigation is challenging task in multi-level inverter. [11-14].

Normally of all the faults [15-17] in induction motor drive 70% of the faults are open faults as per the survey. Conventionally for providing pulses to the inverter we use asymmetrical PWM technique which will also be used for mitigation of these faults.

The paper provides the comparison between the conventional asymmetrical PWM technique and the proposes fourth leg implementation and compared with conventional asymmetrical PWM technique for a 3-level diode clamped inverter fed induction motor drive.

II. ASYMMETRICAL PWM TECHNIQUE

Power industry is been attracted to multi-level inverters very much these days owing to the increased level of power usage.

Conventional 2-level converters gives the level of input DC bus voltage as the output with two-level. Multi-level inverter gives stepped output levels resembling sinusoidal waveform with increase in number of levels and thus reduces the total harmonic distortion.

Variation of Voltage and frequency is obtained using multi level inverters. The inverters output have to fit the connected load in terms of frequency or voltage level. One of the types of multi-level inverter is diode clamped inverter or also called as neutral point clamped inverter which is shown in the fig 1.

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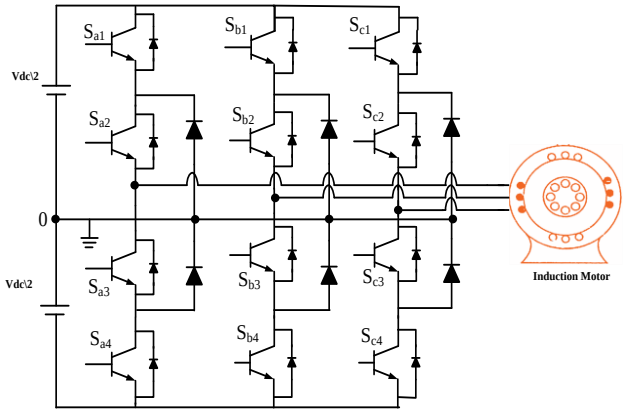

Fig.1: Conventional 3-level diode clamped inverter

In diode clamped multi-level inverter, as the name imply, the circuit needs clamping devices and diodes will be used as clamping devices. It has three legs and the DC link potential is divided across the power electronic switches through capacitors. Only one switch of one leg should be turned ON at an instant and the same legs other switch should be necessarily turned OFF to prevent short circuit of leg.

The DCMLI output is fed to induction motor and its speed is controlled by the inverters output frequency and thus constituting an IM drive.

In inverter, fault occurrence is very common in nature and desires to be identified and mitigated for the appropriate functioning of drive system. Since the common fault type is open type of fault, to identify and mitigate open fault an algorithm has been developed. The steps that involved in clearing the inverter faults and ensuring suitable operation of inverter are first is to spot the phase/leg of the incidence of fault. This developed algorithm can detect location of fault in any arbitrary phase of inverter circuit. Firstly the output phase currents of diode clamped multi-level inverter were measured. Measuring the currents in phase can exhibit the fault location where open circuit doesn't allow current and that particular phase current will be equal to zero. The measured phase current is computed to know the fault existence

Fault mitigation algorithm during fault in any arbitrary phase was shown in fig.2.The response generates 0 and 1 for the algorithm. If fault exists, the output will be 1 and otherwise 0. After computation of fault existence, the phase in which the fault exists must be identified. After computation if all the phase currents reads value, it implies that there is no fault, if currents in any phase read zero, then fault exists and identification is to be needed in which phase fault persists. If amplitude of the signal is non-zero value, it denotes that no fault exists. If no fault exists, all the currents in three phases will read the specified magnitude, phase angle and frequency as per the reference of respective phases. If fault exists, the algorithm will check in phase A, B and phase C for fault. The algorithm checks for the conditions of amplitude, phase angle and frequency and then decides the fault existence in particular phase and sends required gate signals to the DCMLI.

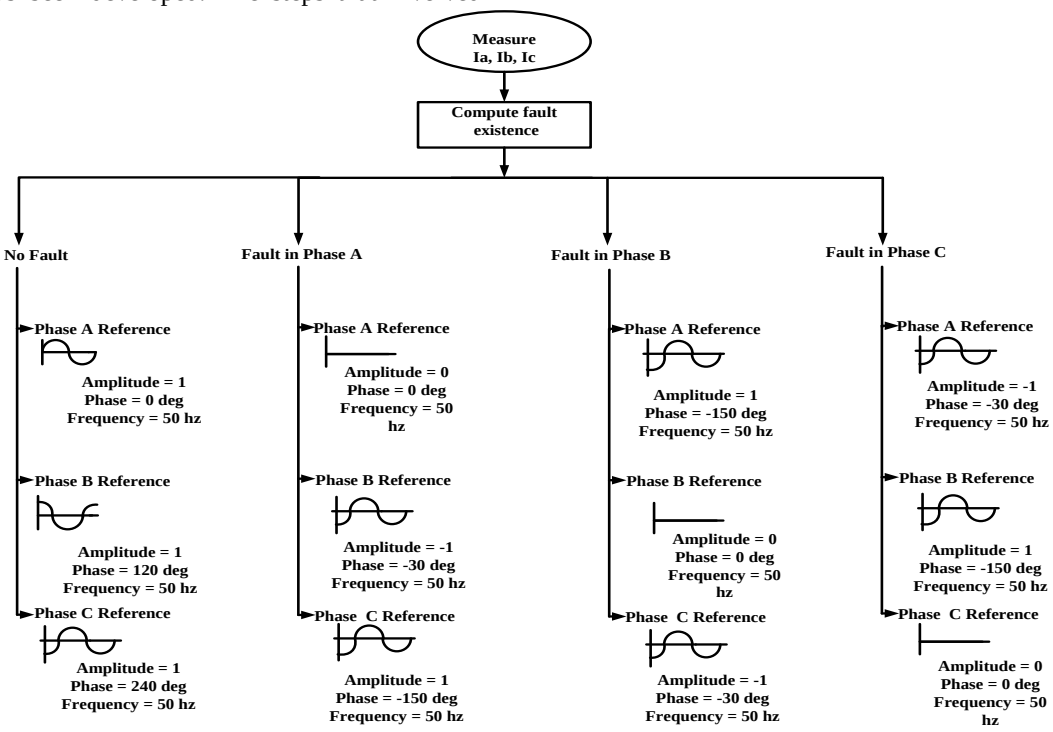

Fig.2: Asymmetrical PWM Fault mitigation algorithm during fault in any arbitrary phase

III. FOURTH – LEG APPROACH

The proposed three-level diode clamped inverter with leg four fed IM with fault mitigation algorithm is shown in fig.3 consists of additional fourth leg to a conventional 3-level 3-leg inverter. The fourth leg comes into act when fault is identified in inverter circuit. Leg Four is operated by thyristors and the thyristors action sends triggering signals to the power electronic switches in leg-4. The faulty leg from the circuit will be disconnected by turning OFF the switches in respective faulty phase and at the same instant of operation, the fourth leg operated by thyristors acts as an

active leg replacing faulty leg. As said, fourth leg is operated by thyristors and the active signals to the fourth leg will be sent from the algorithm to thyristors which turn-ON respective switches in leg-4 to acts as active instead of faulty phase.

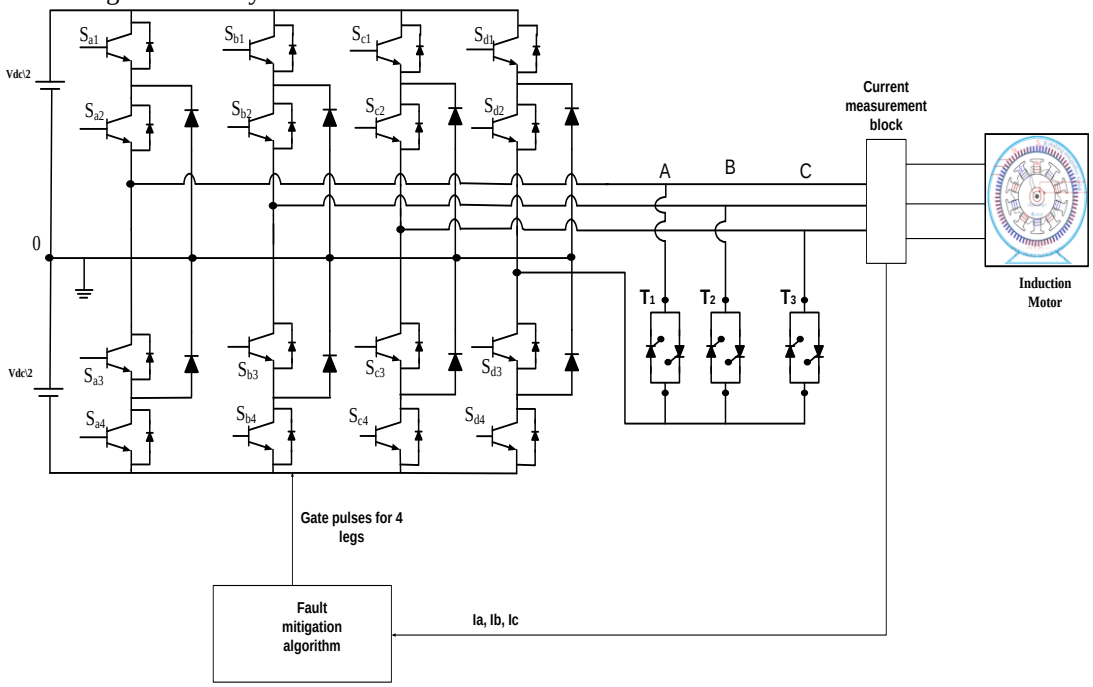

Fig.3: Proposed three-level four-leg diode clamped inverter fed induction motor drive with fault mitigation algorithm

If computed value senses fault existence, the signal will be sent to respective steps and also, no fault case will be operated with respective action. If no fault exists, command will be sent such that thyristor groups T_1, T_2 and T_3 will be turned OFF. If computed value senses fault in phase A, command will be sent such that to turn OFF gate pulses to phase A, then turn ON thyristor group T_1 activating leg 4 by bypassing gate pulses of leg 1 to leg . Similarly for phase – B, Cthyristor groups T_2, T_3 will be activated under fault in the respective phases.

The output phase currents coming from the diode clamped inverter were sensed and computed for fault existence. According to the commands in fault mitigation algorithm, the gate pulses were generated for four legs of the diode clamped inverter. When fault exists in inverter circuit, the faulty phase is disconnected from the core circuit by turning OFF gate pulses to respective faulty phase semiconductor switches. These gate signals were bypassed to fourth leg and the inverter functions in normal condition as if there is no fault.

IV. SIMULATION RESULTS

Table I: System Parameters

Parameter	Value
Stator Impedance	2.9+j71 Ω
Rotor Impedance	2.2+j71 Ω
Inertia of motor, J	0.05
Input voltage	700V
Capacitance	3000e-6
Switching Frequency	3050 Hz
Induction motor power rating	10 kw
Load torque	20 (or) 10 N-m
Modulation index	1

Case 1: Fault mitigation in phase – A using Asymmetrical PWM technique

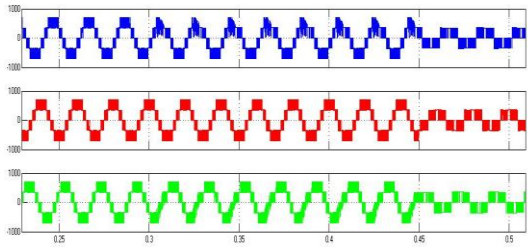

Fig.4: Line voltages in Three-level diode clamped inverter fed induction motor drive with fault in phase-A

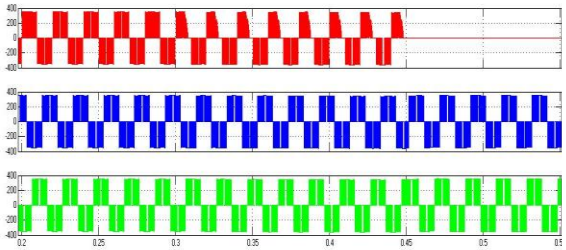

Fig.5: Phase voltages in Three-level diode clamped inverter fed induction motor drive with fault in phase-A

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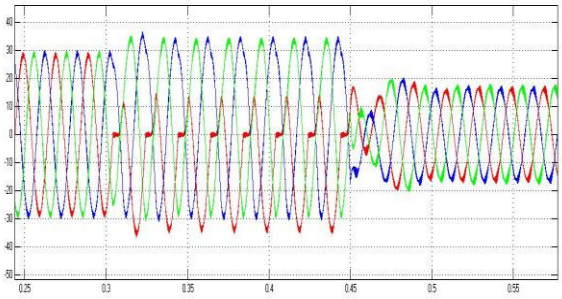

Fig.6: Line currents in Three-level diode clamped inverter fed induction motor drive

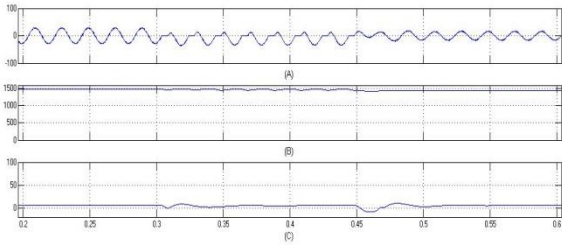

Fig.7: Stator current, speed and torque in diode clamped inverter fed induction motor drive with fault in

System parameters of three-level diode clamped inverter fed induction motor were shown in table-1. Considering the fault is occurring in phase – A.Fig.4 shows the line voltages, Fig.5 shows the phase voltages of 3-level inverter mitigation when switch is open, Fig.6 shows the line currents mitigated when switch are open.From those line voltage and current the fault was produced at 0.3 seconds and mitigated at 0.45 seconds. During fault condition the waveforms in unbalanced after fault mitigation those become as balanced.

The motor characteristics of induction motor fed from 3-level inverter mitigation when the switch is open were shown in fig.7. From the motor characteristics, the stator current after the fault mitigation regains its normal shape maintaining constant speed and torque without any disturbances.

Case 2: Fault mitigation in phase – A using Fourth leg implementation

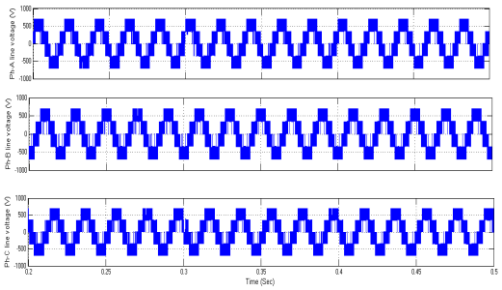

Fig.8: Line voltages in Three-level diode clamped inverter fed induction motor drive with fault in phase-A

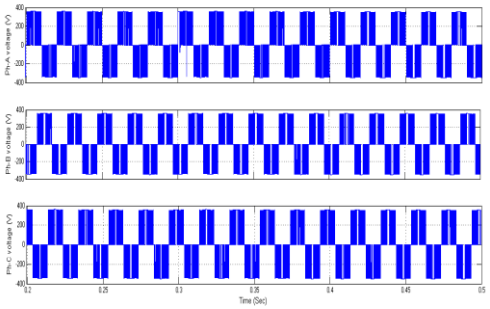

Fig.9: Phase voltages in Three-level diode clamped inverter fed induction motor drive with fault in phase-A

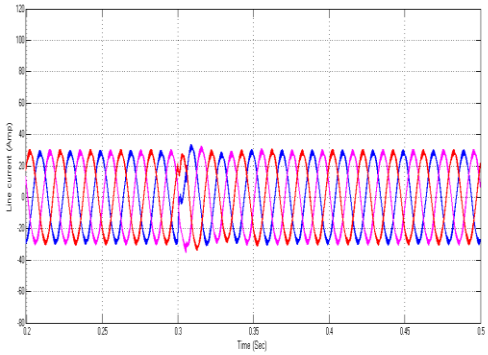

Fig.10: Line currents in Three-level diode clamped inverter fed induction motor drive with fault in phase-A

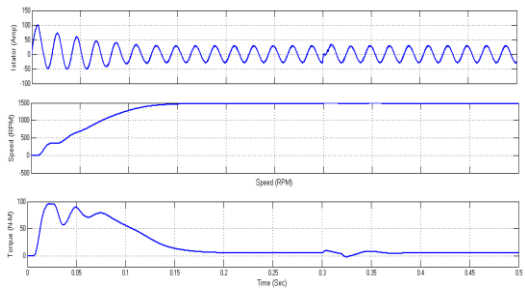

Fig.11: Stator current, speed and torque in diode clamped inverter fed induction motor drive with fault in phase-A

Line voltages and phase voltages of a three-level four-leg diode clamped inverter fed induction motor were shown in fig.8 and fig.9. Line currents of induction motor drive are depicted in fig.10. Induction motor characteristics stator current, speed and torque were shown in fig.11.

Fault was identified at instant 0.3 sec and due to the existence of leg-four; the fault was immediately cleared by activating fourth leg of diode clamped inverter. Fault is mitigated and the induction motor characteristics were resumed to normal shape indicating no disturbance in IM drive performance even when the fault has been identified.

V. CONCLUSION

Multi-level inverters ascertained their functioning in high power applications. Diode clamped multi-level inverter is one of the most frequently used topology in multi-level concept. But faulty conditions might occur very often in the case of inverters. In this paper a fault mitigating technique, which is peculiar to conventional asymmetrical PWM technique was explained. In conventional asymmetrical PWM technique fault will be mitigated but due to asymmetrical nature there will be some reduction in the output of the inverter. Fault has been identified at 0.3 sec and persists till 0.45 sec. At 0.45 sec the fault is been mitigated and motor characteristics were resumed to normal shape after the fault has been mitigated which were distorted during the fault occurrence.

To nullify the effect of fault, for the three leg inverter a fourth leg is added to evade the faulty phase. Fourth leg of diode clamped inverter gets active only when fault is identified in any arbitrary phase of diode clamped inverter following the fault mitigation algorithm which activates the fourth leg corresponding to fault in the phases. Motor characteristics prove to be undisturbed with the existence of fault in the phase from the results; speed and torque characteristics remain unchanged. Fault is observed at 0.3 sec and fault has been mitigated immediately so that the induction motor drive performance was unaffected. This proves the ability of developed algorithm and four-leg operation to be efficient in mitigating open type of fault that occurs in any arbitrary phase of diode clamped inverter.

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