International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-7 Issue-5, January 2019

High Level Synthesis of VLSI based Image Scaling Architecture for High Definition Displays

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Abstract: ***Due to rapid advancements in multimedia technology from consumer electronics to medical imaging, HDTV display systems image scale up/down process is necessary for efficient displaying entire scene without loss of its original quality. The edge oriented based image processing plays the major role in the Image processing technique. The current real time applications demands low complexity, low cost and high performance devices for portable applications and it is achieved through CMOS-VLSI technology. This paper presents an efficient approach for edge-oriented image scaling processor Technique with low power and low complexity VLSI architecture design for edge-oriented area of image pixel scaling technique. This paper approaches the horizontal scaling and vertical scaling processor technique for improving the size of the image with better image quality than the existing image scaling processor. The horizontal and vertical image scaling processor technique is implemented in the proposed technology in order to improve the input image size of 400 X 400 image into 800 X 800 with better image quality. The Proposed five stage VLSI architecture consists of three phases such as edge orientation, vertical scaling and horizontal pixels scaling blocks respectively. Then, this proposed edge oriented image scaling technique is implemented in the VHDL and synthesized in the XILINX ARTIX-7 FPGA and shown the comparison for power, area and delay reports.***

Index Terms**: *Bilinear, FPGA, HDTV display, Image scaling, VLSI architecture.***

I. INTRODUCTION

Now a day's digital Image scaling is more challenging problem to map different image sources on to fixed size of display device. In recent years digital display devices are more popular to display digital data. To remove noise effect during transmission or analog to digital conversion, digital virtual interfaces (DVIs) have been used. Due to resolution variations of the imaging sources or scene it is difficult to display on fixed size physical screen resolution of display devices such as liquid crystal display (LCDS) and flat panel display (FPD). Image interpolation is a process of estimating the missing pixel intensity value by taking known pixel values. Many researchers have contributed to this for improving the resolution level of input images. Mainly image interpolation algorithms are divided into two types based on the level of complexity and visual quality of interpolated image. The basic idea behind image scaling is to interpolate the image onto new sampling HR grid. So far many methods have been introduced to scale the image into required level of interpolations. The selection of particular method/model will surely depends on type of display used, memory requirement for storing and the level of computation used. A very basic approach is nearest neighbor approach [1] it is simple and gives feasible results up to some extent with excellent visibility of scaled image. But this method suffers from aliasing effect due to large scaling factor we impose. Later the most well known first order sample and hold approach is bilinear interpolation[2], [3] here the output scaled image pixels varies linearly with respect the sampling position. Traditionally used bilinear and bi-cubic methods provides zigzagging artifacts if we scale the image more than the prescribed interpolation factor. The more complex interpolation called bi-cubic was introduced. Although these methods performs well for lower scaling factors, as scaling magnitude increases due to high frequency nature will produce blur on displayed image. Recently methods introduced based on polynomial functions and taking both adaptability and correlation properties in mind. A new re-sampling area coverage based win scale algorithm was introduced in [4]. This technique is more suitable for variations in the display device characteristics. Also preserves edge characteristics and it can handle streaming data more straight forward way. In recent years, advancements in VLSI Technology will benefits the designer to improve the device density through scaling process but it will results poor reliability of the system. Field Programmable Gate Arrays (FPGAs) are solved many issues faced by the developers as FPGAs are easily programmed by the end user. Introducing new materials, device density and power minimization methods always provides more reliability. The testing time has been reduced drastically after FPGAs comes into the market. FPGAs provide many solutions for the designing of wireless communications networks and image processing applications. The performance of image interpolation algorithms have been verified with the help of FPGAs easily, meanwhile it is required more circuit components. Image sharpening filter realizations are easily done through FPGAs. First image samples are stored in the frame buffers later they can access for testing the performance of algorithms but it requires more storage capacity. To reduce the no. of buffers used, designers have to configure pipelining and parallelism mechanisms. To implement image processing applications effectively on FPGAs some third party tools will support. To convert HDL code conversion from the given high level model or C language third party software tools are commonly preferred.

Revised Manuscript Received on 30 January 2019.
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The improvements in multimedia and display technologies used in consumer handheld devices normally image re-scaling/de-scaling
methods are used to improve the image resolutions. The performance of the scaling algorithm mainly based on the required computations involved in the particular algorithm or design. Desired information of the image is available along the edges or boundaries. Fig 1. Shows the illustration of image scaling process. Left side image indicated min resolution image it can be scaled up to 2 times than its original pixels. For single pixel scaling normally we prefer four source pixels along with filtering mask. To achieve low cost VLSI architecture for image scaling we prefer area pixel scaling rather than point pixel scaling methods. We proposed method that simultaneously scales-up both chrominance and luminance components for high performance displays of resolution limit up to 800x800 pixels. In order to reduce the computational complexity of the proposed scaling of chrominance and luminance processor we used approximate computation techniques. Further the proposed algorithm handles stream of pixels directly with low memory support.

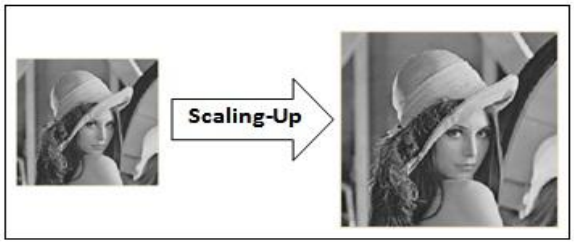

Figure 1. Illustration of Image Scaling-Up process

The FPGA implementation of this algorithm takes four line buffers rather than full frame buffer. The rest of the paper is as follows; in section I describe the introduction and need of efficient image scaling algorithms for next generation high definition displays. Section II gives the basic methods and some of the literature eon earlier works and section III describes proposed edge oriented image scaling algorithm. Section IV and V gives clear analysis of results of proposed method followed by conclusion and future prospects.

II. MATERIALS AND METHODS

The need of high performance low power VLSI based architectures increases due to the rapid growth in multimedia, HD television displays, high speed wired and wireless communications technologies. Recently the advancements in field programmable gate arrays (FPGAs) and re configurable nature will leads to design real time image and video processing applications is quite easy. FPGAs are one of the solutions due to its low cost high efficiency computing power. More recently high level synthesis (HLS) tools makes the design quite easy compared to earlier designs[5]. HLS design is the potential solution[6] for increasing the productivity of real time image and video processing applications. These tools directly optimize the given HDL algorithmic frame work and then optimized design maps on to the corresponding LUTs. HLS design also called C synthesis as it allows the hardware designers to efficiently build and verify their high performance implementations on targeted hardware devices for better control and optimization. Estimating the new data points within a given range of known set of data points is called image interpolation or image scaling. This paper presents the efficient VLSI architecture for edge based image scaling of size 400x400 pixels to 800x800. The proposed algorithm is designed using Verilog HDL language the functionality of the design is verified through Vivado HLS 2017.1 and implemented on Artix-7 FPGA board. In [7] authors have proposed extension of linear interpolation algorithm and decompose the 2D 4x4 interpolation into two vertical and horizontal interpolations. In [2] authors proposed bi-cubic interpolation algorithm for scaling up images in three phases such as generation of interpolation coefficients, applying interpolation process and designing of control unit to control entire process of pipelining. The computation complexity increases, it requires more multipliers and more buffers as zoom factor increases. The bi-cubic interpolation operation is extended up to 16 neighborhood pixels in [8] and used 16 interpolation coefficients. The memory accessing times, no .of multipliers, adders used to generate coefficients are also reduced. In [4]utilizing area coverage ratio of original pixels for estimating new scaled pixels values. This method is feasible for displaying digital images on high definition display devices with good edge preserving, takes less memory to store weight coefficients. It requires four line buffers and this algorithm is suitable for low noise images only. Later, in [9] authors have contributed fuzzy based interpolation algorithms for image scaling in one system. Gaussian membership function can be invoked instead of linear membership functions. To reduce the computation complexity this algorithm uses four neigh boring pixels for estimating one pixel in scaled image. In [10] proposed bilinear interpolation algorithm along with clamp and spatial filtering as a pre processing stage to solve blurring and aliasing effects. The bilinear method is simplified by hardware resource sharing technique to reduce computing resources required. To interpolate missing color components in [11] proposed edge direction and local gain method. The basic bilinear along with adaptive edge direction and use of spatial filtering proposed low complexity image scaling in [12]. Later in [13] authors have contributed another approach with the help of clamp filter along with bilinear interpolation designed more efficient VLSI architecture. Along with T and Inverted T models are preferred to minimize the hardware computational complexity. In [14] authors proposed edge direction based low complexity image scaling processor using TMSC 0.18 um CMOS technology for 2D gray scale images. It requires one line buffer and more complex to extend it for color images. Super Resolution techniques are surveyed in [16] for further improvements.

III. PROPOSED IMAGE SCALING MODEL

A. Basic Concept of Scaling

The proposed image scaling approach uses area model rather than point pixel model in earlier approaches. In our approach we assumed each pixel in original image as a rectangular shape and pixel intensity is distributed entire rectangle area. Therefore, new pixel of scaled output image is obtained through weighted average of the original image pixel values with respect to coverage ratio.

The region of scaled image pixel is calculated based on size of the filter window. Fig 2. Represents the basic area pixel image scaling model where left side image shows original 4X4 image after performing scaling the output image of size 8X8 shown on right side.

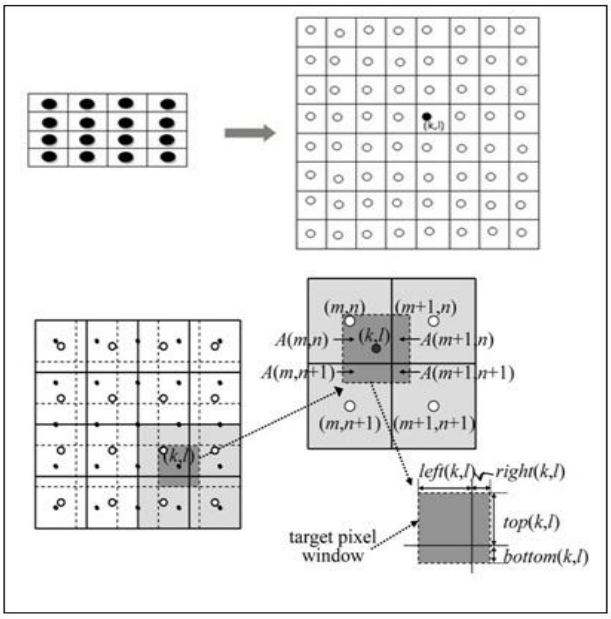

Figure 2. Illustration of basic image area-pixel scaling technique. (a) Original image of size 400X400 (b) Scaled image of size 800X800 pixels (c) Various relationships between pixels.

The proposed algorithm can take the original image is of size 400X400 pixels as input and produce scaling up to 800X800 pixels without loss of any visual quality. The area of original image must be less than the area of the scaled image. If (k,l) is the target pixel location having four neigh boring pixels such as left, right, top and bottom respectively and is expressed in terms of weighted average of area wise pixel luminance values is as follows . Let the luminance values of four neigh bouring pixels represented as

$$P_S(m,n), P_S(m+1,n), P_S(m,n+1), P_S(m+1,n+1) \text{---- (1)}$$

The estimated scaled image pixel intensity value can be

$$\widehat{P_T}(k,l) = \sum_{i=0}^{1}\sum_{j=0}^{1}[P_S(m+i.n+j).W(m+i,n+j)] \text{--- (2)}$$

Where $W(m,n), W(m+1,n), W(m,n+1), W(m+1,n+1)$ represents weight factors neigh bouring source pixel (k,l). Let the regions of four overlapped areas of source neighboring pixels on scaled image of target pixel can be expressed as $A(m,n), A(m+1,n), A(m,n+1), A(m+1,n+1)$ respectively. Let the width and height of four overlapped regions of $A(m,n)$ can be denoted as left (k,l) and top (k,l) and the width and height of $A(m+1,n+1)$ can be right (k,l) and bottom (k,l) respectively. In order to evaluate the above equation for four neighboring pixels will require more floating point operations.

B. Proposed VLSI based Image scaling

The basic relations between original and scaled image pixels and also calculated area wise weighted average of pixel intensity values. In our proposed design we use simple approximation of weighted area averages to compute the target pixel value. The block diagram of the proposed image scaling algorithm described in fig.3. The proposed algorithm can apply for both RGB color and monochromatic gray scale images simultaneously. The selection and type of input image to be scaled up will be selected with the help of MATLAB based graphical user inter phase (GUI).

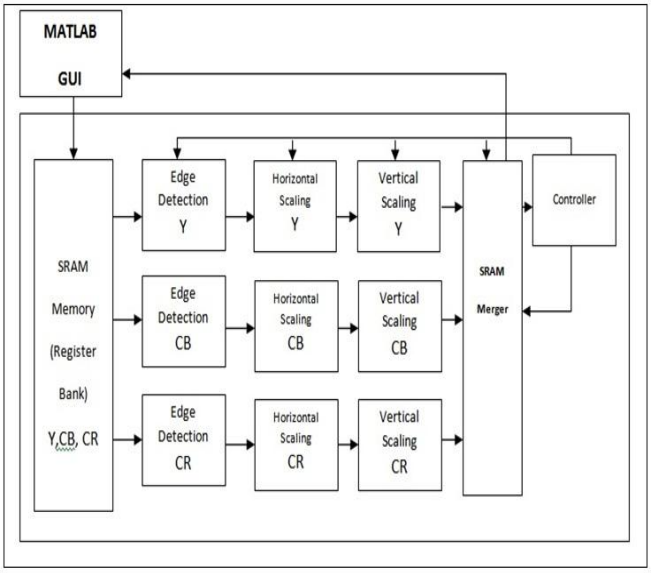

Figure 3. Flow diagram of proposed edge based image scaling algorithm

C. Algorithm Design flow

a. Provide the input images to MATLAB GUI for conversion of Image data to HEX conversion, it will provide Y (luma) and Chrominance (CB, CR).
b. Read the HEX file data and loaded in Memory of 400x400(Y), 200x200(CB), 200x200(CR), then generate the Start pulse.
c. Once Start pulse will latched High, the Controller will read the data, and processing to find the H-Sync and V-Sync, and Edge synchronization.
d. After Edge Synchronization the data will provided to Horizontal Scaling.
e. Horizontal scaling will averaging the data of luminance (Y) in size of 400x400 to 800x800.
f. After Horizontal Scaling, the Vertical Scaling will sampling the data of Chrominance (CB, CR) in size of 200x200 to 400x400.
g. After Vertical Scaling, the controller will find the V-Sync pulse, the Start the SRAM Merger, to merge the luminance and Chrominance, and generate the Hex conversion file.
h. The MATLAB GUI will read the Hex conversion file, and compare with a input file, and provide the corresponding value of PSNR and SSIM.

IV. RESULTS DISCUSSION

Synthesis of a system can be described as process of transforming behavioral description to structural/ gate level description. Recently high level synthesis (HLS) can make the design simple and more optimized[15]. HLS is a potential solution to improve the productivity level of FPGA based real time image processing applications. The proposed image scaling algorithm can bridge the gap between typical image sensors with display sizes up to 800X800 resolution level. The performance of proposed algorithm can be by taken various test images of size is 400x400 on 28nm CMOS technology based Artix-7 FPGA device with speed grade of -2, clock rate of 100MHz, input supply voltage is at 1.05 V and load capacitance of 10 micro farads.

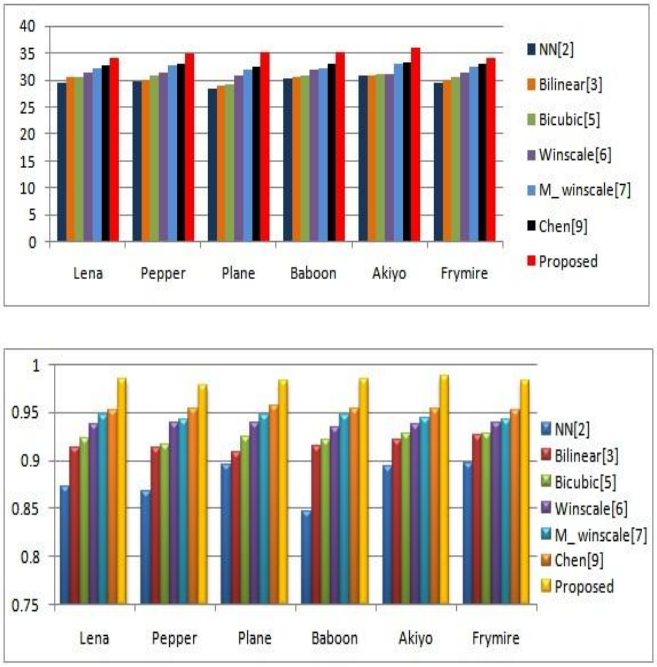

Figure.4. (a), (b) Comparison of PSNR, SSIM for different test images with existing methods.

To evaluate the earlier low complexity edge based image scaling algorithm we selected MATLAB tool with PSNR and SSIM are the evaluation parameters. In this case, we consider fixed size of input test images and can scaled up to 800x800 resolution level. Earlier works NN[1], Bilinear[2], win-scale[3], modified win scale [5], edge oriented algorithms[10] are compared with our proposed edge preserving image scaling algorithm. Finally, PSNR and SSIM are calculated for both test images and scaled images. SSIM is the parameter which will give similarity between two images. Fig 4. (a & b) shows the comparison of PSNR and SSIM values with respect to existing works. Table1,2 shows the comparisons of proposed VLSI based architecture resource utilization summary for both gray scale and color images respectively. The algorithm is designed using Verilog HDL language and simulated for functionality verification later synthesized and implemented for Artix-7 PRO FPGA device. The operating clock frequency is 100MHz we selected for better performance. High level synthesis implementation of RTL Level schematics are shown in figure 5 and 6 respectively.

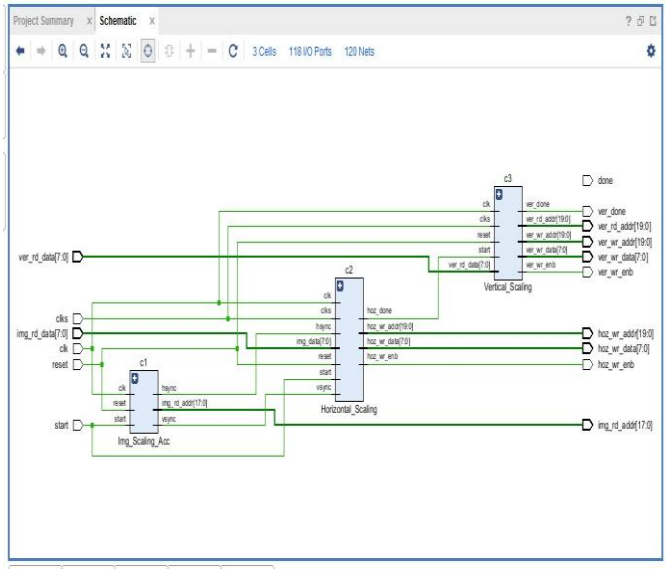

Figure. 5. RT Level schematic of proposed gray scale image scaling system.

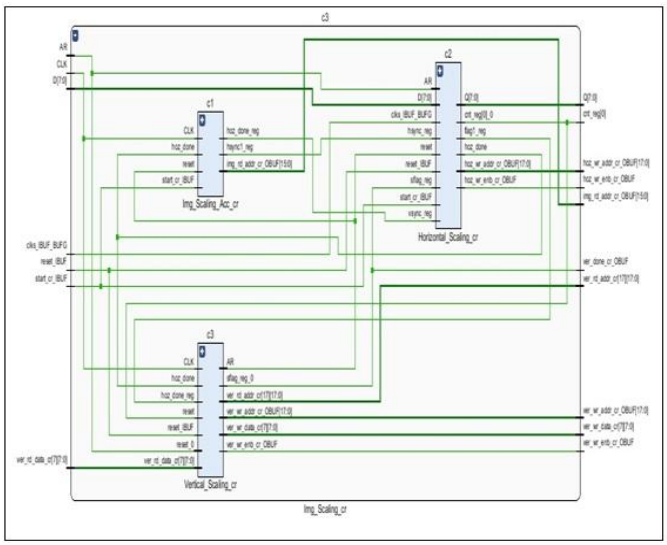

Figure 6. RTL schematic of proposed color image edge preserving image scaling system.

Figure 7. Test images of size 400X400 same for both gray scale and color image scaling.

Fig 7. Shows selected test image set, these images are RGB color images with image depth of 8 bits per color channel. For color image scaling process, not required any conversion mechanism. Both subjective and objective tests are performed by employing evaluation parameters like peak signal to noise ratio (PSNR) and structural similarity index measure (SSIM).

Table 1. PSNR and SSIM Comparison of different methods.

Image	NN[2]		Bilinear[3]		Bicubic [5]		Winscale[6]		M_ winscale [7]		Chen[9]		Proposed	
	PSNR	SSIM	PSNR	SSIM	PSNR	SSIM	PSNR	SSIM	PSNR	SSIM	PSNR	SSIM	PSNR	SSIM
Lena	29.48	0.8726	30.45	0.9123	30.56	0.9234	31.23	0.9378	32.04	0.9467	32.58	0.9522	34.12	0.9845
Pepper	29.65	0.8672	30.02	0.9124	30.78	0.9157	31.27	0.9384	32.78	0.9419	32.94	0.9537	34.84	0.9767
Plane	28.46	0.8954	28.92	0.9076	29.12	0.9238	30.81	0.9396	31.95	0.9472	32.41	0.9567	35.15	0.9824
Baboon	30.27	0.8466	30.47	0.9141	30.86	0.9219	31.92	0.9349	32.15	0.9468	32.94	0.9542	35.17	0.9837
Akiyo	30.68	0.8941	30.92	0.9215	30.97	0.9269	31.12	0.9372	32.94	0.9433	33.11	0.9538	35.98	0.9868
Frymire	29.47	0.8976	30.12	0.9267	30.57	0.9276	31.48	0.9397	32.56	0.9418	32.87	0.9519	34.17	0.9827
Avg	29.67	0.8789	30.15	0.9157	30.47	0.9232	31.31	0.9379	32.4	0.9446	32.8	0.9538	34.91	0.9828

Table 2. Performance metrics of various scaling algorithms

Parameter	Bi-cubic	Winscale	M_Win	Chen	Proposed
FPGA Device	Vertex-II PRO	NA	NA	Vertex-II PRO	Vertex-II PRO
Line Buffers	6	1	1	1	1
Area	890 CLBs	29K Gates	NA	1.06K	867 LUTs
Clock Rate(MHz)	100	65	55	142	100
CPU Time(ms)	3.5	4.74	5.6	2.17	2.9
Dynamic Power(mw)	NA	NA	NA	NA	17.349

Table 3. Performance of proposed image scaling process to scale up to 800X800.

Parameters	Gray Scale Image	Color Image
Target FPGA	XC7a200tfgg676-2)	(XC7a200tfbg676-2)
On chip power	17.349 Watts	31.466 Watts
CPU time	2.9 Secs	4.0 Secs
Area	344 LUTs	867 LUTs
Voltage	0.95V-1.05V	0.95V-1.05V

V. CONCLUSION

In this paper, the efficient edge oriented image scaling algorithm (EEOISA) with VLSI architecture is proposed which can scale image up to 800X800 pixels. The main contributions of this paper include: keep edge information through the edge oriented filtering approach; works well for Gray scale and RGB images, hardware resource utilization is reduced by employing approximation computations and increase the resolution levels along both directions. The proposed algorithm can scaling images up/down up to 75 % without degradation and blurring across the edge boundaries. Proposed EEOISA algorithm designed through Verilog HDL and synthesized and is optimized on Artix-7 FPGA device (XC7a200tfbg676-2) at 100 MHz through Vivado 2018.1 HLS design.

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