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Design of Low Power Delay Cell for Wide Tuning Voltage Controlled Oscillator for Frequency Synthesis Applications

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Abstract: ***This paper reports delay cell for Voltage Controlled Oscillator. The new circuit is designed and simulated in UMC_18_CMOS, 180nm process with 1.8V supply using Cadence tool. Main focus of this design is to achieve low phase noise and less power consumption. Proposed design is 4 stages differential ring VCO. The simulation results are presented with frequency range 2.3 to 4.7 GHz and Power consumption is 7.704 mW at maximum oscillation frequency with phase noise of -91dBc/Hz at offset of 1MHz and -120 dBc/Hz at offset of 10MHz. These results are back annotated to the model and accurate model in verilog-A has been presented.***

Index Terms: Cadence, Delay cell, Differential ring, Phase noise, Voltage controlled oscillator.

I. INTRODUCTION

The use of wireless products has been quickly increasing day by day and there has been global growth of new designs to fulfill the demands of this increasing market. Problems related with wireless communication systems have become severe with the advance of cellular telephony and the wireless data networks. Advance radio architectures and circuit designs are being actively needed that to get maximum stages of integration, less noise and low power operation for various applications and implementation of integrated circuits. Fractional-N frequency synthesis using of ∑- Δ modulation technique is one of technique to design frequency synthesizers with high-resolution and quick settling times [1-4]. To generate a programmable output frequency, these frequency synthesizers are used [5-6].Voltage Controlled Oscillator (VCO) based on ring oscillator is an essential part of the integrated frequency synthesizers because of its easy integration and wide tuning range [7-10].VCO is probably the element with more restrictions in the frequency synthesizer because it defines the tuning range and gain being an important parameter for the design. Besides, the VCO along with the frequency divider are the most power consuming circuits in the frequency synthesizer. To design VCO, frequency range, phase noise, power consumption, and die size are main challenges [10-12]. To overcome these issues lots of designs for VCO have been proposed. VCO based on ring oscillators, which is
generally used in the integrated frequency synthesizers, is one of the solutions. The overall performance verification of a frequency synthesizer is done by VCO[6].

II. VOLTAGE CONTROLLED OSCILLATOR

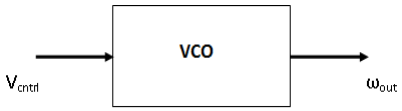
The VCO is a feedback circuit whose closed loop transfer function makes possible to amplify its own noise in a controlled form up to a stable oscillation state
The VCO is a feedback circuit whose closed loop transfer function makes possible to amplify its own noise in a controlled form up to a stable oscillation state. The VCO can be modeled as two port network H(s) feeded back with G(s). The closed loop transfer function is given by-

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1 - G(s)H(s)}$$

The circuit oscillates when the denominator of this transfer function is zero and the open loop gain is enough to maintain the poles in the imaginary axis of the root-locus plane. The situation can be resumed in the Barkhausen's criteria.

$$|G(j\omega_0)||H(j\omega_0)| = 1$$
$$\angle(G(j\omega_0)) + \angle(H(j\omega_0)) = 0$$

A Voltage Controlled Oscillator is a circuit whose output is periodic time varying signal having a semi-square or close to sinusoidal shape whose frequency can be controlled by control voltage at the input. VCO and its output response is shown in Fig. 1



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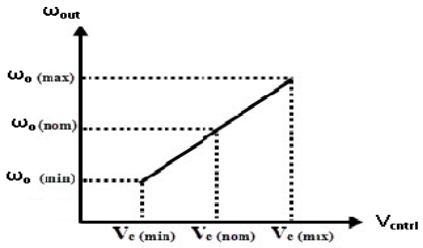

Fig.1: VCO and its response

The output frequency ωosc can be expressed as:

$$\omega_{osc} = \omega_o + K_{vco} * V_{cont} \quad (1)$$

Where ωo is a free running frequency, Vcont is a control voltage input from charge pump, Kvco is the gain or sensitivity of VCO

Output of VCO can be expressed as[6]:

$$V_{out}(t) = A * \sin(2*phi*\int(\omega_{osc})) + V_{offset} \quad (2)$$

where A and V_{offset} is amplitude and offset voltage respectively.

III. Phase Noise and Jitter

The term phase noise is generally used for relating short term arbitrary frequency fluctuations of a signal. Its time domain analysis is known as jitter. The phase noise and the spurious tones are the critical parameters which decide the performance of a VCO. Phase noise in oscillators is mainly due to thermal and or flicker noise(1/f).

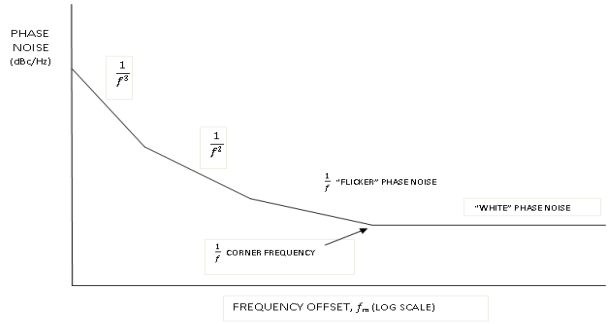

Fig. 2: Phase noise spectrum of an oscillator.

The phase noise spectrum of Lesson model shown in Fig. 2 This spectrum can be divide in different regions. At high frequency offset it is flat and noise added is due to noise floor mainly. At relatively small frequency offset where slop is -20dB/dec, added by device noise mainly. At small offset, flicker noise is dominating factor and slop is -30dB/dec. The noise of $1/(\Delta f)^2$ region is given by[10]:

$$L_{\min}\{\Delta f\} \approx \frac{8}{3\eta}.N.\frac{kT}{P_s}\left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}}\right).\frac{f_0^2}{\Delta f^2} \quad (3)$$

Equation (4) gives the relationship between $1/(\Delta f)^3$ noise and 1/f noise. Corner frequency between $1/(\Delta f)^3$ and $1/(\Delta f)^2$ sections expressed as:

$$f_{\frac{1}{f^3}} = f_{\frac{1}{f}}.\frac{3}{2\eta N}.\frac{A^2}{1-A-A^2} \quad (4)$$

Where, N is number of stages R_L is load resistance, I_{tail} is tail current, and V_{DD} supply voltage.

Where A Shows symmetry between the rise and fall time of the VCO output.

IV. Proposed Design

In delay cell of VCO given in Fig. 3, M1 and M2 are input transistors and M5, M8 are the input transistors with negative skewed inputs. M5 and M6 are used as controlled active loads whose gate voltage is controlled by a control voltage [9]. M1 and M2 together frame the main loop and M5 and M6 frame the minor loop. Primary inputs are connected with outputs of the last stage and the output of previous to last stages feed the secondary inputs. Transistor M9 or M10 will pre-charge the output nodes results in fast charging of output node at high voltage result in high oscillation frequency. M3 and M4 are PMOS transistors compose a latch. Because of latch, on time of delay cell of transistors is get reduced which additional reduces the phase noise. Transistors M5 and M6 are connected to control voltage Vc to control the feedback of the latch.

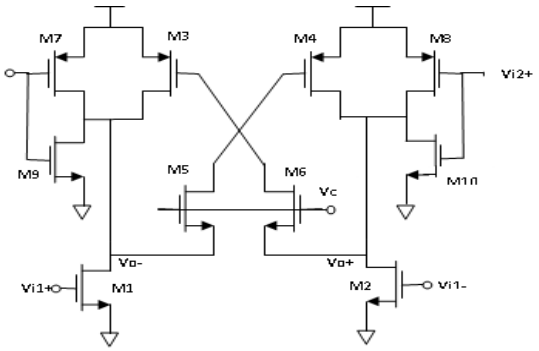

Fig. 3: Delay cell[9]

In this design[9], when input common level, Vincm changes, result in change in bias currents of M1 and M2, results in deviation in transconductance of the devices which further change in the small signal gain while the departure of the output common mode level from its ideal values lowers the maximum allowable output swing. In proposed design authors have used a tail transistor M11as a solution of this problem as shown in Fig. 4. M11 suppress the effect of input common level on operation of transistor M1 and M2 and output level. Delay cell with constant bias current have better noise immunity.

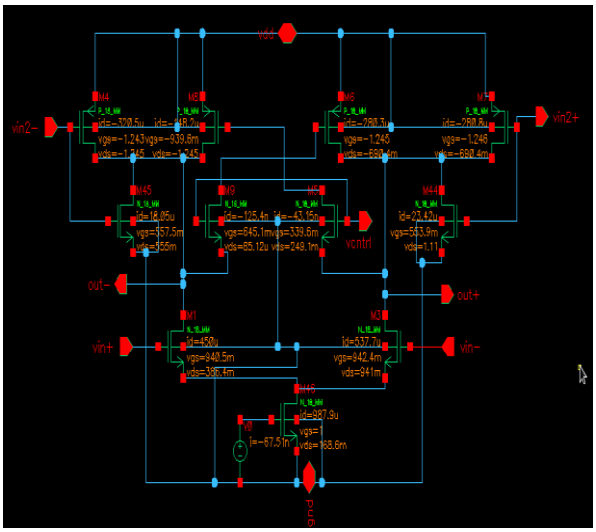

Fig. 4: Proposed delay cell

In the VCO identical delay cells are connected as shown in Fig 5. The output of this cell will be fed to the input of next delay cell. This process of feeding the next delay cell continues until the last delay cell whose two differential outputs are then feedback to the inputs of first delay cell, but in a cross-coupled way.

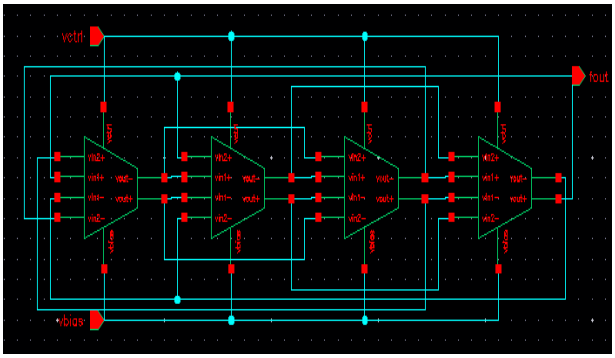

Fig. 5: Schematic Diagram of 4 stage Ring VCO

Fig. 5 shows a ring VCO with cascading four stages delay cells. Normal delay path and negative twisted delay path used to attach the delay cells has been used. Both outputs out- and out+ of delay cell are connected to primary inputs Vin+ and Vin- of next stage, this connection builds normal delay path. Secondary inputs Vin2+ and Vin2- are connected to inputs of second next stage, this connection builds skewed delay. This advance signal turns on the PMOS during the change in output and balance the performance of the PMOS. This correction improves the rise time of the output and resulting in reduction of phase noise of the overall VCO. This design has reduced number of stages with increase in frequency of operation. Reducing number of stage can increase operation frequency. The mathematical relation for Vin+(t) and Vin-(t), are given in equation (5) and (6), in terms of the unknown frequency, f. Vin+(t) and Vin-(t) will be 180° out of phase.

$$V_{in+}(t) = V_{DD} - \frac{V_{sw}}{2}(1 - \sin(2\pi f t)) \quad (5)$$

$$V_{in-}(t) = V_{DD} - \frac{V_{sw}}{2}(1 + \sin(2\pi f t)) \quad (6)$$

resulting in the expression for Vout+(t) in equation (7)

$$V_{out+}(t) = V_{DD} - \frac{V_{sw}}{2}(1 + \sin(2\pi f t - \pi(1 + \frac{1}{N}))) \quad (7)$$

The final frequency expression for the VCO is given in equation (8).

$$f = \frac{I_{ss}}{2NV_{sw}(C_{in}+C_{gdp})} \quad (8)$$

V. MODEL OF VCO

An ideal VCO produces a periodic output whose frequency is linear function of control voltage at the input. The function of VCO can be defined by equation (1) and (2). Model of VCO using verilog-A is given below without and including the Phase noise and jitter. Results of transistor level simulation of the this proposed VCO is than back annotated onto the verilog-A model. This model is useful to precisely predict phase noise behavior of VCO.

VCO without jitter/phase noise:

```
'include "disciplines.h"
'include "constants.h"
module vco ( in, out ) ;
inout in, out ;
electrical in, out ;
parameter real vdd = 1.8, // operational voltage
amplitude = vdd/2, // amplitude of output
offset = vdd/2, // offset of output
gain = 3.6e9, // Kvco gain [Hz/V]
vnom = 0.75, // nominal vin freq ;
fnom = 2.4e9; // frequency at vnom
analog begin
    freq = fnom + gain*(V(in) - vnom) ;
    V(out) <+ amplitude*cos(2*`phi*idt(freq)) + offset ;
end
endmodule
```

VCO with jitter/phase noise:

```
'include "disciplines.h"
'include "constants.h"
module vco ( in, out );
inout, in, out;
electrical in, out;
parameter real Vlow=0;
parameter real Vhigh=Vlow+1 from (Vlow:inf);
parameter real Fl=1 from (0:inf);
parameter real Fh=2*Fl from (Fl:inf);
parameter real Vlow=0.5, Vhigh=1.8;
parameter real tt=0.1/ Fh from (0:inf);
parameter real jitter=0 from [0:0.25/Fh);
parameter real ttol=30n/Fh from (0:1/Fh);
real freq, phase, delT, delta;
integer z, seed;
analog begin
@(initial_step) begin
seed = –456
freq = (V(in)–Vlow)*(Fh – Fmin) / (Vhigh – Vlow) + Fl;
delta = delta/(1–delta); freq = freq*(1+delta);
phase = 2*‘M_PI*idtmod(freq, 0.0, 1, 0.5);
end
@(cross(phase+‘M_PI/2, +1, ttol) or cross(phase –‘M_PI/2,+1, ttol))
begin
delT = 1.414*jitter*$dist_normal(seed,0, 1);
end
z = (phase >= –‘M_PI/2) && (phase < ‘M_PI/2);
V(out) <+ transition(z ? Vhigh : low, 0, tt);
end
endmodule
```

Design has been completed in cadence environment with 180nm Technology and simulated. Simulation results and layout of VCO are reported in this paper. Fig. 6 shows variation of frequency with respect to different input control voltages.

Most of the region is linear. Authors have observed the range of frequencies between 2.3 to 4.7 GHz with control voltage 0.1 to 1V. The gain of VCO (Kvco) is 3600 MHz/V. This high Kvco will give better improvement in loop bandwidth with better phase noise response.

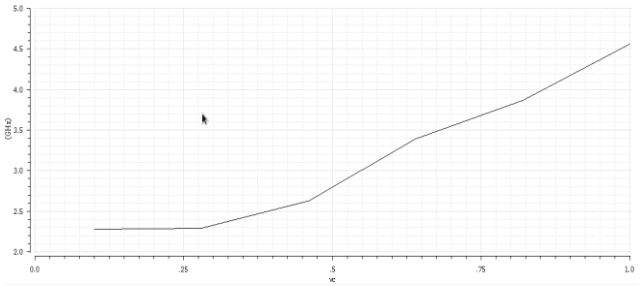

Fig. 6: Frequency range for different control voltage of Schematic

Fig. 7 shows output oscillation of reported ring VCO and obtained output is about 2.4 GHz at control voltage = 0.5v.

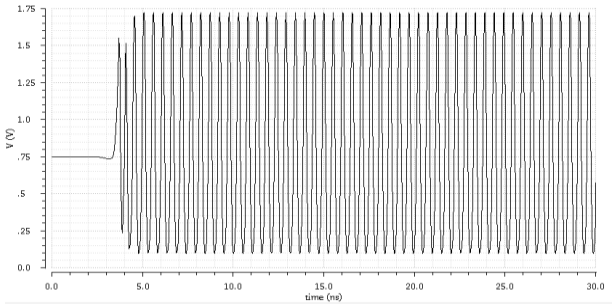

Fig. 7: Output of VCO at control voltage 0.5V

Fig. 8 shows output phase noise of proposed VCO. This curve has maximum frequency range is 10MHz with offset from carrier. Authors have observed the phase noise value at 1MHz offset is about -91dBc/Hz and it is -120dBc/Hz at 10MHz. Authors have also observed that Phase noise can be reduced by increasing tail current with higher power dissipation.

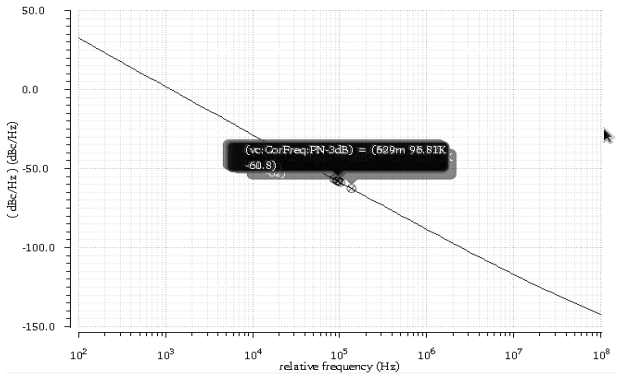

Fig. 8: Phase noise response of VCO

Fig. 9 shows the layout of proposed 4 stage ring VCO. This proposed VCO occupies 2078 µm2 area.

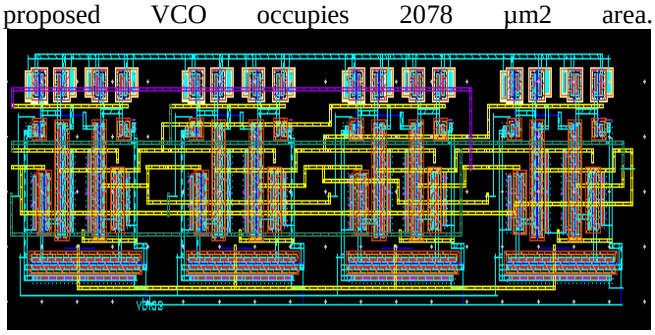

Fig. 9: Layout of proposed 4 stage ring VCO

Finally authors have compared the reported results with earlier published similar work and improvement are obtained as shown in table 1

TABLE 1 Comparition of earlier work with this work

	REF [11]	REF[12]	THIS WORK
Technology	0.18um CMOS technology	0.18um CMOS technology	0.18um CMOS technology
Power supply	1.8 V	1.5 V	1.8 V
Frequency range	3~5.6 GHz	0.5~2.54 GHz	2.3 ~ 4.7 GHz
Area	0.7X1.1mm^2 (chip area)	9280 µm^2 (VCO Core)	2078 µm^2
Power consumption (mW)	9	2.47	7.7
Phase Noise(dBc/Hz)	-80.56@1MHz	-118@10MHz	-91@1MHz -120@10MHz

VII. CONCLUSION

In this paper we have designed a delay cell of the for differential ring VCO using dual delay path technique. This design decrease the transient time to attain wide frequency range, low phase noise and less power consumption. The simulation results are reported with operating frequency range is 2.3 to 4.7 GHz. Power consumption is 7.704 mW at maximum oscillation frequency with phase noise of -91dBc/Hz at offset of 1MHz and -120 dBc/Hz at offset of 10 MHz. Simulation results are than back annotated in a verilog-A model of four stage ring VCO.

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REFERENCES

1. C. Weltin, E. Familier, and I. Galton "A Liberalized Model for the Design of Fractional Digital PLLs Based on Dual-Mode Ring Oscillator FDCs" IEEE Transaction on Circuits and Systems-I, Vol. 62, No. 8, pp 2013-2023,August15
2. Miletic and R. Mason "Bandwidth Expansion in Sigma-Delta PLLs Using Multiphase VCOs" Canadian Conference on Electrical and Computer Engineering, 2006.
3. B. De Muer and M. S. J. Steyaert, "A CMOS monolithic sigma-delta-controlled fractional-N frequency synthesizer for DCS-1800," IEEE J. Solid State Circuits, vol. 37, no. 7, pp. 835-844, Jul. 2002
4. C Y Chen, J J Ho, W R Liou, R. Y. Hsiao "A 5.2GHz CMOS fractional-n frequency synthesizer with a MASH delta-sigma modulator" Symposium on Circuits and Systems, 2008. .
5. Miletic and R. Mason "Quantization noise reduction using multiphase PLLs" IEEE International Symposium on Circuits and Systems ISCAS, May 2006
6. Verma, Virendra; Misra, D. K. ; Gamad, R. S. "Comparative analysis of frequency sysnthesizers" International J. of Electronics and Communication Engineering .Vol. 2, Issue 4, Sep 2013, pp95-104
7. Hao Wei ; Wang Pinglian ; Zhao Hui "The design of an efficient satellite IF PLL PM demodulator with low complexity" International Conference on Computational Electromagnetic and Its Applications, Proceedings, pp: 316 – 319, 2004
8. C. Chung and C. Lee, "An all-digital phase-locked loop for high-speed clock generation," IEEE Journal of Solid-State Circuits, vol. 38, pp. 347–351, Feb. 2003.
9. K. H. Cheng,S. Kuo, and C.M. Tu, "A Low Noise 2.0 GHz CMOS VCO Design" in Proc. IEEE Midwest Symposium on Circuit and Systems, pp. 205-208, Dec03
10. D. B. Leeson, "A simple model of feedback oscillator noise spectrum," proc. IEEE, Vo. 54, pp.329-330, Feb 1966.
11. A.Tsitouras, F. Plessas, "Ultrawideband, low-power, 3–5.6GHz,CMOS voltage controlled oscillator" Microelectronics Journal vol. 40, 2009, pp897–904
12. J. Jalil, M. B. I. Reaz, M. A. S. Bhuiyan, L. F. Rahman and T. G. Chang; "Designing a Ring-VCO for RFID Transponders in 0.18 µm CMOS Process" Hindawi Publishing Corporation, the Scientific World Journal, Volume 14, Article ID 580385, 2014.

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