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Design of Improved Current Differencing Buffered Amplifier for Analog Signal Processing

Mohammad Faseehuddin, Jahariah Sampe

Abstract: ***this paper presents an improved design of current differencing buffered amplifier (CDBA) capable of performing both current mode and voltage mode operations. The improvised flipped voltage follower based current input stage of CDBA offers very low input resistance of only 12.31Ω for considerable frequency range. The voltage follower stage also performs almost rail to rail and exhibits an extremely low output resistance of 3.55 Ω. The circuit is designed in 0.18 µm TSMC technology and the performance of the proposed circuit is examined using H-Spice. The current transfer bandwidth is found to be 67.9 MHz while the Voltage follower bandwidth is 161MHz. The circuit operates at a reasonably low supply voltage of±0.6V while dissipating 0.63mW of power.***

Index Terms: CDBA, Current Differencing Unit, Voltage Buffer,

I. INTRODUCTION

The proliferation of battery operated portable devices, wearable biomedical equipment and the recent internet of things (IOT) have made it a necessity to develop devices working under low voltage and low power regime (LVLP) [1-5]. The current mode approach for LVLP design is found to be superior to the voltage mode approach. The current mode circuits enjoy numerous advantages over their voltage mode counter parts; they have wide bandwidth, low power dissipation, high linearity, simple structure, high slew rate, consume less chip area and are less affected by supply voltage scaling [2, 5. 6]. Numerous current mode devices have been proposed in the last few decades. The most popular among them are the second generation current conveyor (CCII) [2], current differencing buffered amplifier (CDBA) [7], current differencing transconductance amplifier (CDTA) [8] and current feedback operational amplifier [9] etc. After its introduction by Toker [7] the CDBA has emerged as a versatile building block for the synthesis of filters and oscillator circuits. Several proposals can be found [10-13] discussing the implementation of filters and oscillators. It is found that CDBA is capable of realizing both current mode and voltage filters with minimum number of passive components. Many implementations of CDBA can be found in the literature both in bipolar and bulk CMOS [11, 13]. The LVLP implementation of CDBA based on flipped voltage follower (FVF) can be found elsewhere [13]. The previously proposed FVF based CDBA was excellent for low voltage design but had the current input resistance of 56 Ω contrary to the ideal zero value and was also limited in accuracy.

This paper presents a new CDBA implementation with modified FVF based current differencing unit (CDU) with reduced input impedance and a new voltage buffer with higher input impedance and extremely low output impedance. The section II gives a brief description of CDBA followed by the section III giving the design methodology. The simulation results are presented in section IV followed by conclusion.

1. Description of CDBA

The CDBA can be considered as a cascade of unity current follower and unity voltage follower cells. The former designed as current differencing unit (CDU) and the latter as voltage follower. The CDBA and its equivalent circuit are shown in Figure 1(a-b). It has two low impedance current input terminals n and p and a high impedance z terminal which follows the difference of input current. The voltage output terminal w follows the input voltage at terminal z. Ideally, terminals n and p being current input terminals should have zero input impedance and z being current output terminal should have infinite impedance. Furthermore, terminal w must have zero output impedance. The V-I relationship of CDBA is given by Equation below.

$$I_Z = \alpha_p I_p - \alpha_n I_n, \quad V_w = \beta_v V_z, \quad V_p = V_n = 0$$

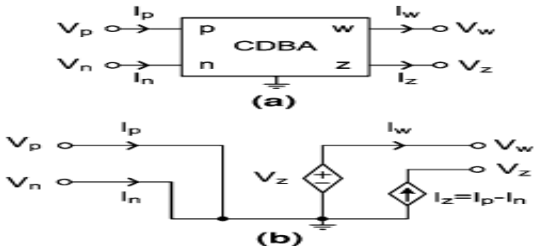

Figure 1. (a) The block diagram of CDBA (b) Equivalent circuit

2. Implementation of improved CDBA

The FVF is found to be a very useful cell for low voltage design [14]. The flipped voltage follower current source (FVFCS) exhibiting very low input resistance is proposed in [14].

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The structure is used by [13] for designing the current subtractor. In this research an attempt is made to further reduce the output resistance of FVF by addition of only two extra transistors. The FVF circuit is shown in Figure 2. The FVF is formed by transistors M_1, M_2 and a current source I_{B1}. The output resistance of the FVF is given in Equation (2) and can be calculated using the expression for output resistance of FVF [14].

$$R_x \cong \frac{2}{g_{m1}g_{m2}r_{02}} \quad (2)$$

In order to further reduce the output resistance of the FVF a regulated cascode approach is utilized [15]. The transistors M_2 and M_3 forming the regulated cascode biased by a current source M_4 are added to the FVF structure as shown in Figure 3. Now the output resistance becomes extremely low being further reduced by a factor of $g_{m2}r_{03}$. The use of only two additional transistors results in negligible increase in power and area. The value of the reduced resistance is given by Equation (3)

$$R_x \cong \frac{2}{g_{m1}g_{m2}r_{02}g_{m3}r_{03}} \quad (3)$$

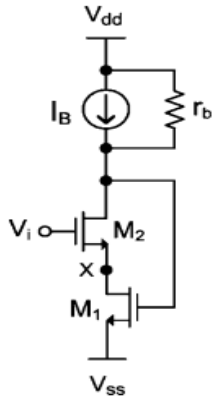

Figure 2: The conventional FVF

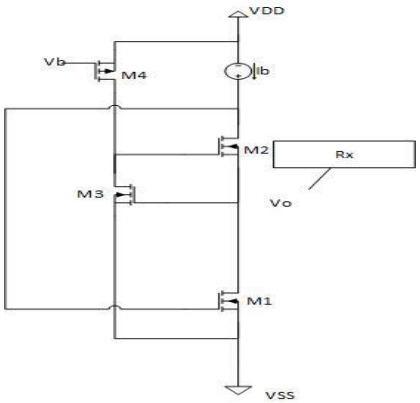

Figure 3. The improved FVF with extremely low output resistance

The CDU is implemented using the improved FVF cell. Considering saturation region operation and that the transistors (M_1- M_4), (M_5 – M_6), (M_7 – M_{10}), (M_9 – M_8) and (M_{11}-M_{12}) are matched. The operation is as follows: The current source, I_{B1} forces equal current in the transistors (M_1–M_4). Thus, equalizing the gate to source voltages of the transistors, this in turn results in voltages of the two input terminals becoming zero. The PMOS transistors (M_5-M_6) perform current subtraction while the combination of cascode transistors (M_9-M_7) and (M_{10}-M_8) reduce the input impedance as explained earlier. Figure 4 shows the schematic of the CDU. The resistance looking at the terminal-z is given in Equation (4).

$$R_z \cong \frac{r_{03}}{r_{06}} \quad (4)$$

The voltage follower is implemented utilizing a tailless differential pair (M_{15}-M_{16}). To reduce the output impedance a feedback connection is implemented with transistors (M_{17}-M_{18}) the value of the output resistance is given in Equation (5). The voltage follower is highly linear and has wide dynamic range. The complete schematic of the improved CDBA circuit is shown in Figure 5.

$$R_{out} \cong \frac{2}{(g_{m17}+g_{m18})g_{m16}(r_{013}//r_{015})} \quad (5)$$

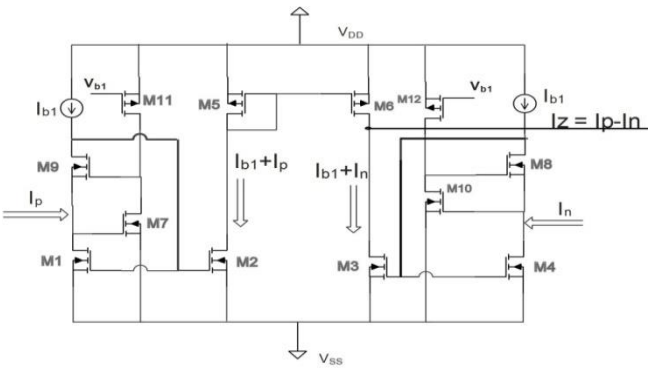

Figure 4. The schematics of the Current Differencing Unit

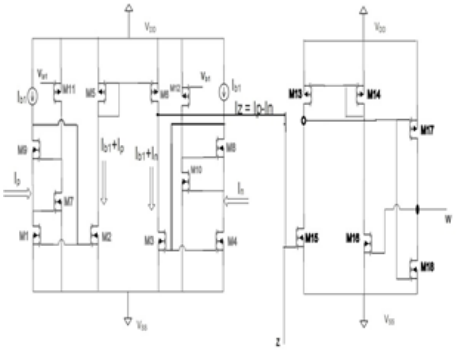

Figure 5. Complete CMOS implementation of CDBA

3. Simulation results

The Improved CDBA circuit is designed in 0.18µm TSMC technology to evaluate its performance. The aspect ratios of the transistors are given in Table1. At first the CDU was simulated to measure the input impedance. The impedance was found to be extremely low at 12.31 Ω till 10 MHz and remained within acceptable limits for almost 100 MHz thus proving the theoretical analysis. The dynamic range of current output was ± 50 µA for a bias current of 56 µA. The range can be further extended by increasing the bias current. Hence a compromise is to be made between the input range and power dissipation. The input impedance of CDU for different frequencies is plotted in Figure 6 and the variation of I_z with current I_p and I_n is shown in Figure 7.

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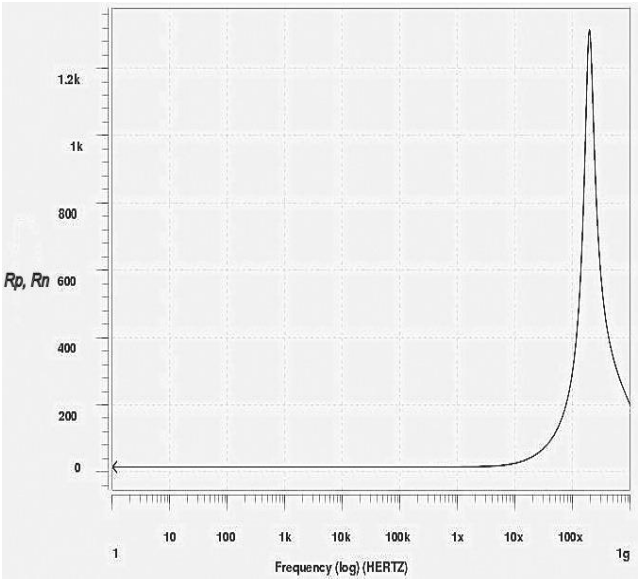

Figure 6. Input impedance vs. frequency of CDU

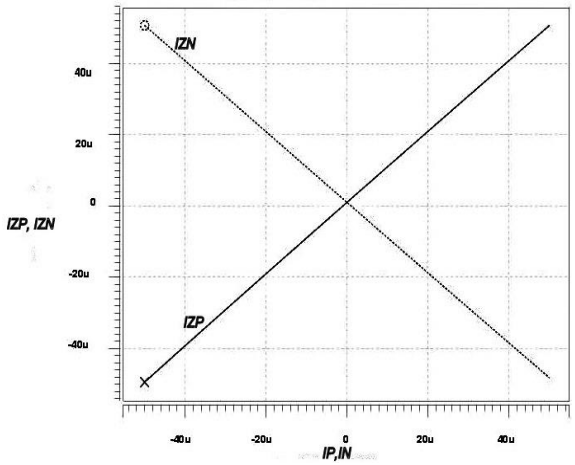

Figure7. Current transfer characteristics of CDU

The voltage following characteristics and the output impedance of the voltage follower is shown in Figure 8 & Figure 9. The AC transfer bandwidths of the Improved CDBA are given in Figure (10-11). The -3dB bandwidths for I_z/I_p, I_z/I_n and V_w/V_z are 67.9 MHz, 67.9 MHz and 161MHz respectively.

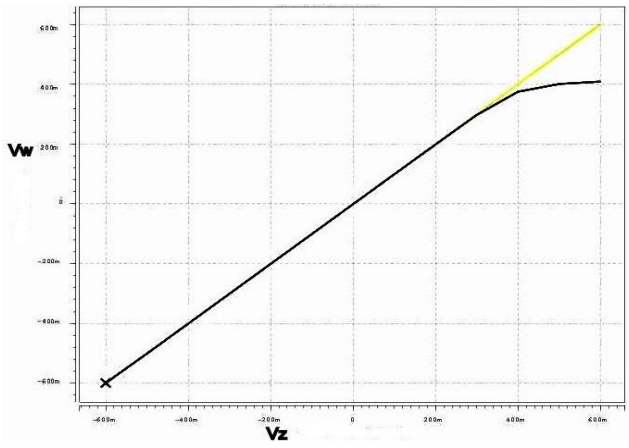

Figure 8. The voltage transfer characteristics

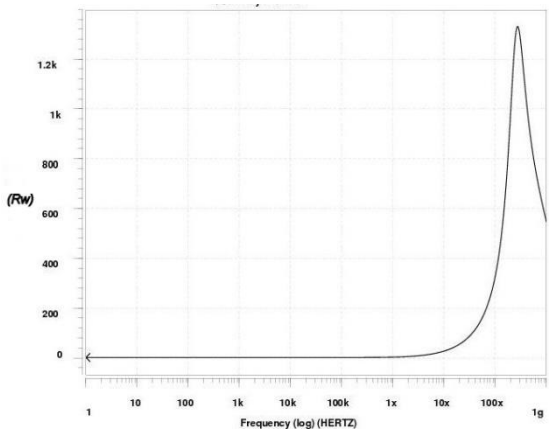

Figure 9. Voltage follower output impedance vs. frequency

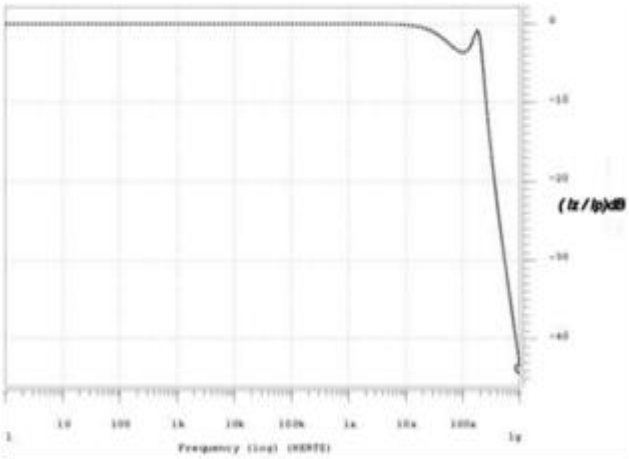

Figure 10. The AC current transfer bandwidth

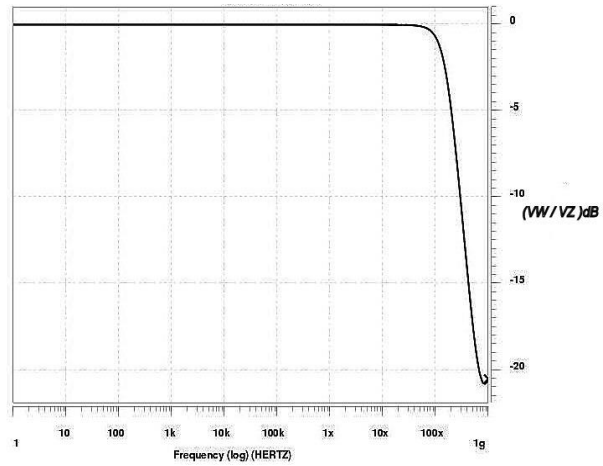

Figure 11. The AC voltage transfer bandwidth

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Table 1. Aspect ratios of the transistors

Transistor	W(μm)	L(μm)
$M_1 - M_4$	3.6	1
$M_5 - M_6$	240	1
$M_7 - M_{10}$	60	1
$M_8 - M_9$	180	1
$M_{11} - M_{12}$	120	1
$M_{13} - M_{14}$	60	0.36
M_{17}	240	0.72
$M_{15} - M_{16}$	30	0.36
M_{18}	120	0.72

Table 2. Performance parameters

Supply voltage	±0.6
Power dissipation	0.63mW
Input current range	±50μW
Output voltage range	-600mV to +400mV
Input resistance (R_p, R_n)	12.31Ω
Output resistance	3.55Ω
Current transfer bandwidth	67.9MHz
Voltage transfer bandwidth	161MHz

II. CONCLUSION

In this paper an improved extremely low input resistance current differencing buffered amplifier is presented. The circuit utilized improvised FVF based current differencing unit and a differential pair voltage follower with low output resistance. The circuit was designed in 0.18μm TSMC technology and simulated in HSPICE. The circuit operated at a low supply of ±0.6 V and consumed 0.63 mW of power. The CDBA exhibited wide current and voltage dynamic ranges. The terminal resistances of CDBA were R_p= 12.31 Ω, R_n=12.31 Ω and R_w=3.55 Ω. Finally, the circuit can be utilized in developing high performance filter and oscillator topologies.

III. ACKNOWLEDGEMENT

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