Performance Evaluation of Re-Configurable VLSI Architecture based on Finite Impulse Response Interpolation Filter

Raja Krishnamoorthy, P.T. Kalaivaani, Puvirajan Thirumurugan

ABSTRACT--- ***The implementation of a two-stage improvement procedure for modelling a reconfigurable VLSI Structure .In this work an Finite-impulse -response interpolation filter and the Multi-standard digital up converter(DUC) are used to reduce limit its power and area consumed in the proposed .In this strategy is mainly minimize the number of multiplications for every input samples with an addition of each samples are compared with the individual applied in each standard filter. While design the specific usage of each level root-raised-cosine conduit and FIR filter with multi standard DUC are determined with three different stages. During the supplementary period, a two-bit based Binary common sub expression (BCS) based eliminating algorithm are presented in this model for providing effective constant multiplier ,which are all fundamental components for various filters. This methodology has been effectively perform with minimizing the area and the power consumption of the system ,with progress an operating frequency of a three-bit Binary common sub-articulation (BCS) technique details are provided in this study, along with the better performance an modelling of multi-standard Digital up converter are Efficiently used in VLSI architecture.***

Keyword: Root-Raised-cosine, Digital up converter (DUC), FIR interpolation filter, Coefficient sector generation module (CG).

I. INTRODUCTION

The requirement of dissimilar high data transfer rates and the high channel are limits by various operational techniques of the contemporary varied driven by a media transmission industry are produce an impression of SDR. As per software defined-radio mentions to a single device are fit for associate every one of the given increasing guidelines which are available further in accessible communication stage.

Reconfigurable and low many-sided quality is a dual strategic conditions with partial drive responseFinite-impulse -response filterchannels utilized in several structural remote communication system [1].Software defined-radio desires FIR filter by means of animatedly programmable channel constant. For theFinite-impulse -response channel increase and complete between single particular adaptable (the information) and a few amounts of the factors are recognized as multiple constant multiplications MCM [2]. The low power and area beat forming FIR channel for advanced up converter were composed. In the current framework, the no good twofold regular sub-articulation based paired basic sub-articulation disposal calculation [3].With a digit-restructured limited drive reaction Finite-impulse -response filterdesign with an acceptable granularity [4].

FIR channel has extensive amplitude varieties in info information with its factors. Allowing for the abundance of mutually channel and its factor sources of info [5].Distributed Arithmeticprocessing elements, they are conceivable with lessen the recollection estimate, yet then again that prompts expanding of snake many-sided quality and the idleness [6].

In the subsequent stage, a 2-bit twofold normal BCS -based sub expression end Formulation should be used for the design with an effective are consistent multiplier or, in other words, component of any channel [7-10]. In a SDR framework, various norms are recognized For single chip system[11]generous of coded network choice channel with the base-band stage[12] It have been used for symmetrical coordinate form architecture , adjusted measured scheme, isolated marked handling design, and changed standard marked digit (CSD) approach are limited drive responseFinite-impulse -response channel to improve the power application. Notwithstanding, the decrease in power proficient are interchange concerning the speed activity creates this plan unsatisfactory with a software defined radio system.

A lesser area use has been utilized for multiplier-lessFinite-impulse -response interpolator [13].

Expert consumption of query tables in this outline decreases the power and region contrasted and the regular FIR channel execution. On account of higher request channel usage, this architecture neglects to accomplish low energy as a result of an expansion in the ROM estimate.

FIR channel structure, the Multiplication distribution multiplier is proficiently utilized minimum multifaceted system of the Finite impulse channel. The primary thought of Computation sharing multiplier (CSHM)are express to increases Finite impulse sifting activities mix with include and move tasks completed regular calculation results in [14].

To defeat the impediments of the past work, we proposed a quick introduction channel calculation and the relating equipment engineering in [15], for a spare the encoding interval and lessen multifaceted compute nature fragmentary movement estimation in HEVC. The outline of the broadcast crosswise of an advanced correspondence modem dependent on the utilization of specific DUC where baseband preparing

Revised Version Manuscript Received on 25 November, 2018.

Raja Krishnamoorthy, Professor, CMR Engineering College, Department of ECE, Kandlakoya Villaga, Hyderabad, Telangana, India.

P.T. Kalaivaani, Associate Professor, Department of ECE, Vivekanandha College of Technology for Women, Tiruchengode, Namakkal, Tamilnadu, India.

Puvirajan Thirumurugan, Assistant Professor, Department of Electronics and Communication Engineering, CMR Engineering College, kandlakoya Villaga, Hyderabad, Telangana, India.

is performed by an elite DSP and up conversion to Intermediate Frequency (IF) is achieved [16-17] by a FPGA based plan.

Likewise, recipient lateral of the advanced correspondence, Digital down Converter (DDC) is utilized.

The plan enhancement of various dimensional completely pipelines registering configurations region time interval-control proficient execution Finite impulse channel filter by systolic decay of (DA)- based inward item calculation {17-18].

Multiplier less limited motivation reaction (FIR) channels [20-21] investigate essential sub-expression sharing when the channel coefficients are upgraded. Raja et al [22] and [23] have designed of a, low power ECG signal processor for wearable health system-review and implementation issues and spike detector for fully Integrated Neuro modulation SoC. Raja and Saravanan [24] and [25] have proposed pipelining shared component architecture in FIR filter. The problem is solved by storing the preceding input in a shadow latch. If any error occurs the data will be read from the shadow latch. Even though the number of components increases by this method, the error is reduced. The flushing time is reduced by more than 50%. The shadow latch requires a separate clock.

II. LITERATURE REVIEW

R. Mahesh et al.,(2010) presented two new reconfigurable and its arranging of low unpredictability FIR channels are alluded, to be specific, consistent movements procedure and programmable movements technique. It is a general point of view for low multifaceted nature reconfigurable channel channels. Sathya. C et al., (2015) The first thought a two-advance positive thinker method and it is demonstrating of a recompose VLSI structure with an interjection channel for Multi Excellence of duc to limit the power and zone Expenditure. Anni Benitta.M and Felcy Jeba Malar.M et al. (2016), Modulated an outline used in multi-standard binary up converter to decrease the Energy consume, deferral with the zone utilization. For an imperative of this plan is the understandable find the root A.P. Vinodet al. (2013), with a general system is chiefly executed FIR channels for SDR recipients utilizing a few adders. A math strategy, recognized as pseudo of adrifting point portrayal to express in the code the channel constants. Kuna-Hung Chenet al. (2006) tobuild up alowest control bit wised recompose Finite impulse response channel with exceptional harshness. It assigns a flexible yet compacted and low-control system for Finite impulse response channel channels through with the thin spread of accuracy and in particular area.

III. BACKGROUND METHODOLOGY

A) Interpolation

"Introduction," in the DSP recognize, the processing are verified by the following filters. (Mainly the operation of filter is removes the spectral images) As a long methodology, the DSP sensing interpolation is rather is differential from the "math" feeling of insertion. However, the result is significantly related to set up "in the middle of" referred motion from the first signal. The outcome is as though inspected increase signal at first at the higher rate.

The essential needs to add is to enhance the testing rate at the yield of the single framework with the goal that another system working at a higher inspecting rate can provide a source of the signal.

Fir Interpolation Factor

The interpolation factor is straightforwardly proportion of the output amount to each source rate. It is by and large represented by "L," so yield rate/input rate=L.

The FIR Interpolation square re-tests the discrete-time contribution at a rate L times quicker than the information test rate, where L is the whole number esteem is particularize for the Interpolation factor parameter.

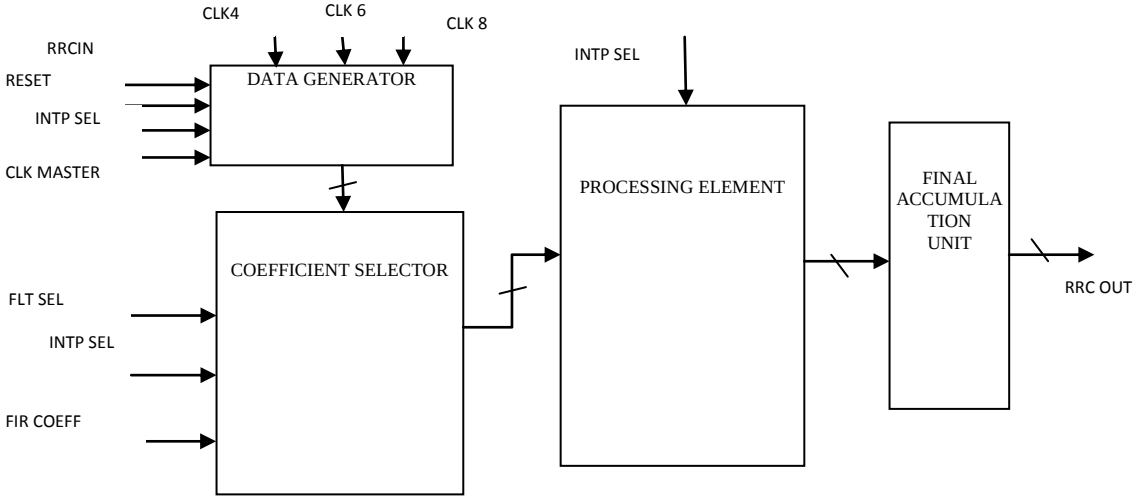

Fig. 1: Block diagram for proposed RRC Filter

B) Root Raised Cosine Technique (RRC)

The raised-cosine Filter is a channel successively utilized for pulse forming in computerized adjustment because of its capability to decrease between image obstructions. {\displaystyle H_{rc}(f)}

The architecture of RRC FIR Filter

Root Raised cosine FIR channel, and its structure assumes an essential job in multi-correspondence measures mainly general portable media transmission, Narrowband frequency separation For numerous advancements and especially in broadcasting visual propagation for its capacity to limit the bit mistake rate by not alluding the planning jitter at the testing immediate.

C) Data -generator (DG)

The interpolation characteristic for the common telecommunication standard is 8 for 49 tap filter, 16 for 97 tap filter, 4 for 25 tap filter. Includes with an interpolation factor, the data generators block samples the input data sequence Root raised cosine clock input (RRCIN) and generates subfilter required for the different tap filters such as 25, 49, and 97. For example, if 25tap filter is used then the subfilters as are essential for their implementation to be 25/4, i.e., seven sub filters.

D) Coefficient sector generation module (CG)

The CG is the structure delivers an expansion activity concerning the information sources also channel level. The two-organize improvement strategy is utilized in this CG hinder for disentangling the RRC FIR channel with the Economic calculation time and with low confusion. The Flowchart of the coefficient generator (CG) Block appears in Figure, and its execution is portrayed as pursues.

For N tap channel with an insertion factor L Needs (N/L) number of convolution working framework also, it requires the number of architectural adders for the new working. On the off chance that O, N, M tap channel with addition factor L, P, Q needs an expansive number of practical examination and more auxiliary adders for their Execution. From this time forward for a constant state engendering delay, the territory and power utilization enhances with an ascending in a few multipliers and auxiliary adders. For this, the appraisal is finished by First coding Pass (FCP) square. In this FCP, channels adjusting just with the channel factors are continued over the 2:1 MUX wherever the control stricture disregarded move factor lean toward the passband channel.

- To decide channel coefficients from the First Coding Pass square are transmitted with the second coding pass square.
- A contingent of the interpolation factor, filter coefficients are coded correspondingly.

At that point, the increased activity and its working traits are characterized between the information and channel coefficients chose from Second Coding Pass square (SCP). For large product generation, Binary Common Subexpression Elimination Technique (BCSE)is utilized for evacuating the most widely recognized sub-expressions inside the coefficients.

The multiplexer unit chooses the yield created from the move and includes square contingent on the coded coefficients. The expansion activity can be executed by summing every one of the returns of the halfway item generator pursued by eight multiplexer units.

The necessary information from the coefficient generator square is controlled to the last gathering unit as per the insertion factor parameter. The reconfigurable passband signal forming FIR channel depends on transposed straightforwardly from its structure.

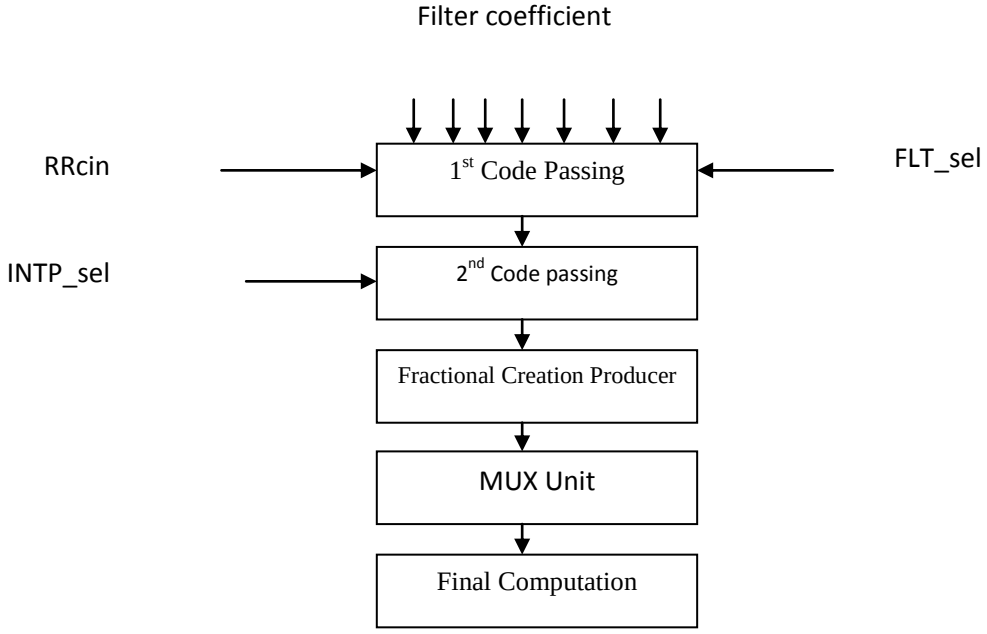

Fig. 2: Flowchart of the coefficient generator Block

E) BCSE Algorithm

BCSE manages and evacuating the repetitive Binary Common Sub expressions (BCS) that happen to incorporate the coefficients. The Binary Common Subexpression Elimination procedure decided for taking out repetitive calculations in coefficient generator MUX are reforming the significantly recognized

paired piece designs BCSE available elements. A number of bit number can be frame $2N\,(N+1)$ BCS between Each other. In the example, a 2-bit paired portrayal can make just a single BCS, or, in other words".

These BCSs can be defined as $11 = Y1 = (Y + 2 - 1Y)$ where Y is the information flag. Another portrayal, for example, 00, 01 and 10 does not require viper for the execution as they have zero and just a single non- zero piece is available.

To have minimum ISI (Inter-image impedance), drive response with the communicate network, channel reaction and gather channel desires to fulfilNY Quist ISI foundation. Raised-cosine channel is the best channel response is profoundly dependable for this standard. Half of extrication is handled sending lateral, and half is complete corporate side. The Receiving end, the station response, on the inedible casual that it very well may be Exactly Reduced, similarly be taken into Range with the goal that the general response is Raised-cosine channel.

F) DUC (Digital up Converter)

A DUC is an advanced circuit which changes a digital baseband signal to a passband wave. The source baseband signal is examined at a generally low testing rate, reliably the tweaking computerized image rate. The bandpass signal is shifted and changed over to a most extreme testing rate convoluting modulating a direct digitally synthesized (DDS) bearer recurrence.

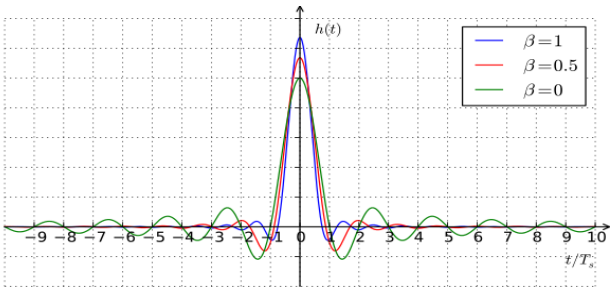

Fig.3: The impulse response of a Root-Raised Cosine Filter

G) SDR (Software Defined Radio)

SDR is a broad casting media transmission System wherever the component which had to be present commonly Implemented in apparatus (e.g., Filters, indicators, radio, modulators/demodulates, Mixtures, and so forth.) are then again actualized using programming on a PC or install the system. While the proposed of SDR isn't new, the quick build up the capacities of computerized hardware renders various effective procedures which used to be just for study investigation.

An essential SDR framework may comprise of a PC furnished fora comprehensive card system, or another DUC system, Introduced by specific Radio frequency at the initial stage. Critical measures of frequency wave preparing remain given to the universally useful system; ideally, it is done in different reason equipment (Microelectronic Models). Each of a model delivers signals can get and communicate generally regulating SDR conventions (interim it alluded to as signals) in light of on the product utilized.

Software radios have basic utility for the different application and PDA benefits, all of this must give an extensive mixture of changing SDR signal conventions in the present analysis.

With a high expression, programming characterized SDR signals stay regular with an example comparable the SDR Forum (Radio signal transmitting system) to end up cutting-edge innovation in frequency. SDRs, alongside programming characterized reception apparatuses, are the empowering influences of the radio. New radio items are logically given in the market by utilizing the general stage design performed in details. It limits the improvement esteem because the product can be re-utilized for the activity.

The time and cost for running exhibitions and support can be lessened because of the bug settling inside the radio is in administration. It tends to be used in remote correspondence. It applies to speak with anybody whenever in any way. Programming redesign naturally is done and new highlights embedded. Remote programming downloads enhance the limit.

IV. PROPOSED METHOD

A) Processing elements

In this work, we use adder and multiplexer. (Data register file, arithmetic/logic unit (ALU), a multiplier and a shifter are some processing elements).

B) PPG Unit

The Modified and enclosed technique is utilized to creating an intermediate product amid with formulation activity in relation to the information Yin and the channel coefficients.

Binary Common Sub expression Elimination system, Fulfilment for a regular sub-articulation utilizing movement and include strategy disposes of the primary term moment in a factor. In the present structure, two-bit BCSE going beginning Zero to eleven over with this enunciated stage. For the most part, utilized four of these BCSs, a viper is requested just for example 11. This advances a decrease in equipment and change in speed while playing out the duplication task.

In this BSCE strategy, the shift and include based method will be utilized to create the fractional item which will be computed by using the accompanying strides for delivering the last augmentation result. The decision of the extent of the BCS will characterize the quantity of halfway items. In the proposed calculation, the layer-1 and the 2-bit twofold normal sub-articulations (BCSs) are extending from 00 -11 will be considered, which will create four halfway items. Be that as it may, inside the four of these BCS, a single turn will be required to develop the halfway object just for example —11, and whatever is left of the item will be made by modified hardwired. AND with a factor of the 16-bit system, eight incomplete item 17-15 -13- 11-9- 7- 5, 3 bits partial generator8-partial generation 1are produced and it is

correct moving of the main halfway product(P8) by the bits 0, 2, 4, 6, 8, 10, 12 and 14 individually.

Expansion unit works like the errand of summing every one of the outputs with the partial product generator square pursued in 8 MUX

portion. Adjusting structure of adders is indicated in various parallel loads. Mainly outcomeFor the 8 MUX viz M7– M0 remain included performed agreeably. Result From the last viper throughput of a double equivalent Model. From the previous outcome the expansion element relies upon every maximum bit ratio factor.

In the present Finite impulse response channel, the coefficient generation square is utilized to control legitimate information between the last gets together square contingent upon the comparing introduction factor factors. It takes the source from the CG square.

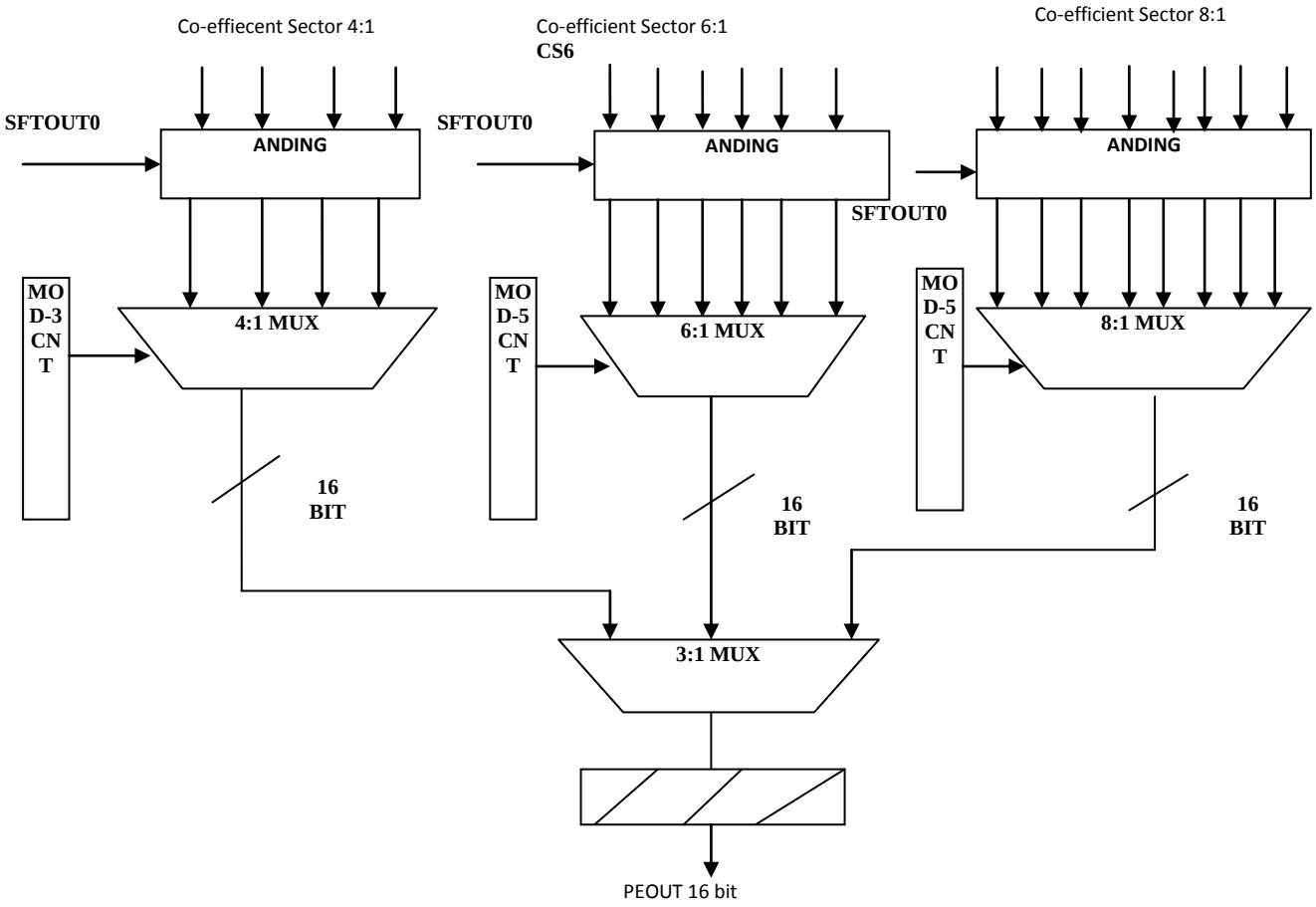

Fig. 4: Hardware model of the co-efficient sector Block.

The MUX channel will be considered to choose the correct information delivered from the partial thing generator unit which will depend on the coefficients of the advanced esteem. At layer-1, eight 4:1 multiplexer is required to give fractional items as per the 2-bit BCSE calculation. The width of these eight multiplexers is 13, 9, 17, 11,5,15 which more, three bit each ideal with each of 16 – bit for each Fractional thing, between all of this will be Minimize the power then equipment utilization.

The Partial Produces PP which creates since the 8 gatherings of two-bit BCS's are additional with the last augmentation solution using will perform in multi-section. The structure of controlled expansion at layer-2 is given in [5]. As indicated by the BCSE calculation, the proposed two-layer needs the 4 option A1-A4 tasks to include the 8 Partial items; the controlled expansion activity is performed at the layer two on account of the proposed VHBCSE calculation. This location (A1-A4) will be overseen by relying upon the optimized signals (C1-C6), those will create dependent with the four-bit BCSE from the Control Logic Generator square.

The 4 MUX entirety results addition section up to 1-4 are created with the two-layer which is currently included in the three layers. Formulation of the, measured extensions are 29 performed, rather than the immediate expansion of these four outcomes will appear in Fig. Consequently, this expansion (A6) is controlled by the Control Signal (C7) from the CG square.

This obtain result are obstructed on four layer plays out the enlargement activity within the multi-output of addition section IV delivered by three layers to make the next increase result between all information and the performance Factor.

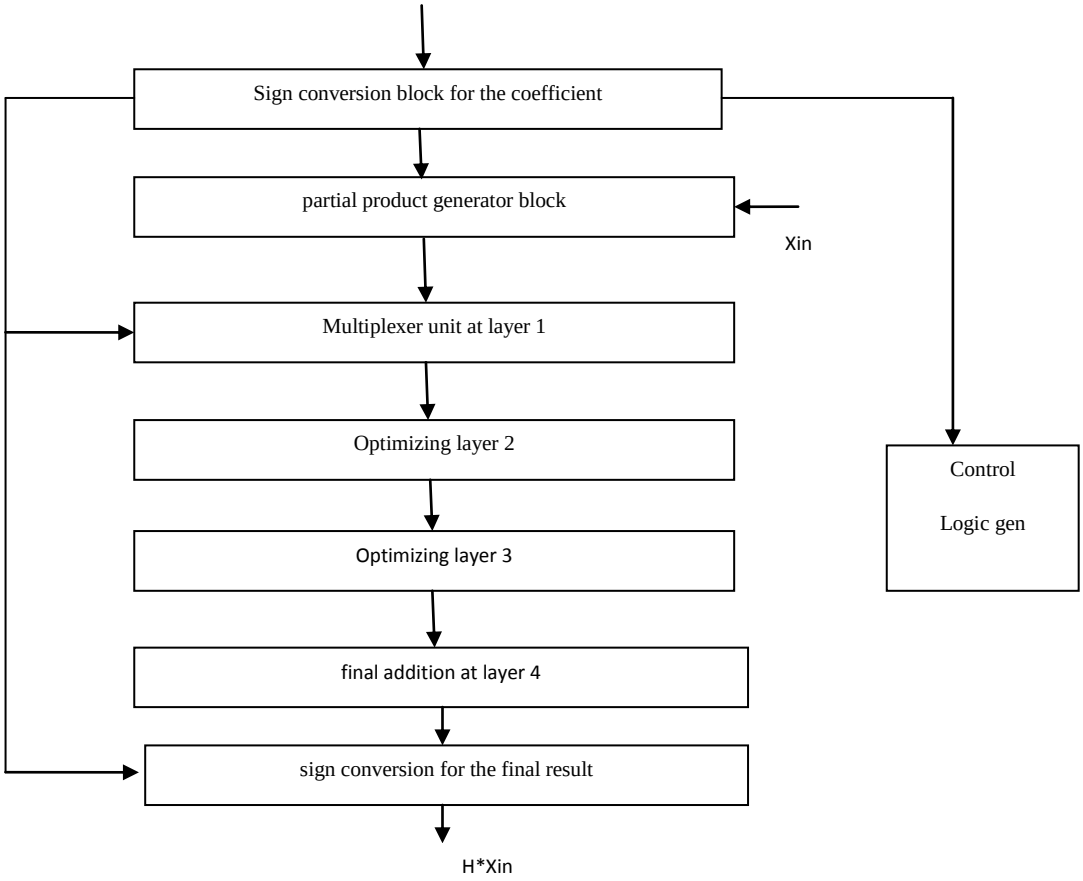

Fig. 5: Data Flow diagram of the Co-efficient Multiplier

V. RESULTS

A) Simulation Waveform

i) Simulation Waveform When soft computing filter SFT = 1:

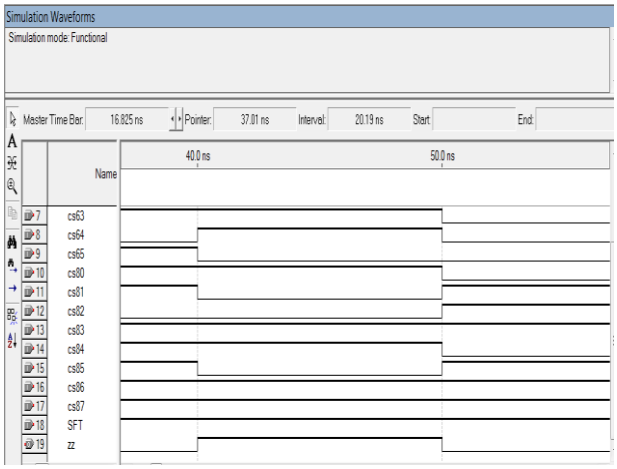

Fig. 6: Simulation Waveform When SFT = 1

From **figure 6** shows the soft computing filter =1 and its 16-bit channel based FIR filter digital architecture signal was obtained. This signal is used to minimize the noise level in the received signal. Then to simulate the final output binary results and to compute the circuit complexity, power, and the speed level.

ii) Simulation Waveform When SFT = 0;

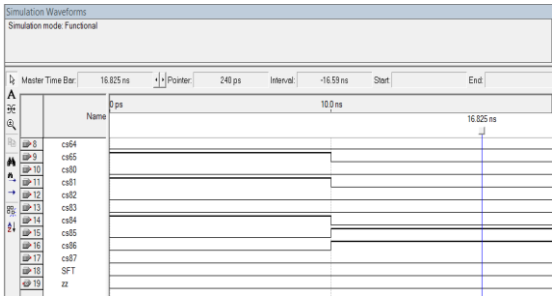

Fig. 7: Simulation Waveform When SFT = 0

Figure 7 When SFT =0, the multiplexer selects the output which it doesn't change any variant in the "ZZ" output stages.

B) Power Analysis

PowerPlay Power Analyzer Status	Successful - Sat Mar 11 12:32:56 2017
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	csblock
Top-level Entity Name	csblock
Family	Cyclone II
Device	EP2C70F672C6
Power Models	Final
Total Thermal Power Dissipation	202.39 mW
Core Dynamic Thermal Power Dissipation	0.03 mW
Core Static Thermal Power Dissipation	155.11 mW
I/O Thermal Power Dissipation	47.24 mW
Power Estimation Confidence	Medium: user provided moderately complete toggle rate data

Fig. 8: Power Analysis Of CS Block

From Figure 8, it is observed that the proposed algorithm

and its specific characteristics. Mainly, there is a desired concerning with the maximum frequency and area utilization. The proposed design low power.

C)RTL View

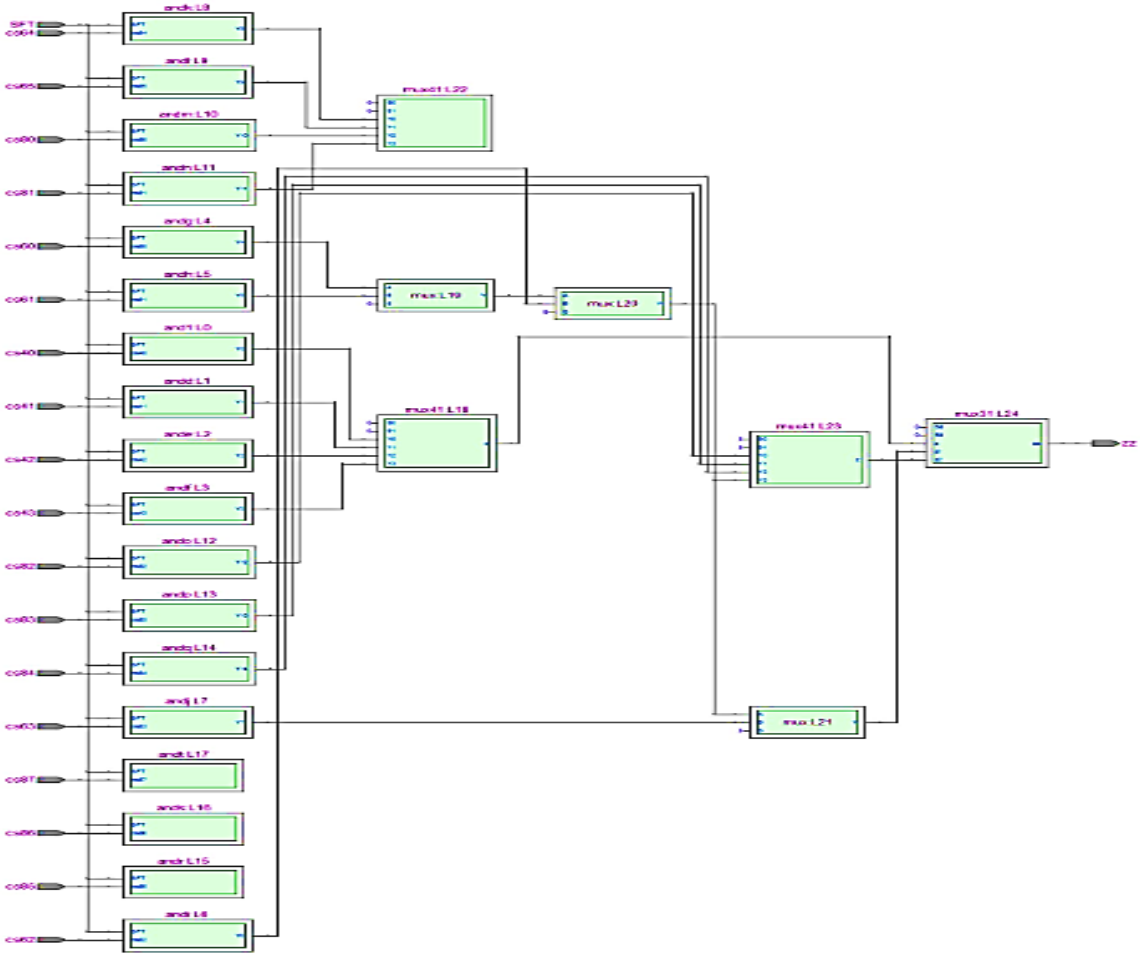

Fig. 9: RTL View of CS Block

Figure 9 shows the Proposed RRC filter is designed. The simulation and RTL are given below. Fig.16 shows the simulation result of the suggested RRC Finite impulse response filter. With its variable 'ZZ' gives the filter output with 'CS' being the input to the system. The variable helps to select the desired filter coefficient.

D) Timing Analysis

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	9.378 ns	SFT	zz	–	–	0
2	Total number of failed paths								0

Fig. 10: Timing Analysis of CS Block

Figure 10 shows the Timing analysis For the Co-efficient Sector mainly for a Worst-case TPD it seems the actual time =9.378ns for the output ZZ when SFT=1.

VI. CONCLUSION

This concise trends to differential issues experienced in planning the reconfigurable channel utilized in multi-standard DUC, or, in other words, the component of SDR/intellectual radio. This analysis likewise offers a solution for the issues by proposing a two-advance optimization procedure to optimize with desired FIR channel more capable by limiting area and power consumption enhanced in the most extreme operating frequency of the present model. Execution of consequences with the present design of every accessible recomposed Finite impulse response channel structures actualized on Control and additionally ASIC stage exhibits the benefits of the proposed architecture in regards to performance, energy and area utilization. Mainly recommended configuration is by all accounts strikingly appropriate for the Future design of a Multi-excellence of restructured digital up converter with the software-defined ratio system are computed, and its working potential and region are better to improve.

REFERENCES

1. A. P. Vinod, R. Mahesh, "New Reconfigurable Architectures for Implementing FIR Filters with Low Complexity" Institute of electrical and electronics Engineering Tran in IC design, (volume.
2. 29, No. 2, February 2010).
3. Anni Benitta.M, Felcy Jeba Malar.M, and "Design and Analysis of Efficient Reconfigurable FIR Filter Using Constant Multiplier Architecture" Pp.: 0976-1353 VOL 20 ISSUE: 3 2016.
4. Sowmiya.J, Sasikala.G, Sathya.C "Area optimization Technique for Multi-standard DUC" Journal in electronics and communication Engineering VOL 2 ISSUE: 3 2015.

5. Tzi-Dar Chiueh, Kuan-Hung Chen, "A Low-Power Digit-Based Reconfigurable FIR Filter,' Institute of electrical and electronics Engineering Trans on Circuits and systems VOL. 53, NO: 8, 2006.
6. Jongsun Park, Seok-Jae Lee, "A Reconfigurable FIR Filter Architecture to Trade off Filter Performance for Dynamic Power Consumption," Institute of electrical and electronics Engineering Transvery large scale integration VOL. 19, NO. 12, 2011.
7. Shrutisagar Chandrasekaran, Abbes Amira "FPGA Realization of FIR Filters by Efficient and Flexible Systemizatio nUsing Distributed Arithmetic" IEEE Trans on Signal Processing, VOL 56, NO. 7, JULY 2008.
8. Mr.S.Karthick, V. Sandhya, "A Survey of New Reconfigurable Architectures for Implementing FIR Filters With Low Complexity" ICCCI, Jan. 03 –05, 2014.
9. Indranil Hatai, Swapna Banerjee, "An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC" Institute of electrical and electronics Engineering Trans VLSI Systems, Pp., 1063-8210.
10. Manojkumar Reddy. Nali, "An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC"IJARECE (Volume 4, Issue 7, July 2015).
11. Naveen Kumar G. N. and L. P. Usha Sri, "Design and implementation of Pulse-Shaping FIR Interpolation filter using BCSE Algorithm"IJERT,(Volume. 4 Issue 05, May-2015).
12. S. Im, W. Lee,J. Chung, "Implementation of SDR-eared digital IF channelized de-channelize for multiple CDMA signals," IEICE Trans. Commun., vol. no. 6, Jun. 2000.
13. S.-F. Lin, S.-C. Huang, L.-G. Chen, "Power-efficient FIR filter architecture design for the embedded wireless system," IEEE Trans. Circuits Syst. vol. 51, no. 1, Jan. 2004.
14. Y. Son, K. Ryoo, Y. Kim, "1:4 interpolation FIR filter," IEEE Electron. Lett. vol. 40, no. 25, pp. 1570–1572, Dec. 2004.
15. Thamizharasan .V" An Efficient VLSI Architecture for FIR Filter using Computation Sharing Multiplier" International Journal of Computer Applications Vol 54– No.14, September 2012.
16. Wei Zhou, Xin Zhou" An efficient interpolation filter VLSI architecture for HEVC standard" Journal on Advances in Signal Processing 2015.
17. Jyothi.N," Design and VLSI Implementation of High Performance DUC and DDC for Software Defined Radio Applications" ICECSPCA 2013.
18. P. K. Meher, A. Amira, "FPGA realization of FIR filters by efficient and flexible systemization using distributed arithmetic," IEEE Trans. Signal Process. Vol. 56, no. 7, pp. 3009–3017, Jul. 2008.
19. J. Xie, J. He, and G. Tan, "FPGA realization of FIR filters for high-speed and medium-speed by using modified distributed arithmetic architectures," Micro electron. J., vol. 41, no. 6, Jun. 2010.
20. K.-H. Chen and T.-D. Chieueh, "A low-power digit-based reconfigurable FIR filter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, Aug. 2006.
21. D. Shi and Y. J. Yu, "Design of linear phase FIR filters with a high probability of achieving a minimum number of adders," IEEE Trans.Circuits vol. 58, no. 1, Jan. 2011.
22. Y. J. Yu , Y. C. Lim, "Optimization of linear phase FIR filters in dynamically expanding sub expressions space," Circuits, Syst., Signal Process., vol. 29. No. 1, 2010.
23. Raja, K., S. Saravanan, R. Anitha, S. Suganthi Priya, and R. Subhashini. "Design of a low power ECG signal processor for wearable health system-review and implementation issues." In Intelligent Systems and Control (ISCO), 2017 11th International Conference on, pp. 383-387. IEEE, 2017.
24. Raja, K., Saravanan, S., Malini, P., Raveena, V., & Praveena, R. S. (2017, January). Design of a spike detector for fully Integrated Neuromodulation SoC. In Intelligent Systems and Control (ISCO), 2017 11th International Conference on (pp. 341-345). IEEE.
25. Raja, K., & Saravanan, S. (2016). A New Clock Gated Flip Flop for Pipelining Architecture. Circuits and Systems, 7(08), 1361.
26. Saravanan, S., & Raja, K. (2016). Shared Processing Element Architecture for An Area and Power Efficient FIR Filter Design using Double Base Number System. Asian Journal of Research in Social Sciences and Humanities, 6(8), 2513-2520.

Authors

Dr. Raja Krishnamoorthy received his B.Tech. degree from Anna University, Chennai, India in 2007, M.Tech. degree from Anna University, Coimbatore, India in 2011 and Ph.D. degree from Anna University, Chennai, India in 2017. His main area of research activity is VLSI Physical Design, Wireless Sensor Networks and Biomedical Engineering. He has published many research articles in refereed journals. He is currently working as Professor and Research Associate Dean in the Department of Electronics and Communication Engineering at CMR Engineering College, Hyderabad, India.

Dr. P.T. Kalaivaani received her B.E degree in Electronics and Communication Engineering from Periyar University, Salem in 2004. She received her M.E degree from Anna University, Chennai in 2006 . She obtained her Ph.D degree in Information and Communication Engineering from Anna University, Chennai in 2018. She has 11 years of teaching experience. Her areas of research includes Wireless Sensor Networks, Network Security, Digital Image Processing, Neural Network, Digital Signal Processing, Cloud Computing, IoT. She is currently working as an Associate Professor in the Department of Electronics and Communication Engineering, Vivekanandha College of Engineering, Tiruchengode, Tamilnadu, India.

T .Puvirajan received the B.E. degree from Anna University, Chennai, India in 2009, M.Tech degree from JNTU Anantapur, India in 2014. He is currently working as Assistant Professor, Electronics and Communication Engineering Department, CMR Engineering College, Hyderabad, India. His research interests are in VLSI Signal Processing, Image Processing, Robotics.