A Hybrid Bio Sensing Medical Implantable Front End Design for Wireless Body Sensor Nodes and IoT Applications

Raja Krishnamoorthy, P.T.Kalaivaani

Abstract--- Internet of Things is the most popularly known creative phenomena of this century. It has gained a lot of popularity with the advancements in the internet technology. IOT is a platform where the user can connect everyday things entrenched with electronics, software and sensors to the international network, empowering them to accumulate and interchange the data. Owing to the development of IoT techniques, bio implantable circuits are becoming more and more popular which can monitor human health on a continuous basis. This paper presents the implementation of analog frontend circuits used in the bio sensing devices. The proposed design uses narrow swing current mirrors which occupy less area and perform considerably well in limited voltage conditions.

I. INTRODUCTION

Internet of things basically expands the affiliation of humans [1] to merge, subsidize, and collaborate to belongings around them. Citified sensors and chips are entrenched in the substantial equipments which are applicable daily, each broadcast precious data. This information leads to a perfect understanding of how devices or equipments work and work together. The diverse information is brought together through the Internet of Things [2-3].The common language is provided to all the devices and apps to broadcast with each other. The functioning begins with the devices themselves which securely broadcast with an Internet of Things stage. This platform merges the information from many devices and analytics are applied to share the most precious information with applications which can fulfill the industry-specific needs. This platform is also used by the manufacturer for creating and managing the applications, which are capable of solving the specific issues.

Fig. 1: IoT overview

One of the latest fields of application where IoT is being thoroughly researched is the implantable wireless body sensors [4]. The system-on-chips and the wireless body sensor nodes are highly implemented in personalize healthcare and adequate hospitalization for different disabilities like neural disorders, cardiac infarction, glaucoma, and sugar. Ultra power CMOS IC's were used in the architecture of nodes for the purpose of nodes utilization. These IC's are used for achieving and transforming the biopotential signals [5] in WBAN. This is applicable in real applications where the data is transferred to the protected mobile services. The figure below explains about the designing of conventional sensor nodule in a WBAN [6]encircle of bio-sensing analog front end (AFE), the analog-to-digital converter (ADC) is used for reorganizing the analog signals into digital signals, the digital signal processing core is used for digital processing, for managing the power resources and clock reset of entire chip the power management unit (PMU) is used, the data and the measurements are collected through the wireless telemetry section by a remote and receiving equipment transmits the data for monitoring. The surface electrodes capture the bio-potentialsignalsby means of bio-sensing AFE, which is a major censuring circuit block in the WBSNs [7] and implantable SoCs.

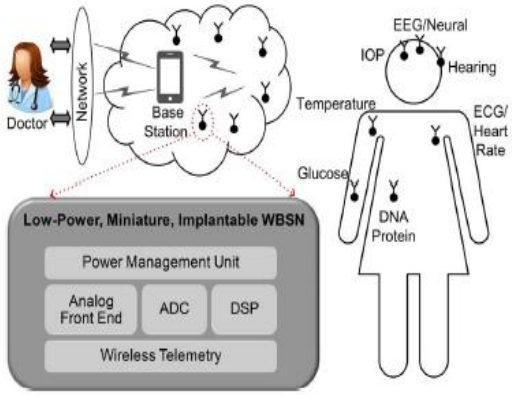


Fig. 2: WBNS forming a WBAN

The next image explains about the design compensations like (buzz, potentiality, area, dimension, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), offset rejection, and input impedance) for a bio perceive AFE [8-9]. The AFE blocks are designed and optimized in such a way that, they are capable of capturing the clear data carried out by the bio perceive signal. The below figure represents the architecture specification compensations in a biosensing AFE.

Revised Version Manuscript Received on 25 November, 2018.

Raja Krishnamoorthy, Professor, CMR Engineering College, Department of ECE, kandlakoyaVillaga, Hyderabad, Telangana, India.

P.T. Kalaivaani, Associate Professor, Department of ECE, Vivekanandha College of Technology for Women, Tiruchengode, Namakkal, Tamilnadu, India.

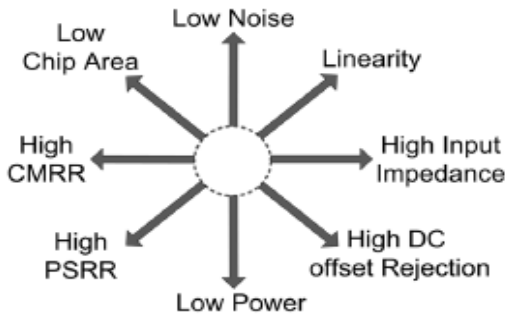


Fig. 3: Architecture parameter tradeoffs in a biosensing

The architecture challenges in the AFE occur because of the following reasons:

1. Device Architecturizing Constraint of the Sensor Nodes: it consists of a flawless count of amplification stages, potential utilization, filter stipulations, linearity, CMRR, and PSRR. The present WBSNS insistences very less power consumption for the entire SoC, when WBSNs are using in wireless power transforms. There is a voltage regulator inside the PMU for recognizing the variations in the supply voltage overdoing to the unpredictable nature of the in taking energy. Because of the absence of bypass off-chip capacitor, the small quantity of wave is observed in the voltage given. In the digital domine, through the post-amplification signal processing the switching noise is injected into the AFE. The common-mode noise appears through the impedance from 50/60 Hz power lines. For overcoming all the above issues, AFE should have huge PSRR and CMRR, the power utilization should be as low as possible ranging from less than 10 μw.
2. The Functioning of Biopotential Signals: These signals are type of signals which have a low-frequency levels, the range of the spectrum is from sub-1 Hz to a few Kilohertz. Less amplitude will be observed in these signals. Its amplitude value ranges from 10s of microvolts to a few milevolts. For assuring better signal recovery, AFE amplifier requisite an adequately less input-referred noise (IRN) per hole radio band. Due to the low frequency levels present in signals, the 1/f noise present in the MOS transistors is an actual responsibility. The amplifier should be capable of adequate vital range, for domiciling the higher levels of the amplitude range.
3. Reconfigurable AFE: In forthcoming, the bio potential authorizations with various magnitudes and radio bands are taken from various parts of the human body and are captured in sensor nodes of WBAN. The reconfigurable criterion frameworkslike gain, radio band, bias current, and sampling rate are majorly considered in a single AFE. The linearity of the amplifier at low bias current is one of the important parameters while designing the ultra- low capacity AFE.
4. Sensor Annexation among the AFE and inert anodes(electrodes): the dc offset voltage is created by the electrode-tissue interface. The offset voltage ranges between 200 to 300 mV. For avoiding the saturation in the first-stage amplifier that offset voltage must be filtered out by the AFE. The input impedance of AFE should as high as possible in order to reduce the impedance balance from sensitivity to electrode.
5. Chip Area: the chip area in this architecture must be as small as possible. The occupied area is inversely proportional to 1/f noise present in the MOS transistors. Due to this, the designing of the device became highly challenging because of its area requirements and specifications of the noise. The image below represents the diagrammatic way of hugely used capacitive conjugated neural networks.

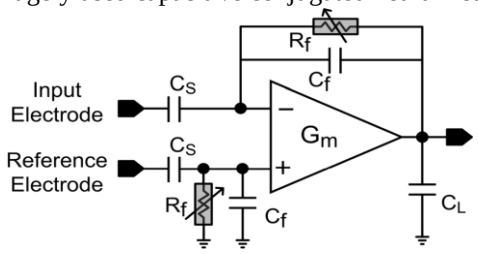


Fig. 4: Diagrammatic way of hugely used capacitive conjugated neural amplifier

Low Pass Filters

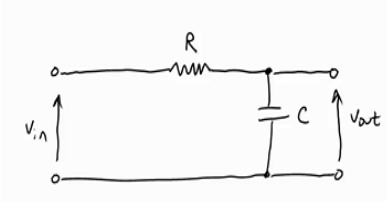
Low pass filters are mostly applicable in all the electronic devices [10] where the low-frequency signals are required by eliminating the high-frequency signals. The low pass filters are easily designed even with passive components. The Gilbert-type cell maintains all the differential current which is executing from the linearized input differential pair. By this, the trance impedance gain [11] will be enabled and that gain is different from the input current I_{var}. The current gain is then mentioned as

$$I_{out} = (I_{var}/I_A)\ X\ (i_{dp}\text{-}i_{dn})$$

Form the above equation it is confirmed that, the trans conductance value is comparative to the intake current I_{var} . All the output values are added for maintaining the output resistance as high as possible. By cascading the output values the DC gain equals to one.

The RC low pass filter

The image below shows the RC low pass filter circuit [12]. The resistor here consists of a resistance R. capacitor with a capacitance C. input voltage is considered as V_{in} and the output voltage as V_{in}.



The input voltage may be a step function, sinusoidal or the combination of both. The general equation for determining the voltage in the resistor is taken as

$$V_R = I_R R \qquad (1)$$

$$\frac{V_R}{R} = I_R \quad (2)$$

The general equation for determining the current in the capacitor is

$$I = C\frac{dv}{dt} \quad (3)$$

$$I_c = C\frac{dV_c}{dt} \quad (4)$$

Here the current flowing through the resistor is equal to the current flowing through the capacitor.

$$I_R = I_c \quad (5)$$

The input potential is similar to the total of the drop down voltage valueacross the resistor and the capacitor.

$$V_{in} = V_R + V_C \quad (6)$$

$$V_R = V_{in} - V_C \quad (7)$$

By following the required derivation of 5 substituting the value of I_c in equation 2.

$$\frac{V_R}{R} = C\frac{dV_c}{dt} \quad (8)$$

Substituting the value of 7 in 8

$$\frac{V_{in}-V_C}{R} = C\frac{dV_c}{dt} \quad (9)$$

$$C\frac{dV_c}{dt} + \frac{V_c}{R} = \frac{V_{in}}{R} \quad (10)$$

$$\frac{dV_c}{dt} + \frac{1}{RC}V_c = \frac{1}{RC}V_{in} \quad (11)$$

Similarly the output voltage is calculated as

$$\frac{dV_{out}}{dt} + \frac{1}{RC}V_{out} = \frac{1}{RC}V_{in} \quad (12)$$

Assuming $inputvoltage V_{in}$ has some sinusoidal input with value

$$V_{in} = V * \sin \omega t \quad (13)$$

Where$V*$ = amplitude of the input voltage

ω = frequency

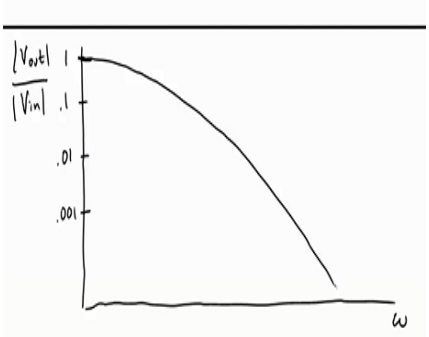
$$V_{out} = A cos\omega t + B \sin \omega t$$

$$= -\frac{\omega RC}{1+(\omega RC)^2}V * cos\omega t + \frac{1}{1+(\omega RC)^2}V * sin\omega t \quad (15)$$

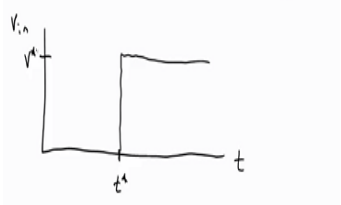
The equations are used for observing the magnitude value coming at the output

$$|V_{out}| = \frac{1}{1+\omega^2(RC^2)}V * = \frac{1}{1+\omega^2(RC^2)}|V_{in}| (16)$$

The ratio of an input voltage and output voltage $\frac{|V_{out}|}{|V_{in}|}$ are shown below.



Here the low-frequency signals are passed through the device and stop the high-frequency signals.If the step function is applied to the circuit



$$V_{out} = V * \left[1 - e^{-\frac{1}{RC}(t-t^0)}\right] \quad (17)$$

$$\frac{1}{2}V * = e^{-\frac{1}{RC}(t-t^*)} = 0.5 (18)$$

$$(t - t^*) - RCln_z^1 = 0.637(RC) \quad (19)$$

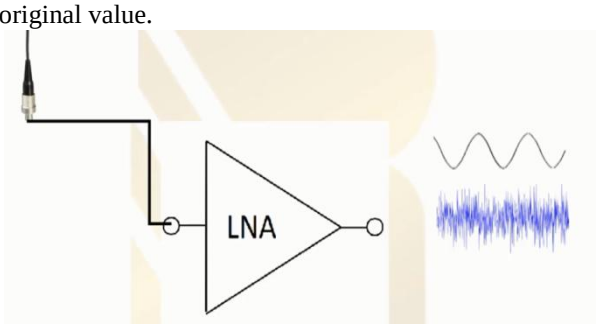
The wave executed at the output.

Low Noise Amplifier

A low noise amplifier is an electronic amplifier which is capable of amplifying a very low-power waves without automatically reducing the value of its signal-to-noise ratio [13]. Raja et al [14] and [15] have designed of a, low power ECG signal processor for wearable health system-review and implementation issues and spike detector for fully Integrated NeuromodulationSoC. Raja and Saravanan [16] and [17] have proposed pipelining shared component architecture in FIR filter.An amplifier expands the capacity of the signal along with the clamour(noise) present at its input. The transmitter sends always the highly amplified signal, but some of the energy of the signal is observed by the environment due to this there will some signal attenuation. When the receiver is receiving the signal, the signal becomes week because of its attenuation.The low noise amplifier intakes the attenuated wave and makes it a strong signal. But as the low noise amplifier intakes the wave from the antenna, due to the noise present in the antenna the user can observe a little error. If SNR = $\frac{P_s}{P_N}$ is before the antenna, then $P_s and P_N$ are amplified with the gain value A.

$$\frac{P_s XA}{P_N XA} \quad (20)$$

By amplifying those values with gain A the user can get anoriginal value.



The sinusoidal wave is the original wave and the blue wave represents the noise present in the antenna. But for getting efficient output SNR should be maintained constantly. All the passive components present in the device consists of noise along with LNA. If all the components are combined then the noise is observed in the output.

$$SNR = \frac{AXP_S}{AXP_N + P_{NO}} \quad (21)$$

P_{NO} is the noise obtained from the device. The main aim of the LNA is to reduce the noise P_{NO} present in the device.

Advantages of LNA

- The noise coming from the device is reduced
- Linearity
- Low power consumption
- High Gain
- Matched to the antenna or filter

System Architecture:

The generic system architecture of analog front end of a bio chip is presented in the figure below. The three main components of the system are Low noise Amplifier, Programmable gain amplifier and a Low pass filter.

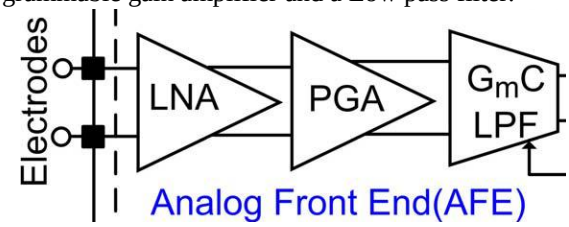


Fig. 5: Analog Front End

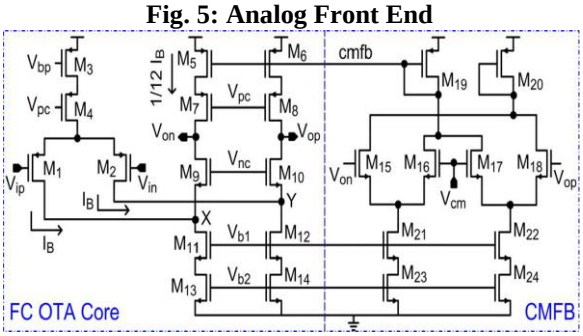


Fig. 6: Illustration of fully differential FC OTA A1 for the biosensing LNA.

Illustration of differential FC OTA A_1 for the bio sensing LNA.The input-referred voltage noise function is mentioned as A_1 , $\overline{v_{ni,A1}^2}$ by using the following relation

$$A_1 , \overline{v_{ni,LNA}^2} = A_1 , \overline{v_{ni,A1}^2} \frac{(C_{S1}+C_{f1}+C_{in\,1})^2}{C_{S1}^2} \quad (22)$$

The value of $\frac{(C_{S1}+C_{f1}+C_{in\,1})^2}{C_{S1}^2}$ as low as possible very near to 1 to lower than the $\overline{v_{ni,LNA}^2}$. By using the below calculation the input-referred voltage noise, with flicker (1/f) and thermal noise factors will be defined as

$$\overline{v_{n,A1}^2} \cong \frac{1}{g_{m\,1,2}}\left\{\frac{4kT}{k} + \frac{16}{3}kT\frac{g_{m\,13,14}}{g_{m\,1,2}} + 163kTgm5,6gm1,2+2COX2fKpW1,2L1,2+KnW13L13gm13,14gm1,22+KpW5L5gm5,6gm1,22 \right. \quad (23)$$

g_m = transconductance of an ith transistor of A_1

K = Boltzmann's constant

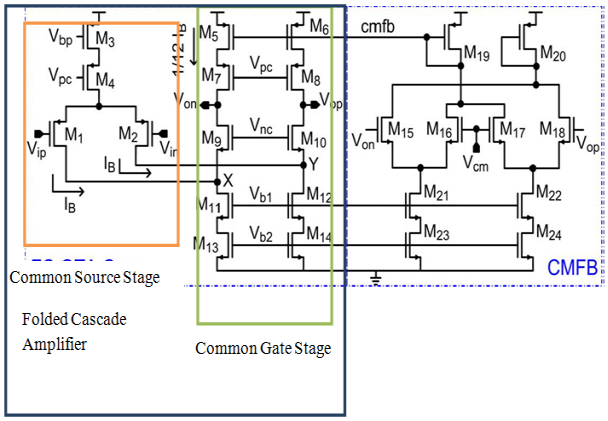
k = subthreshold slope inverse

T = temperature

1/f noise coefficients are taken as K_p and K_n

If the equations (22) & (23) are combined, then the conclusions given by the equations for the LNA design are: it maximizes the transconductance $(g_{m1,2})$ value, the area $(W_{1,2}L_{1,2})$ gets decreased than the thermal and the 1/f noise factors respectively. The parasitic capacitance C_{in1} input pairs gets minimized by keeping the input dimensions less. $\frac{(C_{S1}+C_{f1}+C_{in\,1})}{C_{S1}}$ will be reduced easily if the area is not that much important.

Circuit Operation:



The sub circuit marked in the above figure is the two level folded cascade amplifiers. The first stage is the natural source standing point and is pursued by common gate standing point. In common source part, the transistors M1 and M2 are the common source amplifiers and the transistors M3 and M4 administers the biasing current for the circuit. The signal passed to the common gate stage is amplified. The transistors M9 and M10 are connected in the common gate mode. The transistors M11, M12, M13 and M14 are connected in the feedback mode to adjust the biasing current of the circuit. The transistors M5, M6, M7 and M8 act as load to the circuit. One major problem of the cascade amplifier is that the circuit goes to saturation if the input voltage has fluctuations. In order to nullify the fluctuations and stabilize the circuit, the Common mode feedback circuit is added at the output.

Variable g_{mf} stages used in the LPF core

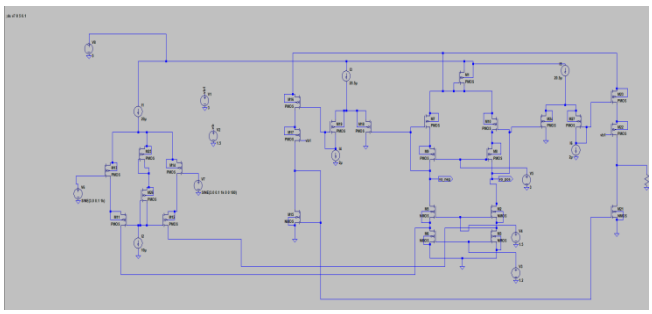


Fig. 7: Proposed reduced diagrammatic way for the variable gmf-stages applied in the LPF

Simplified schematic for the variable $\boldsymbol{g_{mf}}$ stages used in the core LPF. The equation for the simplified variable $\boldsymbol{g_{mf}}$ stages used in the core LPF is taken as:

$$\frac{V_{op}(s) - V_{on}(s)}{V_{ip}(s) - V_{in}(s)} = \frac{(1/b)(g_{mf}/C)^3}{\left\{s^2 + \left(g_{mf}/aC\right)s + (g_{mf}/C)^2\right\}\left\{s + (g_{mf}/bC)\right\}}$$

Single stage transconductance is taken as g_{mf} . The output

resistance of the transistors M_3 and M_4 are kept in saturation mode, these two transistors work as source degenerators for the transistors M_5 and M_6. With the help of the total harmonic distortion (THD) the linearity will be enhanced.The primary functioning of the architecture is the voltage to current conversion. The circuit consists of cascade narrow current swing. The differential stage converts the voltage to current.

Results

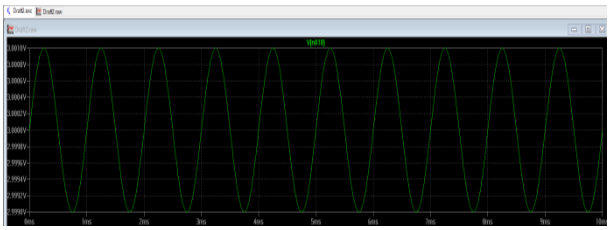


Fig. 8: Input Voltage - FC OTA

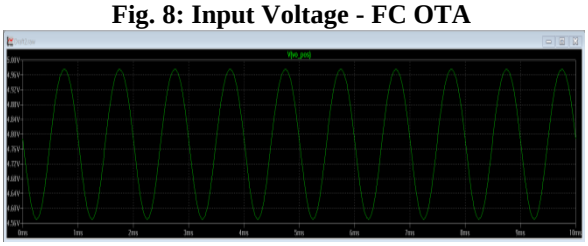


Fig. 9: Output Voltage - FC OTA

Table 1

Input voltage range		Output voltage Range	
Min Voltage (v)	Max Voltage (v)	Min Voltage (v)	Max Voltage (v)
2.9	3.01	4.56	5

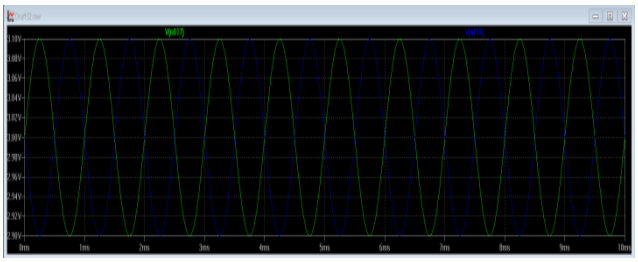


Fig. 10: gmf-stages used in the LPF

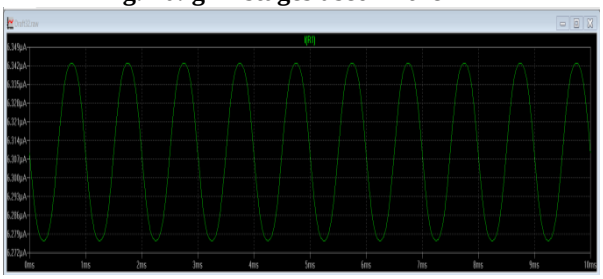


Fig. 11: Current output of gmf-stages used in the LPF

Table 2

PMOS	Size (µm x µm)	Count (µm x µm)
	1x16	6
	1x3	6
	1x1	5
	1x10	2
NMOS	1x1	2
	1x2	4

Table 3

	Chip Area
Proposed Circuit	157 μm^2
Existing Circuit	159μm^2

II. CONCLUSION

This paper presents the implementation of analog frontend circuits used in the bio sensing devices. The proposed design uses narrow swing current mirrors which occupy less area and perform considerably well in limited voltage conditions. The circuit area is reduced to 157 μm^2 by using the narrow swing current mirror circuit instead of wide swing current mirror.

Ethical Clearance- Taken from Department of ECE, CMR Engineering College

Source of Funding: No

Conflict of Interest: No

REFERENCES

1. J. Guo, "Smartphone-Powered Electrochemical Biosensing Dongle for Emerging Medical IoTs Application," in IEEE Transactions on Industrial Informatics, vol. PP, no. 99, pp. 1-1. doi: 10.1109/TII.2017.2777145
2. D. Metcalf, S. T. J. Milliard, M. Gomez and M. Schwartz, "Wearables and the Internet of Things for Health: Wearable, Interconnected Devices Promise More Efficient and Comprehensive Health Care," in IEEE Pulse, vol. 7, no. 5, pp. 35-39, Sept.-Oct. 2016
3. J. H. Abawajy and M. M. Hassan, "Federated Internet of Things and Cloud Computing Pervasive Patient Health Monitoring System," in IEEE Communications Magazine, vol. 55, no. 1, pp. 48-53, January 2017.
4. V. Sadhu, X. Zhao, and D. Pompili, "Energy-efficient analog sensing for large-scale, high-density persistent wireless monitoring," in Proc. IEEE 13th Annu. Conf. Wireless On-Demand Netw. Syst. Services, Feb. 2017, pp. 1–8.
5. M. Wang, T. C. Chang, T. Teisberg, M. Weber, J. Charthad, and A. Arbabian, "Closed-loop ultrasonic power and communication with multiple miniaturized active implantable medical devices," 2017 IEEE Int. Ultrason. Symp., pp. 7–10, 2017.
6. D. S. Zois, M. Levorato, and U. Mitra, ''Energy-efficient, heterogeneous sensor selection for physical activity detection in wireless body area networks,'' IEEE Trans. Signal Process., vol. 61, no. 7, pp. 1581–1594, Apr. 2013.
7. D. Bortolotti, M. Mangia, A. Bartolini, R. Rovatti, G. Setti and L. Benini, "Energy-Aware Bio-signal Compressed Sensing Reconstruction on the WBSNgateway", IEEE Transactions on Emerging Topics in Computing, 2016. DOI: 10.1109/TETC.2016.2564361.
8. M. S. Mahmud, H. Wang, A. Esfar-E-Alam, and H. Fang, "A Wireless Health Monitoring System Using Mobile Phone Accessories," IEEE Internet of Things Journal, vol. 4, pp. 2009- 2018, 2017.
9. F. Pareschi, P. Albertini, G. Frattini, M. Mangia, R. Rovatti, G. Setti, "HardwareAlgorithms Co-design and Implementation of an Analog-to-Information Converter for Biosignals based on Compressed Sensing," IEEE Trans. on Biomed. Circuits Syst., vol. 10, no. 1, pp. 149-161. February 2016.
10. M. Elhoseny, G. Ramírez-González, O. M. Abu-Elnasr, S. A. Shawkat, N. Arunkumar, and A. Farouk, ''Secure medical data transmission model for IoT-based healthcare systems,'' IEEE Access, vol. 6, pp. 20596–20608, 2018.
11. C. Sawigun and P. Pawarangkoon, "0.6-V, Sub-nW, second-order lowpass filters using flipped voltage followers," in Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Jeju, 2016, pp. 254-257..
12. A. Rasekh, M. S. Bakhtiar. "Design of Low-Power Low-Area Tunable Active RC Filters". IEEE Transactions on Circuits and Systems II: Express Briefs, 2017. DOI: 10.1109/TCSII.2017.2658635.
13. H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications", IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 1993–2005,Aug. 2010.

14. Raja, K., S. Saravanan, R. Anitha, S. SuganthiPriya, and R. Subhashini. "Design of a low power ECG signal processor for wearable health system-review and implementation issues." In Intelligent Systems and Control (ISCO), 2017 11th International Conference on, pp. 383-387. IEEE, 2017.
15. Raja, K., Saravanan, S., Malini, P., Raveena, V., &Praveena, R. S. (2017, January). Design of a spike detector for fully Integrated NeuromodulationSoC. In Intelligent Systems and Control (ISCO), 2017 11th International Conference on (pp. 341-345). IEEE.
16. Raja, K., &Saravanan, S. (2016). A New Clock Gated Flip Flop for Pipelining Architecture. Circuits and Systems, 7(08), 1361.
17. Saravanan, S., & Raja, K. (2016). Shared Processing Element Architecture for An Area and Power Efficient FIR Filter Design using Double Base Number System. Asian Journal of Research in Social Sciences and Humanities, 6(8), 2513-2520.