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Performance Analysis of Low Noise Amplifier using Junction Less GAA TFET and Conventional MOSFET

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Abstract: ***The risingdemands to overcome the disadvantage of conventional MOSFET such as physical limitations due to its short channel effects has stimulated the development of a number of better device geometries and materials. Few of such novel devices are FinField Effect Transistor, Nanowire and FETs based on Carbon Nanotube, having characteristics like quasi two- as well as one-dimensional channel geometries for better electrostatics. While a lot of these efforts aims only on building up high-performance devices, the making of a roadmap to forecast analog circuit performance added with the large scale integration for these technologies is essential. In this paper we have incorporated Junctionless gate all around TFET for analog circuit design, thus leading to ease of fabrication because of absence of doping concentration gradients for specific regions. In addition low power consumption is obtained by TFETs as they are less prone to second order effects. The common source low noise amplifier circuit has been designed using the device as well as MOSFET and their performances are analyzed using various parameters like gain and noise figure.***

Keywords: Junctionless Gate all around TFET, MOSFET, Low Noise Amplifier, Gain, Noise figure.

I. INRODUCTION

As technology keeps on scaling down to the nanometre range, reserchers and engineering professionals are stressed to struggle with problems linked with power limitations in every level of abstraction. As a result of this, efforts are taken to implement efficient device designs[1][2]. This focuses on latest efforts to diminish the supply voltage by discovering new device architectures as well as appropriate material arrangements, especially in device level simulations. Voltage scaling in Complementary MOS transistors is considered as a important issue due to the divergence between the threshold voltage scaling and high leakage[7]. Development to device architecture like superior electrostatics via multi-gate devices aids in lesser supply voltages as well as constant threshold. Similarly, III-V group materials presents the ability to get better electron mobility along with same field strength.[6][11] Junctionless TFET with Gate all around architecture has come out as a well-built candidate for low-energy applications because of its better energy competence which occurs due to the sub-thermal switching characteristics at low supply voltages. In addition the steep switching characteristics, a blend of sole qualities of TFETs such as asymmetrical source/drain design, and uni-directional conduction offer new opportunities and confronts for analog and digital design.[10] Even thougha first-class device-level performance metrics do not always fall into a noteworthy advantage at the circuit level, any improvement in circuit performances are decided byproper designing of device-level components.[8][9] Drive current (Ion) is significantlyenhanced by the narrow energy bandgap of Ge (0.66 eV) and theambipolar behavior because of gate-induced drain leakage. (GIDL) is wellconcealed with the help of wide energy bandgap of GaAs (1.42 eV). Ion of Tunnel FET is chiefly determined by energy bandgap (EG) of source material and effective tunneling mass of carriers.[4][5] A steeper slope is estimated by Band To Band tunneling in Tunnel FET than by drift-diffusion transports in conventional MOSFETs. Moreover, the small swing is extremelycertain becauseof embedding Germanium with a narrow energy-bandgap at source and GaAs with a large one at drain.

In this paper, the performance of Junctionless Gate all around TFETs has been investigated by employing the device in the design of low noise amplifier. The vigor and the peculiar advantages of its suitability for circuit design as well as the circuit performance is analyzed via its performance parameters like gain and noise figure. Also the low noise amplifier is designed in Conventional MOSFET as well as Junction less GAA TFET and the performances are evaluated.

II. SIMULATION ANDMETHODOLOGY

In order to for ecasteffective performance of the circuits, we performed the mixed mode simulation of Common Source Amplifier. We performed simulations using Sentaurus TCAD software tool. The various sections of the simulation, the files and the methods involved in it are briefed below. A brief overview on the method of simulation and the tool is explained.

A device simulation offers information about the inner limitations and the terminal characteristics of the device by which the device behaviour is predicted. The device to be simulated is taken as a meshed finite-element structure. Every node of the device has special characteristics such as material type and doping concentration. For all the nodes, the carrier concentration, current densities, electric field, generation and recombination rates, and many other parameters are found using simulation.

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The purpose of Sentaurus Structure Editor is to build two dimensional and three dimensional device structures. Input file is basically a script file that holds commands describing the steps to be carried out as well as the physics section describing the specific material properties. It also contains the simulation timing details with respect to other parameters. Sentaurus Device simulates numerically the electrical behaviour of a device or circuit in separation or quite a few physical devices joint in a circuit.

The grid of the the circuit simulated holds an account of a variety of regions such as the boundaries, material types, and any electrical contacts. Sentaurus Visual is referred to picturise the results produced bysentaurus simulation tools in all three dimensions.

The following steps are followed in simulation of the circuit.

- The modelled p-type and n-type device files are included within the DEVICE sections separately for n type and p-type devices with unique names. The "output " files are removed from the device sections.
- Both the n-type and p-type devices are declared within the DEVICE sections and a common output file is declared within a separate file section which is shared by both the p-type and n-type devices.
- The interconnections between the transistors are specified within the system section.
- Also they are specified within the instances of the devices declared. The voltage sources and any other electrical components are also declared within the system section.
- The voltage sweeps are given within solve section using quasi- stationary statements for all the specified voltage sources.
- Then the file is simulated using the sDevice command.
- The plot is specified within the system section and the output plot is viewed through sVisual.

III. DESIGN OF LNA USING CONVENTIONAL MOSFET

There are various topologies of LNA like CS (Common Source), CG (Common Gate) and Cascode stage LNAs. In this paper, Common source LNA with inductive load to be designed in 45 nm technologies is simulated and analysed.

Usually, Low Noise Amplifier circuits are designed as Common Source (CS) or Common Gate (CG) stages. Selecting appropriate circuit depends on the special purpose for which the circuit is designed for. CS and CG are two commonly used transistor configurations in Complementary MOS based LNA circuits. Common Source LNA offers good gain as well as better noise performance.

The inductor over the source of a Common Source LNA influences the gain as well as the noise performance of LNA. Common Gate configuration offers reduced power consumption and poor noise. Common Source configuration can be applied for wideband as well as matching circuits. Inductive source Common Source configuration is commonly employed in narrowband Low Noise Amplifiers. The most important parameters that defines the efficiency of a low noise amplifier are power consumption, bandwidth, stability, linearity and area.

The schematic view of the 45nm technology common source LNA simulated using Virtuoso Simulation spectre (cadence EDA tool) is shown in Figure 1. The transistorsizing ratio and the values of other components of the circuit has been varied according to the technology to obtain the proper Gain and Noise Figure.

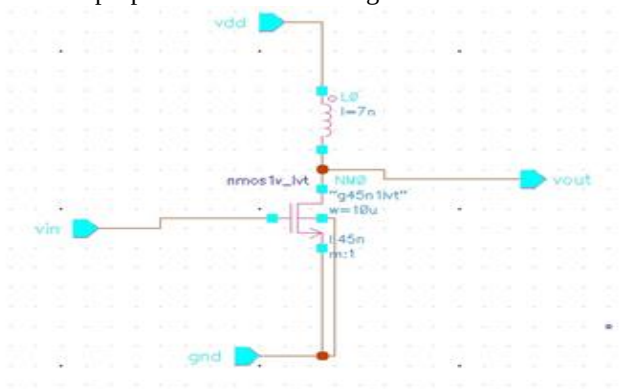

Figure 1 Schematic of 45nm CS LNA with inductive load

The transient analysis is carried out to the amplification character of LNA. the transient analysis for 45 nm LNA is shown in figure 2

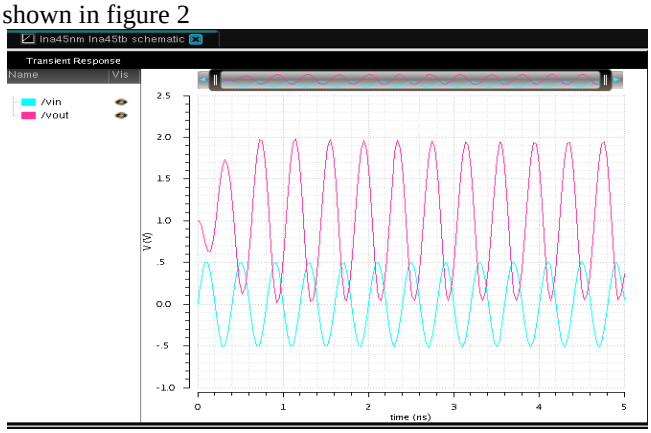

Figure 2 Transient analysis of 45nm MOSFET based CS LNA with inductive load

The gain is computed by S-parameter analysis in cadence and it is found to be16.14 dB and is shown in figure 3. By varying the resistance of the voltage divider circuit the gain is altered.

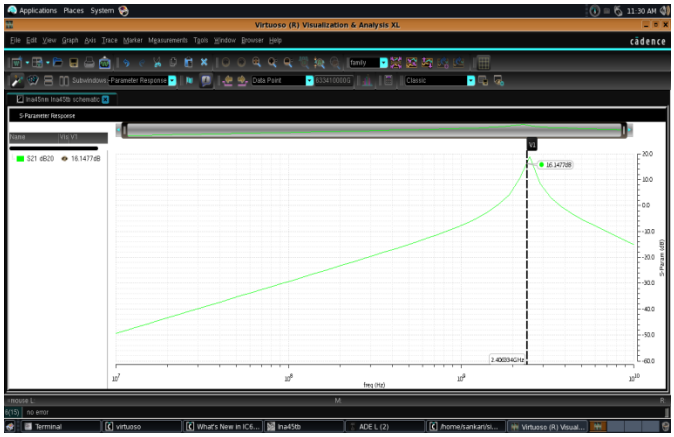

Figure 3 Gain of 45 nm MOSFET based LNA with CS with inductive load

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The noise figure is computed by noise analysis in cadence and it is found to be 1.4 dB and is shown in figure 4By varying the resistance of the port network the noise figure can be varied.

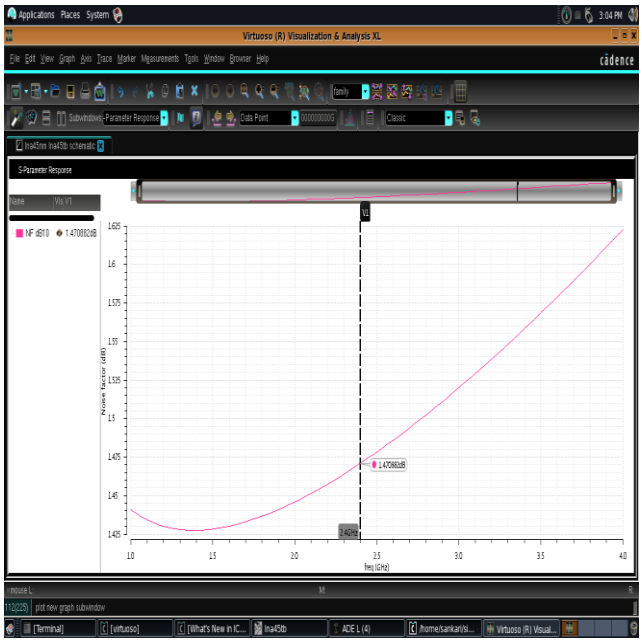

Figure 4. Noise figure of 45 nm LNA with CS with inductive load

IV. DESIGN OF LNA USING JUNCTIONLESS GATE ALL AROUND TFET

The Low Noise Amplifier was simulated for similar parameters using the Junctionless Gate all around TFET using the mixed mode simulation as mentioned using Sentaurus TCAD. The transient waveform of the LNA designed using the 45 nm Junctionless GAA Germanium TFET is obtained as shown in the figure 5

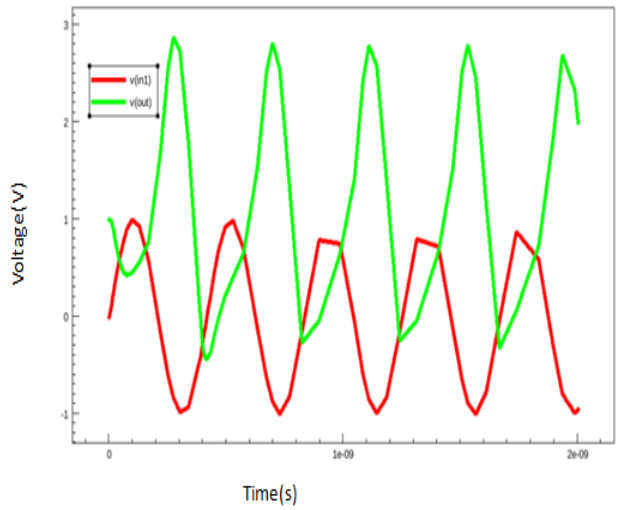

Figure 5Transient waveform using Junctionless GAA 45 nm Germanium TFET.

Also, the Masons unilateral gain through the AC analysis of the Junctionless Gate all around Germanium TFET is simulated using inspect. The waveform of gain is shown in the figure 6

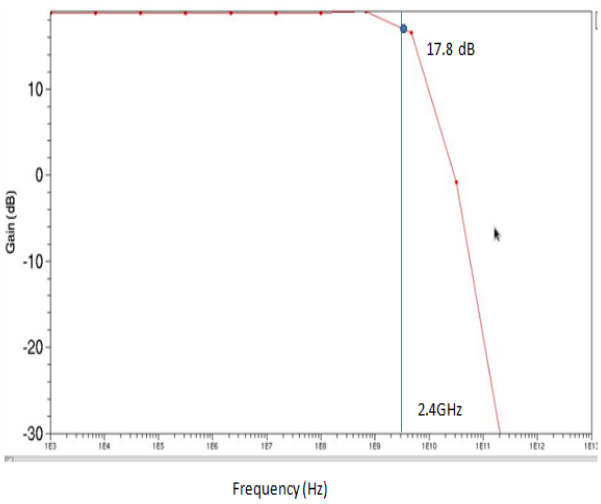

Figure 6 Gain of CS LNA using Junctionless 45nm GAA Germanium TFET

The inductor was varied from 6 nF to 8 nF to obtain the optimized Gain. As it is done in LNA using MOSFET, Similar resistive biasing is used to bias the input to the TFET. Also, the inductor, the input and output capacitances are used to design the frequency of the Low noise amplifier. The device is simulated for the specific range of frequencies according to the application for which the circuit is designed for. The outputs obtained are transformed to S parameter and S21 is considered as gain of the amplifier. Noise simulation in SentaurusSdevice is simulated with noise models added in the physics section. Noise-figure (NF) is calculated by considering a signal source resistance equal to 50 Ω.[3][4] Thus the noise figure manual calculation is doneand the result is obtained as 1.5 dB**.**The results obtained for 45nmCommon Source with inductive load Low Noise Amplifier using conventional MOSFET and Junctionless GAA TFET are compared in table 1

Table 4.1 Results

Parameter	CS with inductive load 45nm MOSFET	CS with inductive load using 45 nm Junctionless GAA TFET
Gain(dB)	########	########
NF(Noise figure)(dB)	########	########

V. CONCLUSION

In this paper, the low noise amplifier design using Junctionless TFET Nanowire as well as MOSFET is simulated and analyzed for its performance via performance parameters like gain and noise figure. More analyses were done on choosing appropriate technology as well as dimensional parameters. Germanium, out of other materials, had given an optimized gain as well as noise figure whereas other materials including certain heterostructurecombinations seem to have tradeoff between gain and noise figure.

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The CS with inductive load LNA designed using Junctionless GAA TFET was designed and simulated to obtain the optimized and improved gain of 17.8 dB when compared to MOSFET. Further improvement can be achieved by choosing proper hetero structure [12][13] since bandgap plays a major role in varying both frequency and Ion/Ioff parameters.

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