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Design and Anlaysis of Low Power Full Adder using 65nm CMOS Technology

K.Paramasivam, Suresh Kumar N

Abstract: ***This Paper deals with Low-Power full adder using 65nm CMOS Technology by taking merits of existing full-adders. The proposed one-bit full adder has least power consumption. The proposed adder compared and then analyzed average power, Area and Max power with existing full adder. The designs have been simulated shown results using Tanner EDA tool.***

Keywords: CMOS, Area, Average Power

I. INTRODUCTION

The demand of increasing electronic circuits the least energy design of very large-scale integration circuits has important role in digital circuits [1]. The energy dissipation in a circuit has two types namely dynamic energy and static energy [2]. Reduce the run time leakage is main challenge in digital system design [3]. here we discuss various type of one-bit full adders transistors level and implementation method.

A. Transistor full adder

Sum and Carry out are outputs and A, B and Cin are inputs[4]. It has 28 transistor full-adder also known as Mirror full-adder. This is an efferent way implement of generate/propagate/delete function of full adder. As depicted in fig 1. Cout is set and Vdd is GndEither delete or generate is high respectively the conditions [5].

$$Cout = AB + BCin + ACin \quad (1)$$

$$Sum = Cout(A + B + Cin) + ABCin \quad (2)$$

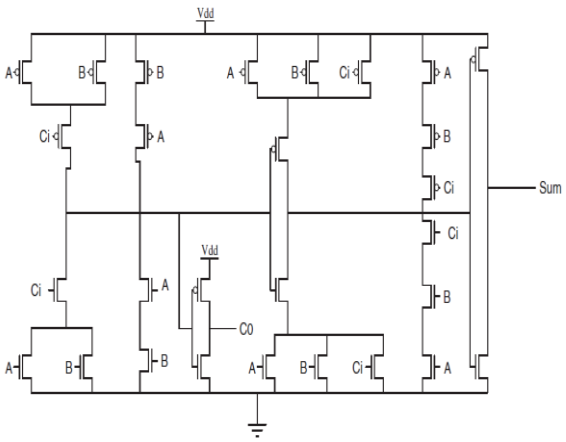

Fig. 1 28T Mirror Full adder

B. 14T Full-adder

The design is customary compare with classic full-adder design. Both Ex-nor and Ex-Or are used to generate sum and carry out at same time.14Transistors have four transistors Ex-Or logic and next part is inverter to make Exclusive-Nor. The improved 14T full-adder as depicted in fig 2.

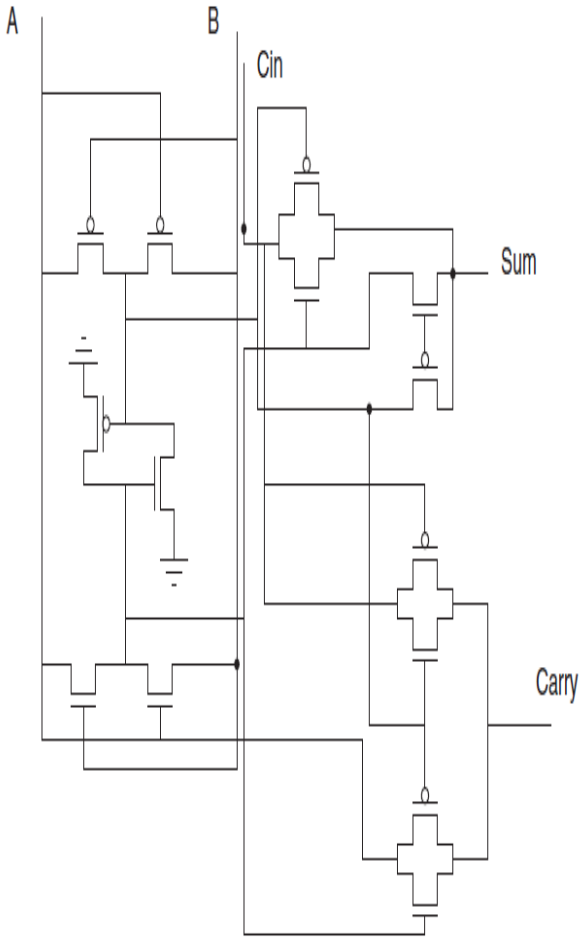

Fig.2 14 T full-adder

C. 12 Transistors Full-adder

The 12 Transistors full adder fully created by using 2:1 mux. Power reduction achieved by dully executed mux based full-adder as depicted in fig 3.

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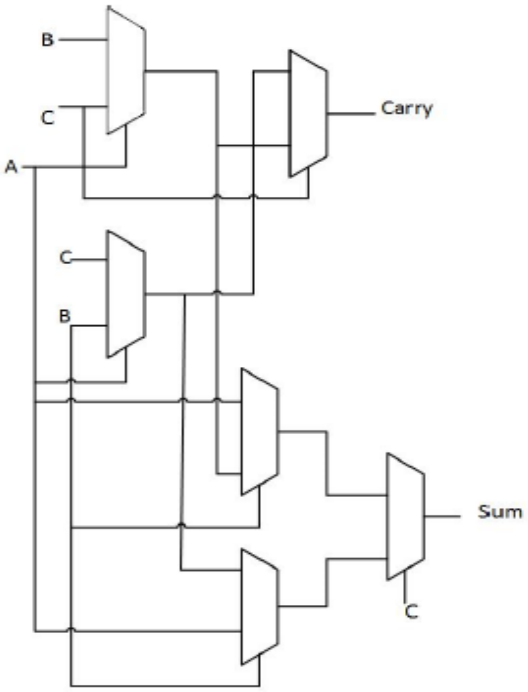

Fig.3. 12T full-adder

D. 8 Transistor Full-adder

The 8T full adder created by three selectors. In Two selectors each selector has one Vdd and two pMOS and third selector has one invertor this structure lead to speed up propagation of Cout and generate of Sum. The 8T full adder depicted in fig 4.

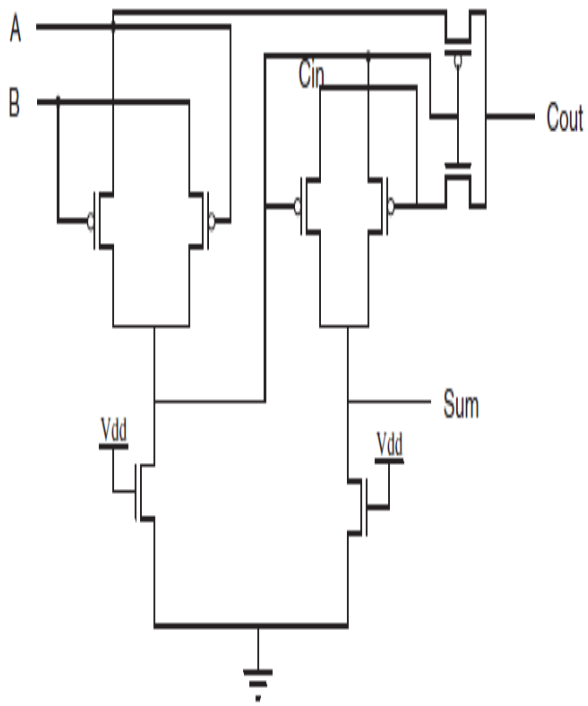

Fig. 4 8T Full-adder

E.Proposed low-power Full-adder

This 10T Full adder made by 4TXor and Two 2:1 mux and one inverter. The 2:1 mux reducing critical path delay these lead to reduce the consumption as depicted in fig 5.

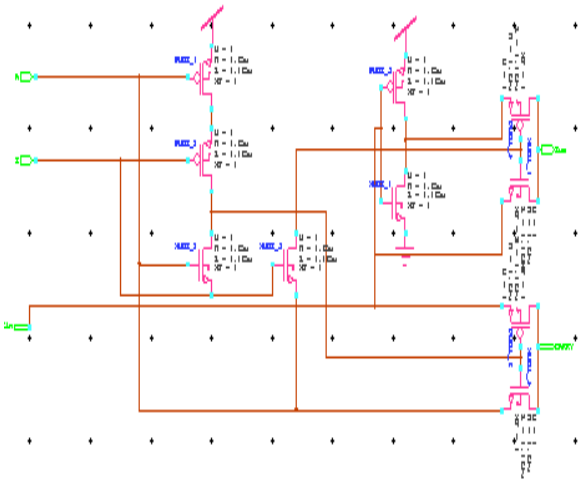

Fig. 5 low-power 10 T full-adder

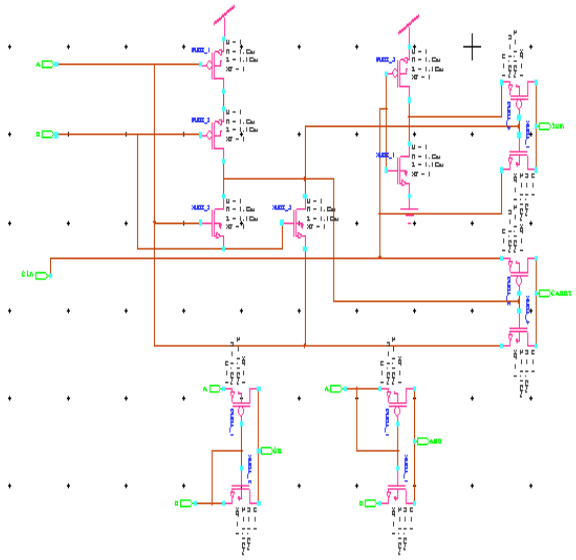

Fig.6 Proposed Low-power full-adder in ALU

Proposed 10T Low-power full-adder enforced to Arithmatic logic unit (ALU) and array structure multipliers. The major funtions of ALU are arithmetic and Logical operations the total number of transistor count is 14. The low power minimum area ALU as depicted in fig 6.

II. SIMULATION RESULT

The table I shown the comparison of Area, Average Power, Maximum-Power in 28T, 14T, 12T, 8T and proposed low power 10T full adder. Simulation results shown in table 1 for the analysis. Full adder and ALU output waveform shown in fig 7 and 8 also performance graph of Avg power, Area and Max power as depicted in fig 9 (a), (b) and (c).

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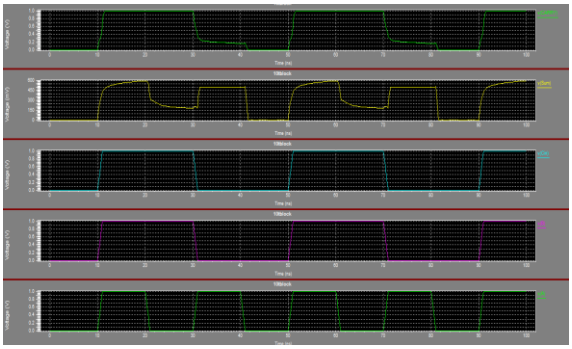


Fig. 7 Low-Power Full-adder waveform

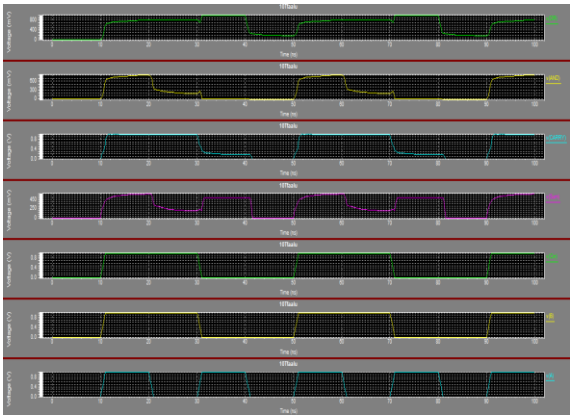
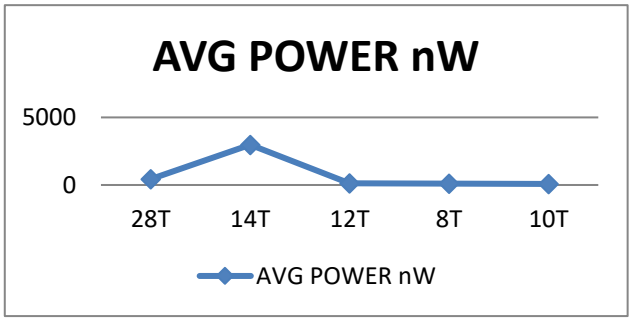


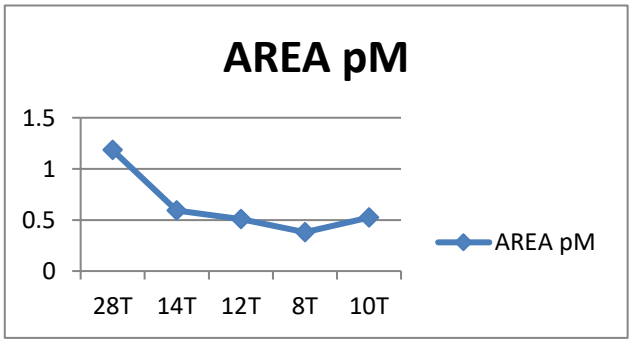
Fig. 8 proposed ALU waveform

Table1. Proposed Full-adder compare to Existing Full adders

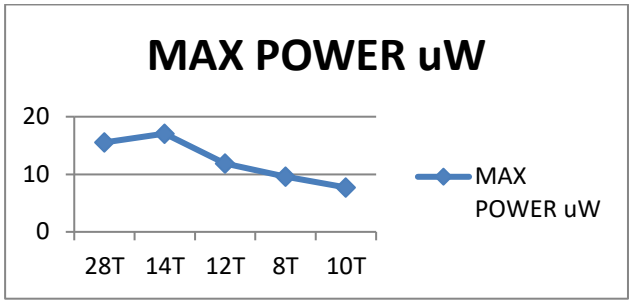
S.No	FA's	AVG POWER	AREA	MAX POWER
1	28T	.435uW	1.183pM	15.51uW
2	14T	2.975uW	.591pM	17.06uW
3	12T	.135uW	.507pM	11.89uW
4	8T	89.66nW	.380pM	9.604uW
5	10T	77.31nW	.523pM	7.713uW



(a)



(b)



(c)

Fig. 9 Performance Graph

From the result 10T full adder in ALU achieved good efficient circuit compare with traditional adder basics of Average-Power, Area and Maximum-Power.

III. CONCLUSION

The proposed Low-power full adder in ALU using 65nm CMOS Technology has good performance in terms of Average-power and Maximum power reduction compared with Classical Full-adder. This approach archives high Power minimization

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