Minimum Power Consumption High Efficiency Bypassing-Based 2D Multiplier Design using 65nm CMOS Technology

K. Paramasivam, Suresh Kumar N

Abstract: ***Presently, in VLSI design, Power management has turn out to be a major issue. In this research, a Minimum Power Consumption Bypassing-Based 2D Multiplier Design using 65nm CMOS Technology was presented. When matched up with digital row bypassing based multiplier design, digital column bypassing based multiplier design and digital low power two-dimension bypassing based multiplier design, the experimentation outcomes shown our presented Multiplier Design decreases 31.2% of the power dissipation for 4*4 Multiplier.***

Keywords: Low Power, Multiplier, CMOS, Bypassing

INTRODUCTION

In case of DSP applications, Multiplication is a basic arithmetic operation. The multiplication movement of 2 un-signed n- numbers bit,, $X=x_{k-1}$, $x_{k-2}\ldots x_0$ are multiplicand, $Y=y_{k-1},y_{k-2}\ldots.y_0$ are multiplier, $p=p_{k-1},p_{k-2}\ldots p_0$ are Product denoted in this manner:

$$P = P_{2k-1}P_{2k-2}....P_0 = \sum_{i=0}^{k-1}\sum_{i=0}^{k-1} (x_m y_n)\, 2^{m+n}$$

With the intention of making the greater effective demand in Digital Signal Processing applications, the digital array basic multiplier deign depicted in fig. 1 the general enforcement in a digital array design [1] was depicted. In order to perform the multiplication, each adding unit encompassed an AND gate and Full adders for accumulating the k x k partial product multiplication therefore, needs an overall k2 AND gates and k(k-1) Full Adder.

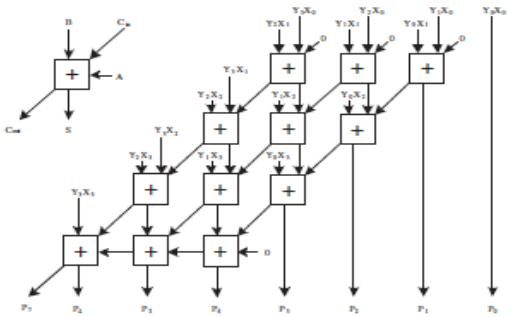

Fig. 1 Digital basic array Multiplier

Revised Version Manuscript Received on 25 November, 2018.

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According to Complementary MOS circuitry, the power dissipation is split into dynamic power dissipation and staticpower dissipation [2]. The dynamic power is produced and the utilization from charging as well as dis-charging of the load capacitances, the static power dissipation is producedand the utilization is relative to the amount of the transistor utilized [3]. Instead, from the switching transient current average dynamic power-dissipation of in CMOS could be

$$p_{avg} = \tfrac{1}{2}\, c\, f\, V_{dd} N$$

Here V_{dd} is known as power supply voltage, C is known as load capacitance, N is called as number of switching activity of clock cycle and f is known as clock frequency. Obviously, when provided logic circuit switching activity is decreased deprived of varying its function, the power utilization could be decreased.

DIGITAL ROW BYPASSING BASED MULTIPLIER DESIGN

In case of a digital row bypassing based multiplier design [8], In addition process the m^{th} row could by-passed for the purpose of energy usage drop. When binary ynbit, multiplication is 0, that is to say each and every partial products, $x_m y_n$,, $0 \le m \le k-1$, are 0.

$$\begin{array}{llllllll}
Y = & Y_3 & Y_2 & Y_1 & Y_0 & & & \\
X = & X_3 & X_2 & X_1 & X_0 & & & \\
\hline
 & Y_3X_0 & Y_2X_0 & Y_1X_0 & Y_0X_0 & & & \\
 & Y_3X_1 & Y_2X_1 & Y_1X_1 & Y_0X_1 & & & \\
 & Y_3X_2 & Y_2X_2 & Y_1X_2 & Y_0X_2 & & & \\
 & Y_3X_3 & Y_2X_3 & Y_1X_3 & Y_0X_3 & & & \\
\hline
P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}$$

Consequently, in addition n^{th} row of carry save adders could by-passed, the outcomes from the $(n-1)^{th}$ row of carry save adders could be unswervingly sent to the row $(n+1)^{th}$ Carry Save Adders deprived of disturbing outcome in the multiplication. In order to the multiplier design, every changed Full Adder of array Carry Save Adder connected by 3-tri state buffers as well as that 2 two-to-one multiplexers. So that the addition processes of the right at the end full adder in the rows of carry save adder are by-passed,

residuary rectifying circuits should be included to rectify the multiplication final outcome. A 4x4 digital array multiplier with row by-passing multiplier as depicted in fig. 2.

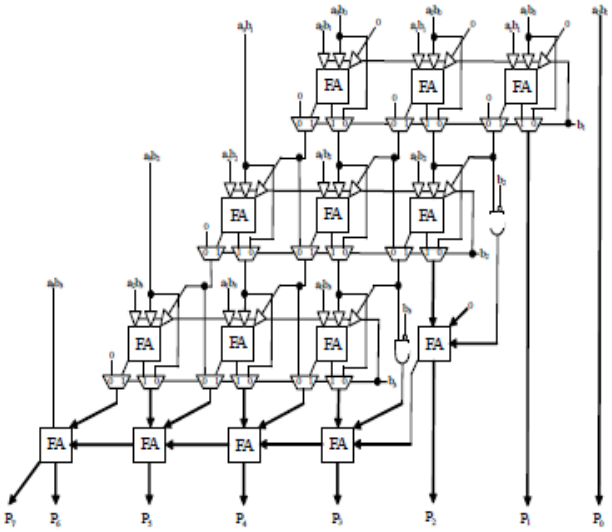


Fig. 2 Digital row bypassing based multiplier design

I. DIGITAL COLUMN BYPASSING BASED MULTIPLIER DESIGN

According to a digital column bypassing multiplier [9]. In case of multiplier design, the changed Full Adder is unpretentious compared to the row bypassing multiplier. Every changed Full Adder in the Carry Save Adder array is just connected through 2 tri-state buffers as well as 1 2- to -1 multiplier. In addition processes $(m+1)^{th}$ column could be bypassed, when $x_m$bit. The multiplicand is 0, to say that complete partial product $x_m y_n$, $0 \leq n \leq k-1$ are 0. Since the bit x_m, the multiplicand is 0, inputs in the $(m+1)^{th}$ column would be put out of action and the carry yields in the column should be fixed to be 0 with aim of generating the accurate results. Therefore, the conserving process could be accomplished through adding an AND gate at the outcomes in the final row of Carry Save Adder. On the other hand, the multiplier design doesn't want the additional rectifying circuits as depicted in fig. 2. A 4x4 digital column by-passing multiplier design could be depicted fig. 3.

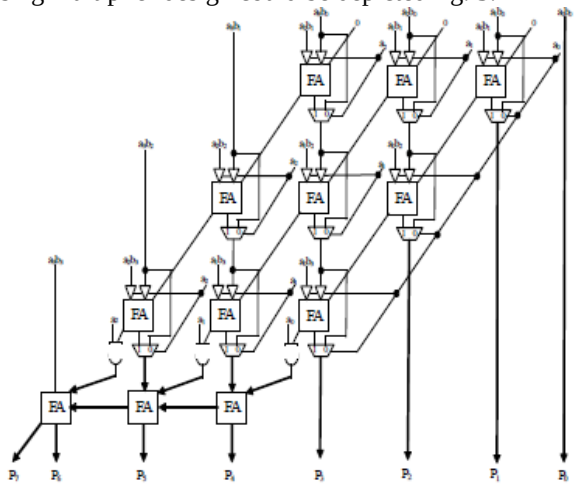


Fig. 3Digital column bypassing based multiplier design

II. DIGITAL LOW POWER TWO-DIMENSIONAL BYPASSING BASED MULTIPLIER DESIGN

In case of two dimensional by-passing based design [12], in addition processes the n^{th} row or $(m+1)^{th}$ column could be by-passed to the purpose of energy reduction. When x_m bit, y_n bit either the multiplicand 0 or the multiplier 0. Instead with the aim of correcting Carry Propagation for the multiplication outcome, the carry bit to the prior row should be taken for two- dimensional by-passing-based condition.

Dependent upon low-power two dimensional by-passed multiplier design [11], in adding function $(m+1,n)^{th}$full adder could be by-passed, when multiplying $x_m y_m$ product is equivalent for the bit Carry Cm,n-1. Specifically, product $x_m y_n$ is not equivalent for Cm,n-1bit, in addition process for $(m+1,n)^{th}$ full adder should activated. Therefore, the CS(control signal) signal for the by-passing position could be received through XOR outcome in the $x_m y_n$product, and the Carry Cm,n-1 bit.

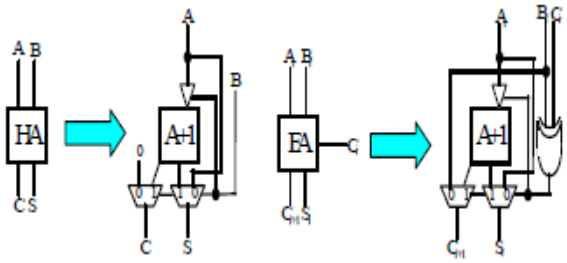


Fig. 4 HA (Half Adder) and FA (Full Adder) using incremental adder

Dependent upon the by-passing based situation, it's well known $(m+1,n)^{th}$ full adder performs addition incremental adder (A+1), as $x_m y_n$ product not equivalent for bit carry Cm,n-1.Instead, the $x_m y_n$ product equivalent for carry Cm,n-1 bit, in addition outcome for $(m+1,n)^{th}$ full adder would received by adding two or zero. As a result the ensuing Carry Cm+1,n bit, for $(m+1,n)^{th}$ full adder could by-passed from former Carry Cm,n-1 bit, the $(m+1,n)^{th}$ full adder could substituted combined an incremental adder , moreover, every simplified adder A+1, in the carry save adder array is connected by one Tri-State buffer as well as 2 two-to-one multiplexers, likewise, a half adder could be substituted with an incremental adder (A+1), combined the by-passing level as $x_m y_n$=zero. The by-passing Half Adder as well as Full Adder is depicted in fig.4. By means of the by-passing design for a Half Adder as well as Full Adder, in fig.5, a 4 x 4 digital low-power two-dimensional by-passing multiplier design is depicted.

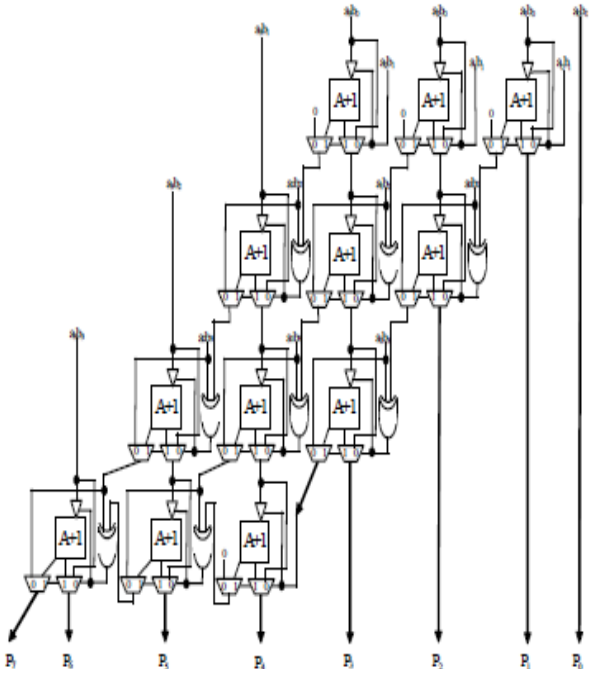
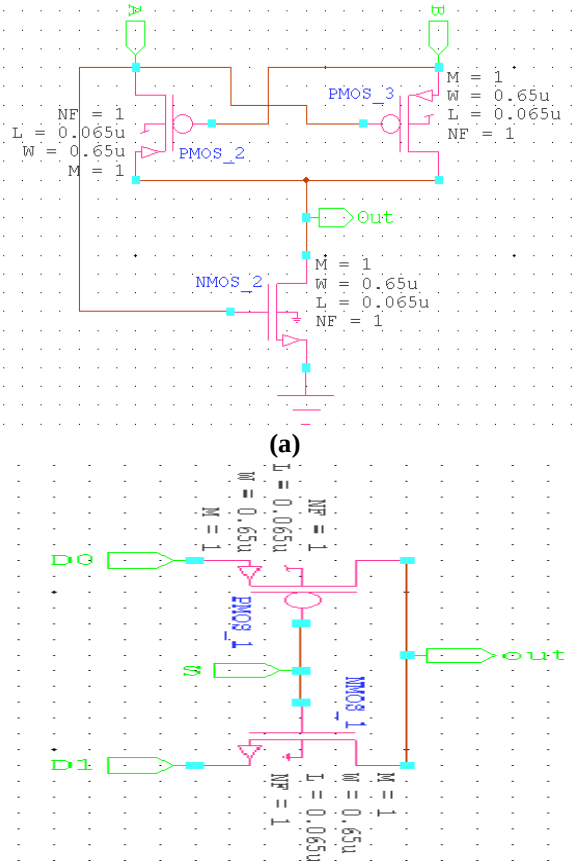


Fig.5. Digital 2-Dimensional by-passing Multiplier Design

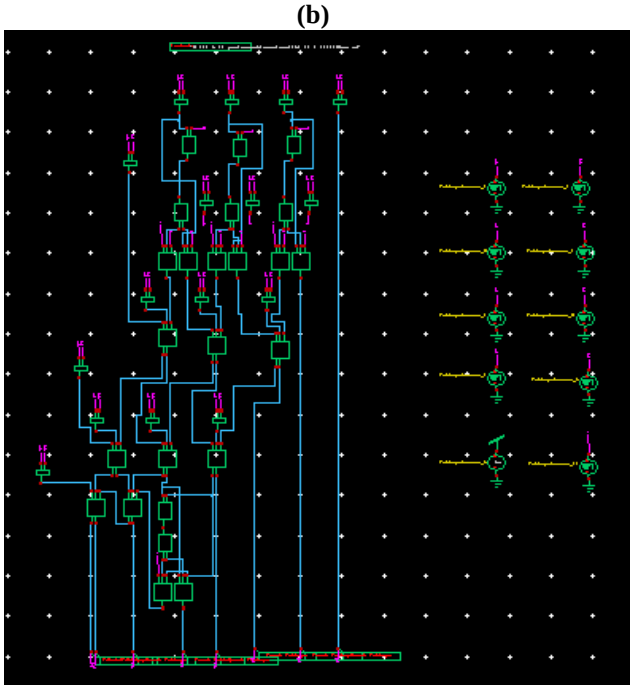
III. PROPOSED LOW-POWER HIGH EFFICIENCY BY-PASSING 2D MULTIPLIER DESIGN

The Implementation of Low Power High Efficiency Bypassing-Based 2D Multiplier Design using 65nm CMOS Technology is same as fig.5. Instead of using the 8T Xor gate and 10T multiplexer gate we use 3T Xor and 2T multiplexer gate also depicted as fig (a) and (b)



(a)

(b)



(c)

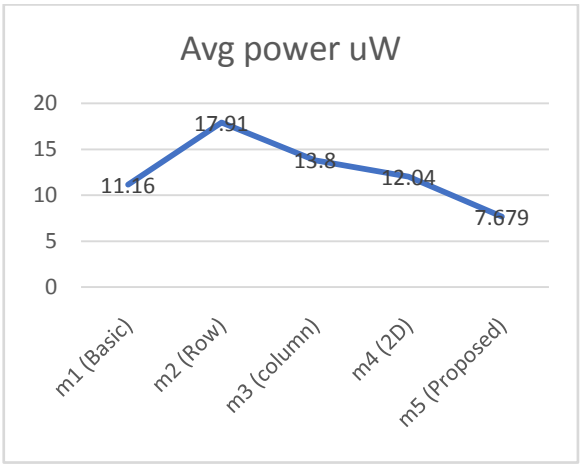
Fig 6. CMOS gates: (a) 3T Xor gate, (b) 2T 2:1 mux gate, (c) Schematic diagram

The fig. 6. Shows two input MUX configuration, we linked PMOS in addition to NMOS in the company of a select line (S), as in MUX. Since recognize that PMOS performs on ACTIVE LOW and NMOS performs on ACTIVE HIGH. Consequently, while the select line (S) input is low (0) at that point, the PMOS gets triggered, and displays the input D0 in the yield because of low input (0) the NMOS stand idle, since it is triggered in high input. When the select line (S) input is high (1) at that point, the NMOS gets triggered, and displays input D1 in the output. Therefore, this circuitry performs as a 2:1 MUX with Select line (S) choosing the feasible input for the output.

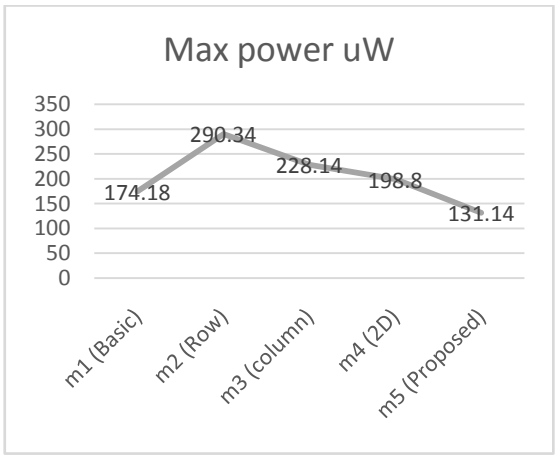
Conventional XOR gate is made-up of 8T CMOS logic that wants above 3 transistors. On the other hand, fig. 6 depicts the design of a XOR gate with three transistors.

IV. SIMULATION RESULTS

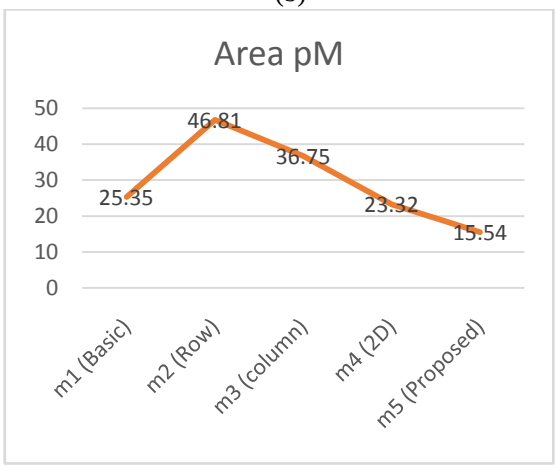
In table I, simulation outcomes are provided for the analysis. The table I provide comparison of Average Power, Maximum Power and Area in basic array multiplier (m1), Digital Row by-passing Multiplier (m2), Digital Column by-passing Multiplier (m3), Digital low power two-Dimensional bypassing Multiplier (m4), and presented low-power high efficiency by-passing 2D Multiplier Design. The Multipliers are simulated in Schematic Editor Tool, the results are compared and analyzed also performance metrics are shown in fig. 7 (a), (b) and (c).



(a)



(b)



(c)

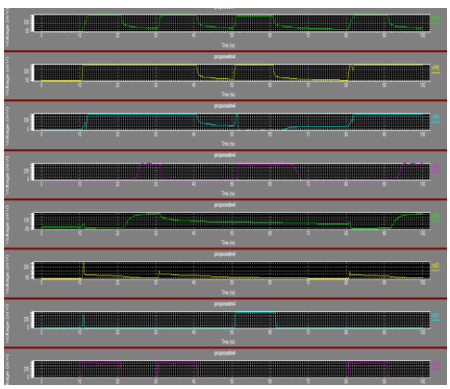


Fig7. 4x4 Output waveform of proposed multiplier design

Table I Comparison Of Proposed Multiplier With Existing Multipliers.

S.No.	Multiplier (4x4)	Avg power uW	Max power uW	Area pM
1	m1 (Basic)	11.16	174.18	25.35
2	m2 (Row)	17.91	290.34	46.81
3	m3 (column)	13.8	228.14	36.75
4	m4 (2D)	12.04	198.8	23.32
5	m5 (Proposed)	7.679	131.14	15.54

From the result Minimum Power Consumption High Efficiency Bypassing-Based 2D Multiplier Design using 65nm CMOS Technologyachieved good power reduction and high performance compare with digital row bypassing based multiplier design, digital column bypassing based multiplier design and digital low power two-dimension bypassing based multiplier design in terms of Average power, Area and Maximum power.

V. CONCLUSION

Dependent upon the easiness of the addition process for a low-power 2D by-passing Multiplier, an Implementation of low-power high efficiency by-passing 2D Multiplier Design was presented. In the consideration of Average power consumptions, Peak power consumption and Area the simulation outcomes shows that our presented multiplier design attains high efficiency and greater power reduction when compared to the other existing multipliers.

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