International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-7 Issue-4, September 2018

A Low Power and High Resolution 2nd Order DT Sigma-Delta Modulator for Data Converters

E. Srinivas, Lakkireddy Jhansi, N. Sharath Kumar

Abstract*: A 2nd order low power and High Resolution discrete time Sigma-Delta modulator presented in this paper for Analog-to-Digital converters (ADC), is developed using CMOS technology. This paper is specifically designed through which it accepts an input signal of frequency 1 KHz, an over sampling ratio (OSR) ≤512 and sampling frequency up to 2MHZ for a second order Sigma-Delta modulator. It is put in to practice in a standard 0.18 µm (180nm) CMOS technology. The design of the sigma-Delta modulator and the simulation of it is done by using CADENCE tools. To form Sigma-Delta modulator this paper essentially elaborates integrator, summer, comparator, D-Latch and Digital-to-Analog (DAC) converters which are integrated together. The key component used in the design is CMOS Operational Amplifier, the OP-AMP open loop gain is 86.8dB, unity gain frequency 5.41 MHz and power consumption is 35.6microwatts. Finally using a ±1.8 v supply voltage a 2nd order Sigma-Delta modulator is realized.

Keywords: Analog-Digital Converters, Op-Amp, Operational Amplifier, Sigma-Delta Modulator.

I. INTRODUCTION

There is a huge demand for analog to digital and digital to analog converters since all the general world signals are in the form of analog signal but digital signal processing is very easy. Compared with all other analog to digital (ADC) converter architectures, sigma-delta analog to digital will have the unique advantage. Nyquist rate and oversampling analog to digital are the two types of available architecture in which delta-sigma analog to digital converter comes under oversampling analog to digital converters. Sharp filters or aliasing filter are can be avoidable by using oversampling technique and signal degradation can be avoided in the central stages using high gain full swing amplifier. Modulator and decimation filter are the major blocks in sigma-delta analog to delta. In sigma-delta analog to digital converter high resolution is the prior factor which is more advantageous among other analog to digital converters.

Design of low voltage and low power modulators are developed to get the required performance of sigma delta modulator. Low power and low voltage high performances are necessary to design the low power and voltage amplifiers. Generally, for 180nm technology the supposed voltage is 1.8V. In low voltage modulators, it is designed with ±700m V which is less than half of the 1.8V voltage and power consumption range should be between 1µ W to some tens of µ W. Using this type of modulator we can achieve accomplished performance in the given band width and resolution performance constraints with low power voltage. The organized manner of this paper is as follows. Block diagram and operation of Sigma-Delta modulator is described in section II. Operational - amplifier design and the power optimization can be discussed in section III. Simulation results of proposed sigma delta modulator and comparison are detailed in section IV. Conclusion and future scope are mentioned in section V.

Revised Manuscript Received on 30 September 2018.
* Correspondence Author
E. Srinivas*, Research Scholar, Jawaharlal Nehru Technological University, Hyderabad (Telangana), India.
Lakkireddy Jhansi, M.Tech Student, Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad (Telangana), India.
N. Sharath Kumar, M.Tech Student, Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad (Telangana), India.

II. BLOCK DIAGRAM

To get digital signals from analog signals we use a technique called sigma-delta modulator, which can be used in ADC's. This modulator can also be used to convert higher bit-count and low frequency into lower bit-count and higher frequency digital signals. Discrete time sigma-delta modulator consists three blocks mainly, they are Sampling circuit, Comparator and DAC.

Sampling circuit: It is used to convert the continuous input an analog signal into sampled signal by using a switch. When the switch is ON signal will be transferred otherwise it will maintain the same level.

Comparator: It will compare the integrator output with the reference signal and provides a compared output.

DAC: For better noise shaping the output signal is provided at the input of second integrator through mixer using DAC feedback loop.

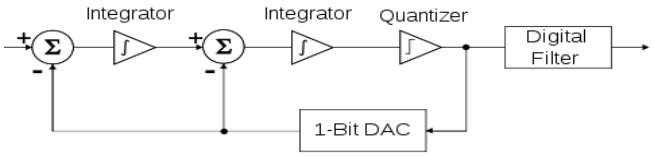

Figure 1: Sigma-Delta Modulator Block Diagram

A. 2nd Order DT Delta Sigma Modulator:

The order of delta-sigma modulator can be depends on the Integrator number, therefore number of feedback loops. First-order modulators are unconditionally stable, but stability analysis must be performed for higher-order modulators.

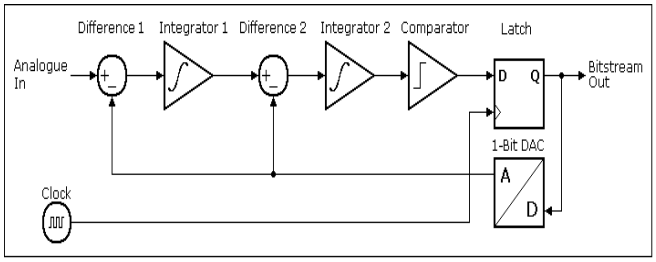

Figure 2: 2nd Order Sigma Delta Modulator Block Diagram

III. OPERATIONAL AMPLIFIER

An operational amplifier (Op Amp) is having multiple stages, which will take the two differential inputs and provides a single ended output. It provides high gain (AV >0.1M), and it also controls the overall output characteristics using a feedback loop.

At the input stage we use a differential amplifier, provides differential inputs and D.C frequency. To provide the input impedance requirements as high for the op-amp, some special methods are used. To provide high gain, high gain voltage amplifier is used at the second stage, provides up to 2×105 gain. To get low output impedance at the final stage we use an output amplifier could be Emitter-follower. It should provide a milli ampere of current to a load. To provide the op-amp output either positive or negative, it has +VCC and –VEE (positive & negative) power supply. Inverting and Non-Inverting terminals are the two input terminals of op-amp. Using these two input terminals, we can use the operational amplifier in three modes, they are: (First mode) with differential inputs, two input terminals are used and two input signals are out of phase by 180o, gives output signal which is in-phase with the Non-Inverting input. (Second mode) At the Inverting terminal input signal is provided and Non-Inverting terminal is grounded, the output signal is 1800 out of phase with the Inverting terminal input signal and the amplitude is half of the first mode output. (Third mode) input signal is applied at the Non-Inverting terminal and the Inverting terminal is grounded, the output is in- phase with the input signal and the amplitude is half of the first mode output.

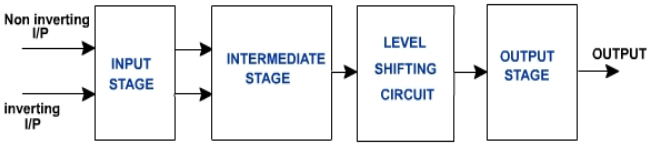

Figure 2: Op-amp General Block Diagram

Input Stage:

CMRR will be increases.
Requirement of high gain can be adjusted.
Very high input impedance can be provided.

Intermediate Stage:

This stage is driven by using the output of 1st stage.
This stage can be used to cancel the error voltage.

Level Shifting:

D.C level can be suppressed to the zero volt with respect to the ground leads to error minimization.
Emitter-Follower used as the current amplifiers.

Output Stage:

Output voltage swing and the current in supply capability of the amplifier can be increased by using this stage.
Low output impedance can be provided.
Using PMOS differential pair or NMOS differential pair the differential gain can be designed.

IV. SIMULATION RESULTS

Two stage CMOS op-amp using PMOS differential pair as follows

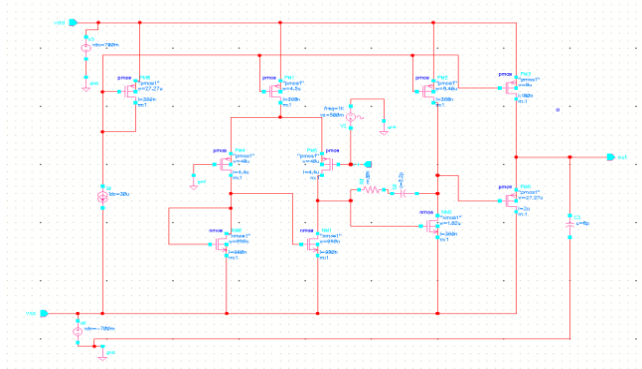

Fig 3: Schematic of PMOS Differential Pair Two Stage CMOS Op-Amp.

Transient, DC and AC response after simulating the above circuit in cadence virtuoso simulator are:

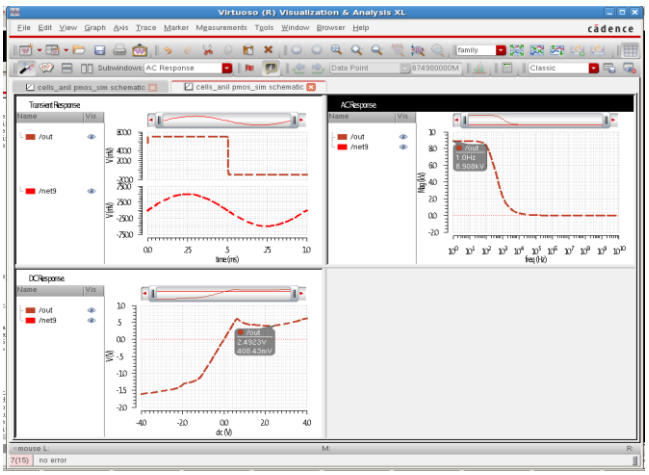

Figure 5: Outputs of PMOS Differential Pair Two Stage CMOS Op-Amp.

Magnitude vs. frequency, phase vs. frequency graphs given by

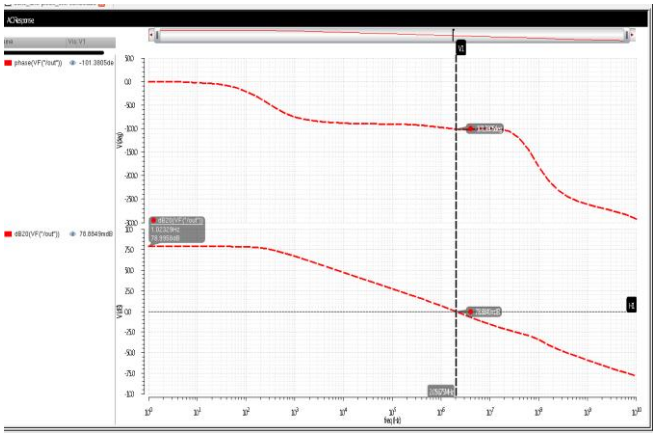

Figure 6: Magnitude & phase plot

Two stage CMOS op-amp using NMOS differential pair as follows

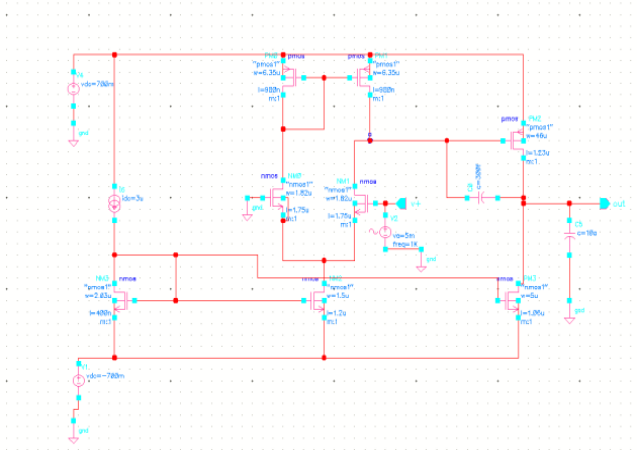

Fig 7: Schematic of NMOS Differential Pair Two Stage CMOS Op-Amp.

Transient, DC and AC response after simulating the above circuit in cadence virtuoso simulator are:

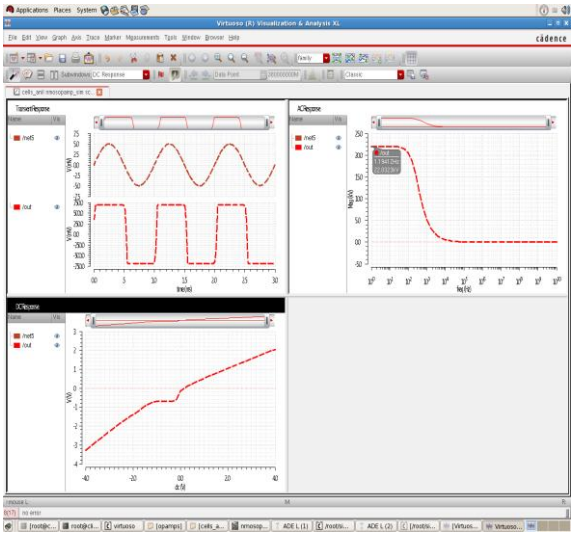

Fig 8: Outputs of NMOS Differential Pair Two Stage CMOS op-amp.

Magnitude vs. frequency graph and phase vs. frequency plot is given by

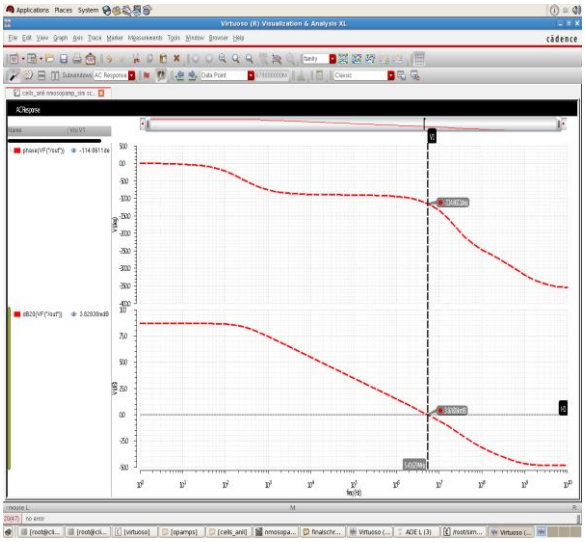

Fig 9: Magnitude & Phase Plot

Comparative analysis simulations results of above two simulated op-amps is given by

Table 1: Comparative Analysis of Two Stage Op-Amps

Specifications	Simulated results of PMOS differential pair Two stage CMOS op-amp	Simulated results of NMOS differential pair Two stage CMOS op-amp
Gain	**78.99 dB**	**86.7dB**
Phase margin	**78.6degrees**	**65.2degrees**
UGF	**2.072MHz**	**5.419MHz**
CMRR	**76.7dB**	**86.58dB**
Power Consumption	**31.53µwatts**	**4.39 µwatts**

By comparing the NMOS and PMOS two stage CMOS operational amplifier circuit, we can say that NMOS differential pair gives the very good results and consumes lower power. So, for further NMOS differential pair is used.

A. Design of Sampling Circuit:

NMOS differential pair two-stage CMOS op-amp is connected as follows to implement the sampling circuit.

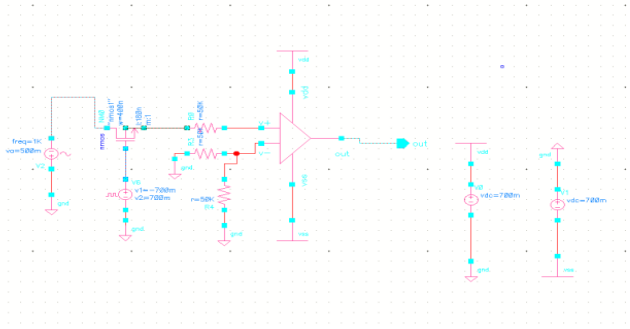

Fig 10: Sampling Circuit Schematic Diagram

By applying a sampling signal (pulse signal) at the transistor gate terminal and input signal at the transistor drain terminal, transistor (NMOS) will be ON when the pulse is high and signal will be transfer from drain to source and the value is in hold, when the pulse is at low. That is shown in fig.

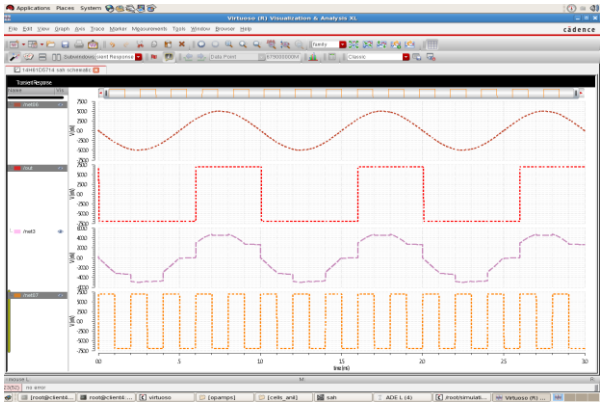

Fig 11: Sampling Circuit Simulated Waveforms

Design of 2nd order DT Sigma-Delta Modulator:
It contains two integrators and two mixers, a comparator and a DAC at the feedback. The suggested schematic diagram of a 2nd order DT Sigma-Delta Modulator is as shown below

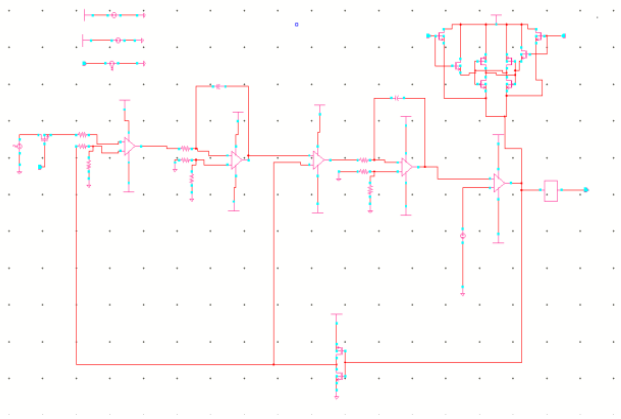

Figure 12: 2nd order DT Sigma-Delta Modulator Schematic Diagram

Simulated transient response is given by

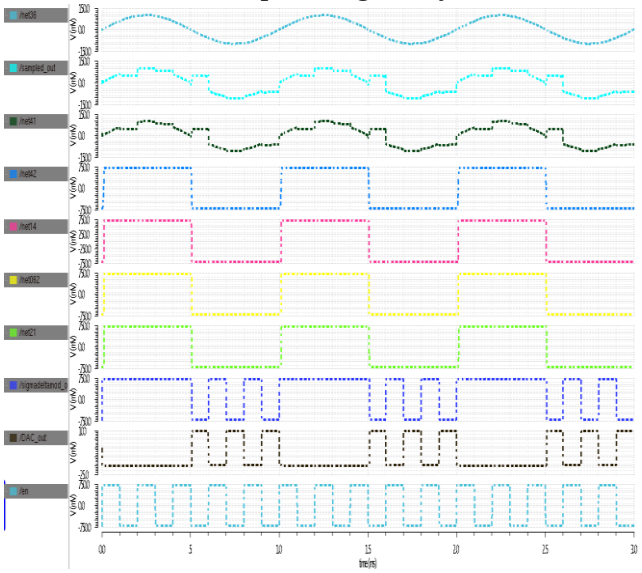

Figure 13: Transient Response of Sigma-Delta Modulator

The Below Table Gives the Simulation Results

Table 2: Tabulation & Comparison of Current Work with Other

S. No.	Parameter	Base paper, (Year)	Paper 2 (Year)	Paper 3 (Year)	This work
1	Technology	180nM	350nM		180nM
2	Power Supply	±900mV	±1.2V		±700mV
3	Input signal	Up to 500Hz	8KHz		1Hz to 2.5KHz
4	Input clock	250KHz	2MHz		2.5KHZ to 2MHz
5	Gain	52dB	40dB		86.8dB
6	Phase Margin		-		65.2
7	UGF		-		5.41MHz
8	CMRR		-		86.58
9	OSR	250	-		1024
10	SNR max	74 dB	81 dB		145.39 dB
11	SNDR	64dB	63dB		70dB
12	ENOB (Effective no. of Bits)	12 Bits	-		23.89 = 24Bits
13	Power consumption	4.6 µwatts	5.6 µwatts		35.6µwatts

V.CONCLUSION

This conclusion section must be included, the 2nd order delta-sigma modulator is designed using CADANCE tool with 180nm CMOS technology. The main block used in this modulator is a operational amplifier with open loop gain is 86.8dB, unity gain frequency 5.41 MHz and power consumption is 35.6microwatts.

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