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Design of RF LNA with Resistive Feedback and Gain Peaking for Multi-Standard Application

S. Radha, D. S. Shylu, P. Nagabushanam, J. Sunitha Kumari

Abstract*: *Low Noise Amplifier (LNA) for 2.4 GHz is the leading block in RF to enhance the performance of the receiver. LNA used in video applications, satellite communications at RF front end of the receiver. Linearity is one of the key requirements for designing LNA, because LNA must exhibit linear operation in the presence of large interfering signals. Some of the existing techniques which improves linearity are Noise cancellation, Derivative superposition, Modified DS technique, body biasing, optimum gate biasing, MGTR, feed forward. The existing challenge in designing a LNA circuit is to achieve high gain, low noise figure and with low power usage without affecting its linearity. This paper analyses variety of linearization techniques that are used for CMOS Low Noise Amplifier (LNA). The LNA methods include (1) single ended LNA (2) PD-LNA (3) capacitive feedback (4) Current-Reuse. We also proposed a Resistive feedback & Gain Peaking technique for LNA using gated inductor at transistor to obtain high gain with low power consumption. Using variety of linearization techniques, the LNA circuits had been designed at 90nm CMOS technology in cadence virtuoso. The resistive feedback and gain peaking LNA gives a gain of 25.4dB with low power consumption of 3.4mv which is better compared to other existing linearization techniques.

Index Terms*: *low noise amplifier (LNA), noise figure (NF), single ended LNA, resistive feedback, capacitive feedback, post distortion linearization technique (PD-LNA), current reuse technique.

I. INTRODUCTION

The necessity of wireless communication have appreciably influenced today's world. The wireless communication is referred as the amendment of data over a large distance without usage of cables or wires. A radio frequency wireless electromagnetic wave that is mainly used as a pattern of communication in which frequency is extended from 3 KHz to 300 KHz. RF circuit is used in cordless phone, Wi-Fi, cellular phone and Bluetooth [2]. The IEEE standards works with three major license free frequency bands that include 860MHz, 960MHz and 2.4GHz. But 2.4GHz is deployed all over the world because it has an advantage of covering longer distance without any loss of signals.

The LNA find its requirement in wireless system and instruments. Any receiver system elementarily consists of three major blocks namely mixer, LNA and filter. Since LNA is used as the basic buildings block in any receiver chain. The system sensitivity is governed by its noise performance and linearity. Basically LNA is an electronic amplifier which can provide adequate amplification of low power signal without degrading its signal to noise ratio and finally helps to boost up the signal strength [4]. Low noise amplifier plays a censorious role in designing an RF front-end receiver, especially the performance of the receiver. The receiver system susceptibility is driven by the noise figure and linearity. The attribute of the LNA determine the apex on the performance of the receiver system. Many circuits with variety of techniques and configuration have been suggested for LNA optimization and designing, in divergent application. LNA integrated with input band selection and capacitive cross coupling give good linearity by improving noise figure and interference rejection [33]. In [31], a low noise logarithmic preamplifier is designed with an active filter to eliminate or limit DC offsets.

The LNA optimization is an entangled task that involves tradeoff among certain parameters like linearity, noise figure and power consumption. There are several linearization methods that are used to optimize the performance of LNA in order to moderate the gain and noise figure of the system. The traditional LNA optimization methods include optimum gate biasing and are used to linearize the circuit but the challenge associated with this technique is to limit the trans conductance at the input stage which results in gain degradation. Another technique, MGTR (multi-gate transistor technique) the prime disadvantage associated with this technique is the weak transistor that is fused with the input and it shrinks the noise figure of LNA [5]. In [3], a commercial products design by following stochastic addressing is discussed. In [14], authors implemented three techniques namely current-reuse, mirror bias and source inductive degeneration technique. The topology used here is two stages. The circuit find its role in video application. In [9], the LNA is designed using two CS-CS stage transistors configuration. This circuit uses current-reuse technique to construct the LNA and the circuit performance is measured at a particular frequency 5.4GHz. This circuit found its application in wireless and satellite communications. In [13], authors used common-gate topology to design the circuit. For providing improved input matching it uses a gain boosting technique.

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The circuit uses common-source amplifier as feedback path and thereby improve the trans conductance of CG and also downgrades the noise parameter. The circuit meets its application in wireless sensor network. The RF LNA linearization technique should be flexible and reliable. In addition, it should retain the gain and noise figure. There are varieties of linearization methods examined in [6].

In [12], the circuit uses common-gate topology. It uses double capacitor cross coupled technique to upgrade the input trans conductance of LNA circuit. The overall power consumption of the LNA circuit is reduced by using current-reuse technique. The circuit is designed in the absence of bulky inductors. Designed in 180nm for a supply voltage of 1.8V the circuit consumes 3.24mW. The circuit meets its application in multiband wireless communication.

In [11], the circuit uses a double feedback structure to enhance the gain of the circuit. This circuit uses noise cancellation and distortion approach to lower the noise figure. This circuit is based on merging of both a common-gate (CG) stage and common-source (CS) stage. The circuit meet its application in biomedical. In [7], the performance comparison of two LNA techniques, a basic cascade LNA and modified cascade LNA is done. The modified LNA technique uses dual common- source transistors and they compare the parameters like noise figure, gain and power consumption with basic cascade LNA. In this method there is 10% improvement in the overall gain and 40% reduction in the noise figure using modified cascade LNA. The modified cascade LNA is designed for 2-3 GHz range. In [8], the circuit uses feedback and balanced topology to design LNA circuit. The balanced topology method employs a hybrid coupler to reduce the output return loss of the circuit. The use of negative feedback topology helps the circuit to enhance the noise figure. This circuit specifically uses 2.4GHz range of frequency. LNA is designed for WLAN front-end applications by using enhancement mode technology.

In [10], a three stage LNA is designed for 0.7V supply. The circuit is operated at a particular frequency range 5.745 GHz. This proposed LNA is designed using transformer-coupling technique that helps to enhance the gain and reduce noise figure of the circuit. This circuit meets its application in wireless local area networks (WLAN) and ISM. In [30], a frequency selective feedback is applied using shunt capacitor which improves noise performance. In [32], an operational amplifier with shunt-shunt configuration is designed with a feedback resistor to increase the gain and decrease noise. A two stage LNA with resistive feedback in first stage give linearity and input matching for wideband operation. By connecting cascade amplifier in second stage with inductive peaking in series and shunt path give high gain and increased bandwidth [35]. By adding substrate resistor and feedback topology, power gain is increased and noise figure is reduced [36]. By frequency transformation and mobility transistor return loss and impedance bandwidth can be improved in LNA [37]. By trans conductance Gm boosting technique, noise cancellation and noise performance improvement can be obtained in LNA [38]. LNA with active loads and noise cancellation, current reuse mitigate the necessity for hogh power requirement [39]. A CG amplifier with gain boosting technique and multiple gated transistor technique is analyzed, a shunt peaking bandwidth extension technique is implemented [40]. A three stage LNA with current reuse, input matching network and multiple gate transistors is implemented using 180nm technology to obtain input matching and high gain [41]. The challenge behind designing RF LNA circuit is to obtain modest gain and lower noise performance with low power usage without affecting its linearity.

In this paper, we designed LNA with resistive feedback and gain peaking technique for RF front end circuit using 90nm CMOS technology in cadence to obtain low noise figure and nominal gain. The prime objection of LNA is to accomplish an enhanced gain and noise figure. Section 2 examines the LNA related work and section 3 discusses the design methodology of variety of linearization techniques. Section 4 gives the design and simulation results of our implementation and section 5 concludes our entire work in this paper.

II. EXISTING LINEARIZATION METHODS FOR LNA

The linearization method that is used for designing a circuit should be simple and reliable. There are different types of LNA methods reviewed in this paper.

2.1 Single Ended LNA

The single-ended LNA schematic diagram is shown in figure 1[15]. The cascading M2 transistor helps to spare the impact of M1 transistor's gate to drain capacitance effect. Additionally, it is used to abbreviate the combined effect of the tuned input with the tuned output. The drain inductor is illustrated using L2 and is used to earn high gain for circuit by fluctuating it with the drain of the M2 transistor. The input matching is given by the source degeneration inductor illustrated using L3. The gate inductor L1 should be selected in such a way that it gives desired input resistance. The R1, R2 and M3 form a bias circuit. The transistor M3 is used to form a current mirror with the transistor M1 and its width is small compared with M1 transistor. By adjusting R2 value the fixed operating point can be acquired. The C1 and C2 forms the DC blocking capacitors.

Component design

Calculation of gate-oxide capacitance (C ox)

$C_{ox}=\varepsilon ox/tox$

$\varepsilon_{ox} = \varepsilon_o * \varepsilon_r$

Where ε_{ox}=permittivity of gate oxide

tox = Thickness of gate oxide

ε_o=Free space permittivity

$\varepsilon_o=8.854*10^{-12}$F/m $\varepsilon_r=3.9$

Hence we get, $\varepsilon_{ox}=3.45*10^{-11}$F/m

So $C_{ox}=3.45*10^{-11}/4.1*10^{-9}$

$=8.42*10^{-3}$F/m^2

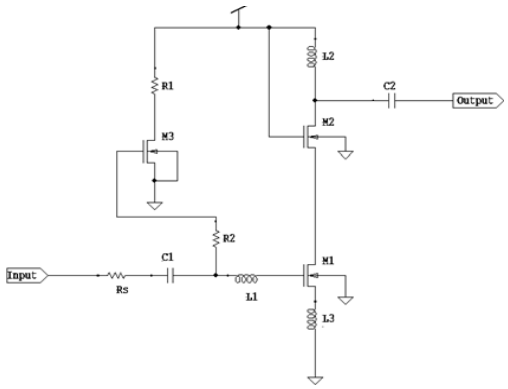

Figure 1.Diagram of Single Ended LNA

2.2 Post Distortion Linearization Technique

The concept behind post distortion linearization technique (PD-LNA) is demonstrated in figure 2. In PD-LNA circuit, the preparatory transistor's non-linearity is abolished by using the secondary transistor's non-linearity [16], [17].

Calculation of optimum width of the transistor M1

$$W_{opt} = 1/(3.C_{ox}.\omega.L.R_S)$$

Where C_{ox}= Capacitance of the gate oxide
ω = Angular frequency
L=Length of the device
R_S= Source Resistance

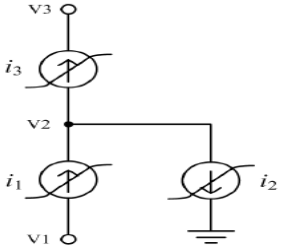

Figure 2 Conceptual idea of PD-LNA

The advantages of PD-LNA includes,

(a) It scales down the influences of input matching by amalgamate the secondary transistor to the output of the primary device rather than amalgamate it to the input of the primary device.

(b) There will be strong exaggeration abolition.

In [18], authors use an active PD-LNA technique where it is used for highly necessary bandwidth application. This linearization method is applied to the dual band cascaded CG-LNA. The circuit found its application on mobile Wi-max. The power utilization of this circuit is high by the additional usage of the parameters.

2.3 Capacitive Feedback Technique

The outlook of capacitive feedback technique is demonstrated in figure 3.

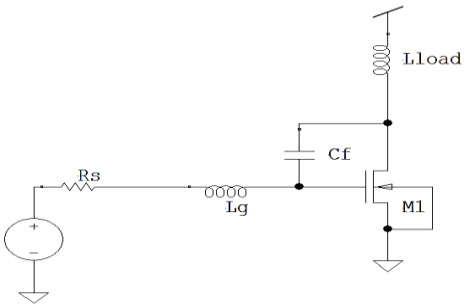

Figure 3 Conceptual view of Capacitive Feedback Method

$$C_f = \frac{2 * Wopt * Cox * L}{3}$$

The benefits of capacitive feedback technique include [19], [20].

(a) Able to provide matching impedance at the input without reckoning the noise.

(b) The noise accomplice with the gate-inductor is being obliterated using capacitive feedback technique.

In [21], an input matching is introduced through the capacitive feedback technique. This circuit is able to earn a 13.2dB gain with a NF of 4.5dB. LNA with resistive shunt feedback and parallel LC load will operate with low power and high gain. By incorporating forward biasing and current reuse technique in second stage LNA can work in low supply voltage with low power consumption [34].

2.4 Current Reuse Technique

In current reuse method, the current generated by the initial transistor will bias the load. It benefits in two facts [22], [23], [24].

(a) It shrinks the total power usage in the circuit and able to earn enhanced gain.

(b) Supply voltage is minimum throughout the circuit.

The conventional current-reuse technique is shown in the figure 4.

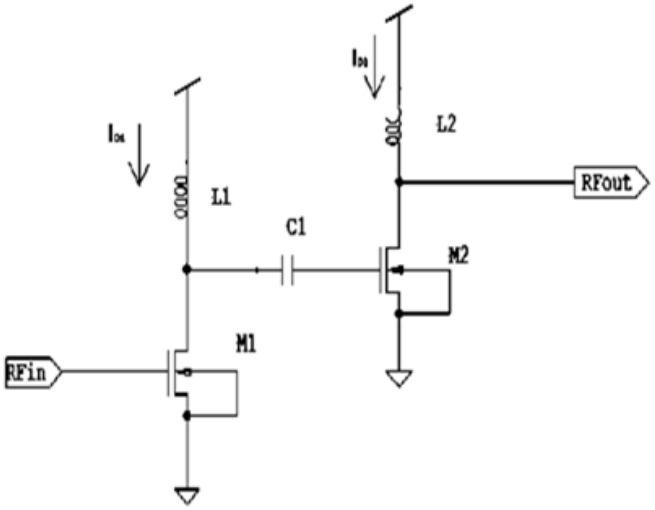

Figure 4 Conventional Current-Reuse Techniques

In [25], the circuit is designed using CS-CS LNA and it uses a current-reuse technique in 180nm technology. The circuit meets its application in satellite communication.

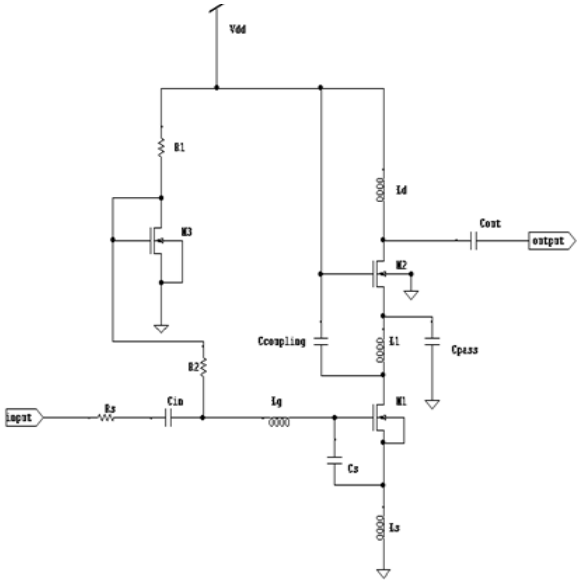

Figure 5 Circuit Implementation of Current-Reuse LNA

However common gate LNA degrades gain and noise figure performance compared to common source LNA.

In this paper we have presented a new technique with resistive feedback and gain peaking which improves gain and noise figure. The small inductor connected to transistor gate compensates gain loss and boost the transistor's trans conductance.

III. DESIGN METHODOLOGY

3.1 Resistive-Capacitive Feedbacks

To amplify the weak signal received by the antenna as well as the noise contribution, the LNA should have a considerable gain. LNA designed using Resistive-Capacitive Feedback gives input matching.

$R_f = 1/(\omega_0^2 * L_g^2 * R_s)$

In [29], authors use a resistive capacitive feedback technique that helps to improve the linearity but the main drawback of the circuit is that the amplifier gain is reduced.

The theoretical idea behind resistive feedback is illustrated in figure 6.

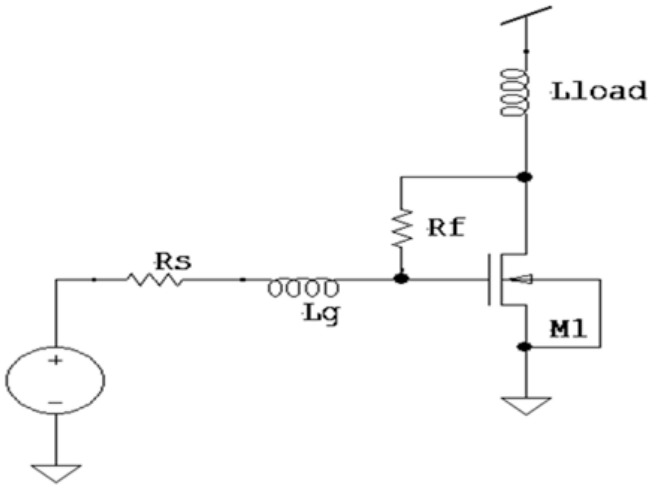

Figure 6 Conceptual view of Resistive Feedback Technique

3.2 Gain-Inductor peaking Technique

The theoretical idea behind gate-inductor gain peaking technique is illustrated in figure 7 [28].

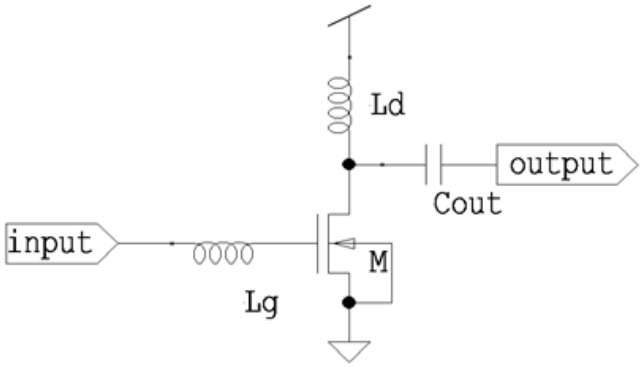

Figure 7 Conceptual Gain Peaking Technique

Gate-inductor Gain peaking technique gives bandwidth enhancement. This technique is advanced in two aspects, [26], [27].

(a) Minimum power supply is required and power consumption of the circuit also reduced.

(b) Lesser noise performance for high sensitivity gain.

(c) Offers matching of the networks.

3.3 Proposed LNA with Resistive Feedback and Gain Peaking Technique

The Resistive feedback and Gain Peaking low noise amplifier (LNA) at 2.4 GHz complete circuit diagram is shown in the figure 8. The Lg, Ld and LS are labeled using spiral inductors. The gate inductor is labeled using Lg. The input capacitance ramification is turned down by using Lg. The degeneration inductor is labeled using Ls and is used for input matching. The Ld labels the drain inductor that earns a better performance LNA by improving its gain. The M2 transistor is used to diminish the communication of tuned input with the tuned output and also it diminishes the gate to drain effect of M1 transistor. The Lg and Ls are the spiral inductors that must be selected in such a manner that it gives the desired input resistance. The transistor M3 along with the resistors R1 and R2 builds the biased circuit. The transistor M3 is used to form a current mirror accompanied by M1 and comparing with M1 its width is small, and that helps to reduce the power utilization of the circuit. The fixed operating point is acquired by adjusting the value of R2. The resistive feedback and gate-inductor gain peaking technique is used in this circuit. A relative small inductor is connected to transistor's gate (Lg2), which boosts transistor's effective trans conductance, compensates gain loss and then leads the proposed LNA with a flat gain and wider bandwidth. Moreover, the LNA′s noise is partially inhibited by the gate inductor, especially at high frequency. The advantage of resistive feedback technique is that it is able to handle large undesired signals without much distortion. The Cin and Cout represents blocking DC capacitors.

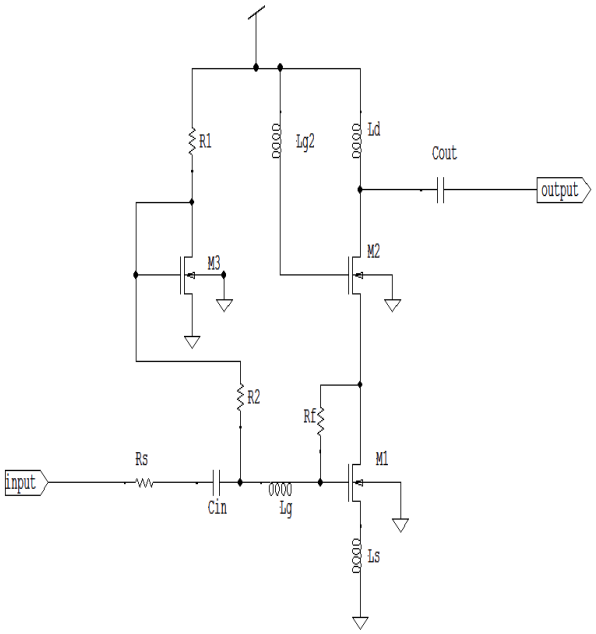

Figure 8 Circuit of Resistive feedback-Gain Peaking Method

IV. SIMULATION RESULTS

The LNA with various linearization techniques was simulated using 90nm RF CMOS technology.

4.1 Single Ended LNA

The schematic diagram of single ended LNA is shown in the figure 9.

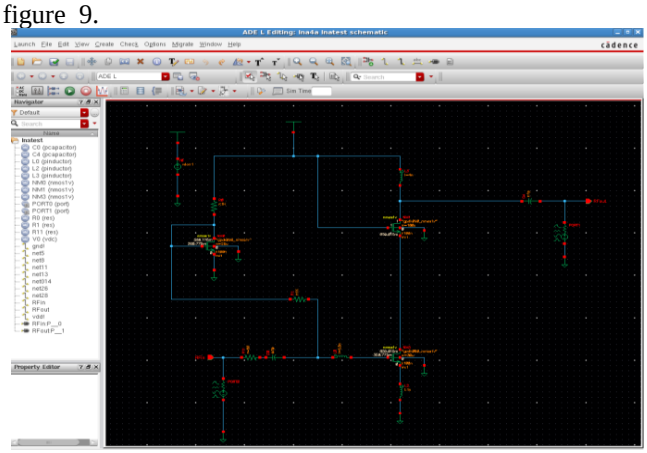

Figure 9 schematic of Single Ended LNA

The noise factor or noise figure represents the noise performance of the LNA and it is nearly 3.8dB for single ended LNA as shown in figure 10. And it gives a gain of 5.5 dB as shown in figure 11. The power obtained for single ended LNA is around 4.8mW as shown in figure 12.

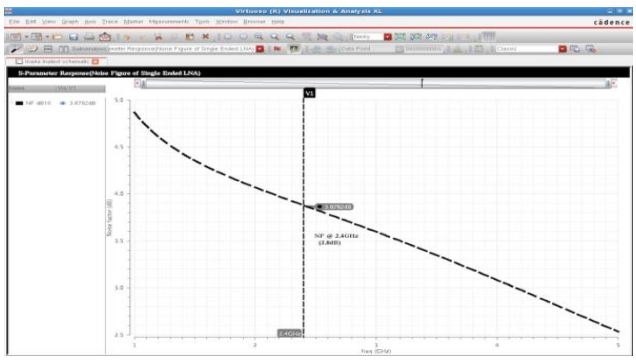

Figure 10 Noise Figure of Single Ended LNA

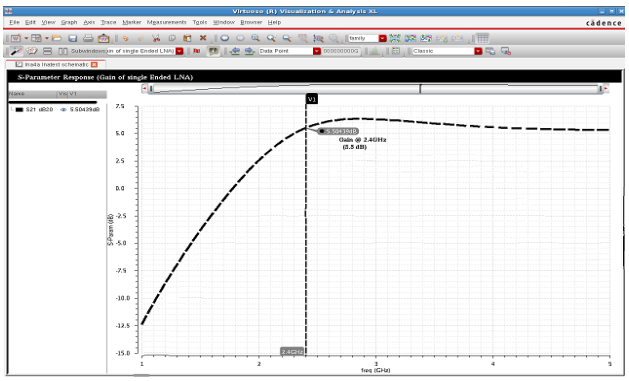

Figure 11 Gain of single ended LNA

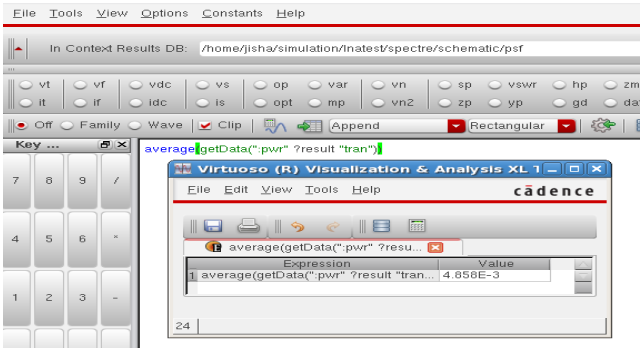

Figure12 power of Single Ended LNA

4.2 Post Distortion Linearization Technique

The schematic diagram of PD- LNA is shown in the figure 13.

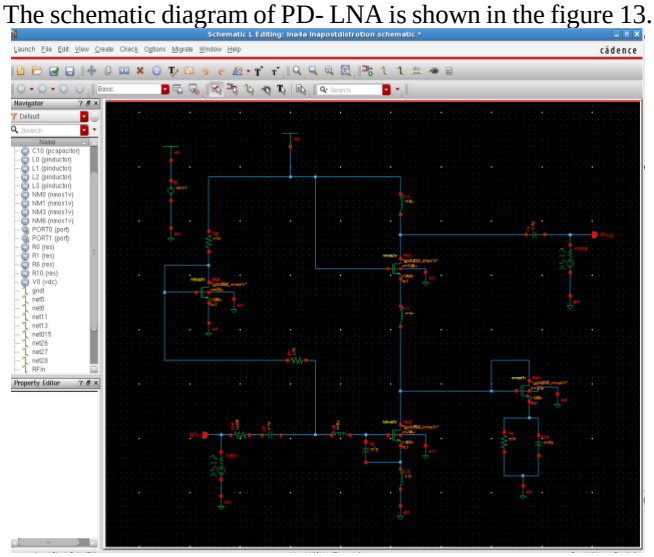

Figure 13 Schematic of PD-LNA

The noise figure obtained for PD-LNA is around 3.4dB as shown in figure 14 and gain obtained for PD-LNA is around 8.7dB as shown in figure 15. The power consumption for PD-LNA is around 14.5mW as shown in figure 16.

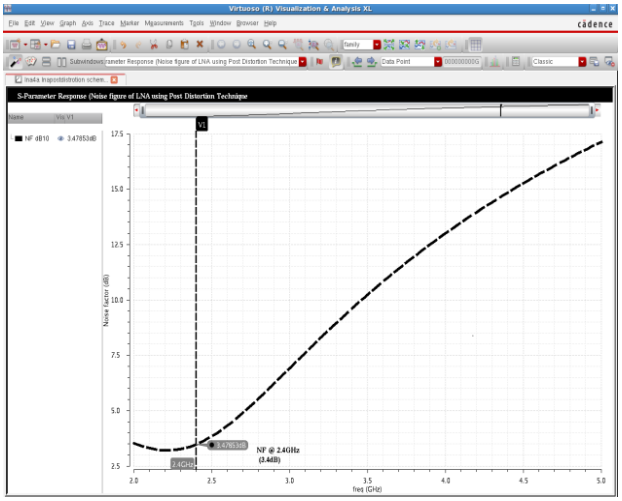

Figure 14 PD-LNA Noise Figure

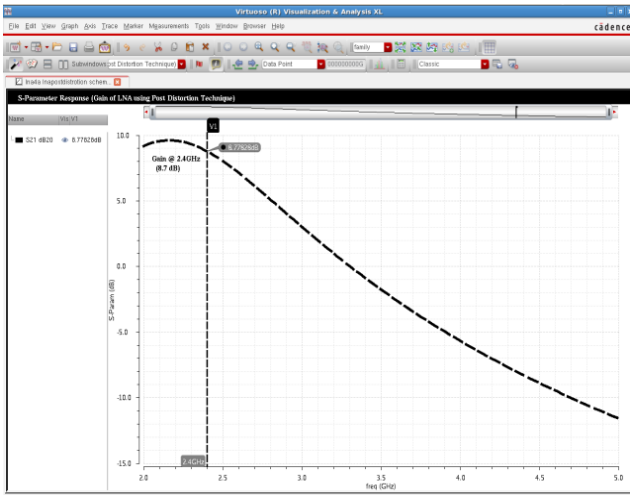

Figure 15 PD-LNA Gain

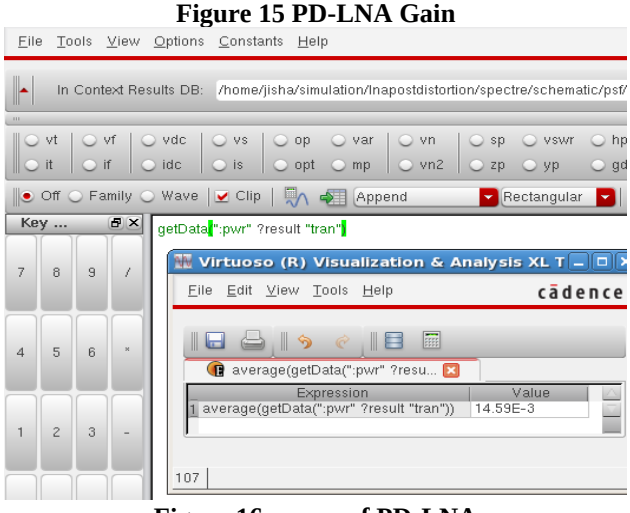

Figure 16 power of PD-LNA

4.3 Capacitive Feedback Technique

The schematic diagram of capacitive feedback LNA is shown in the figure 17.

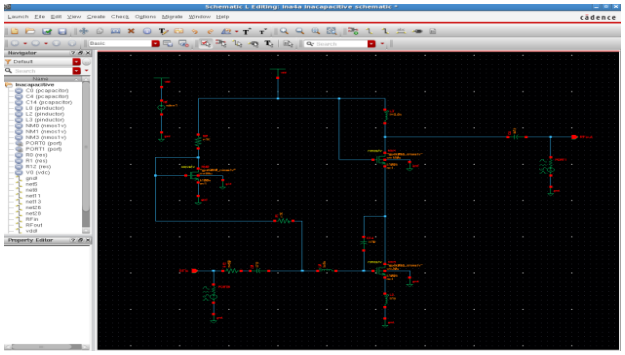

Figure 17 Schematic of Capacitive Feedback LNA

The noise figure obtained for capacitive feedback is around 5.1dB as shown in figure 18 and gain obtained for capacitive feedback LNA is around 4.13dB as shown in figure 19. The power obtained for capacitive feedback LNA is around 6.1mW as shown in figure 20.

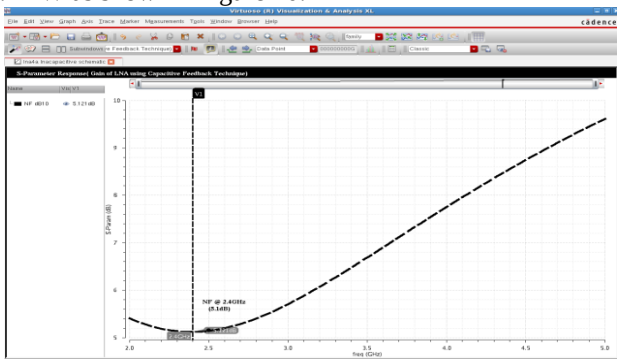

Figure 18 Noise Figure of Capacitive Feedback LNA

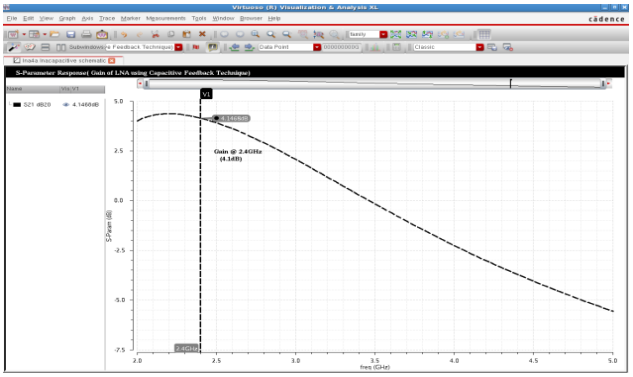

Figure 19 Gain of capacitive Feedback LNA

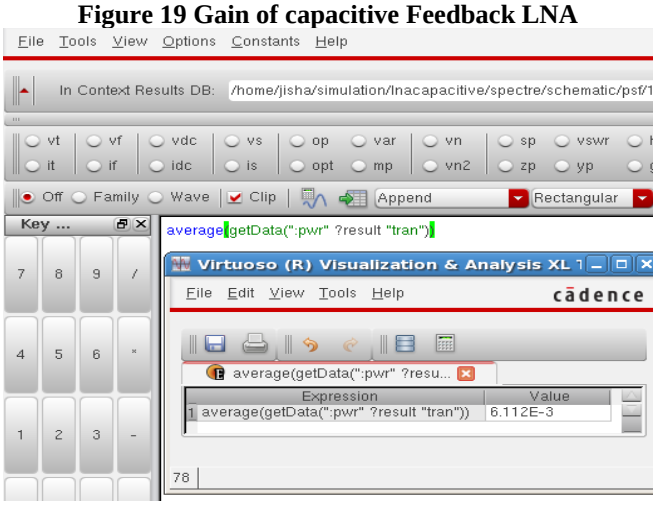

Figure 20 Power of Capacitive Feedback LNA

4.4 Current Reuse Technique

The schematic diagram of current-reuse LNA is shown in the figure 21.

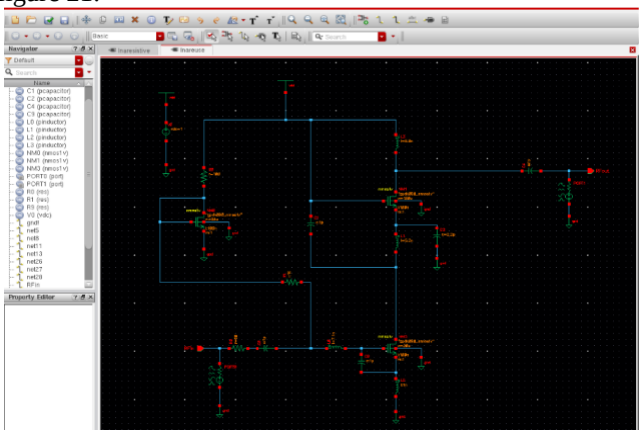

Figure 21 Schematic of current reuse LNA

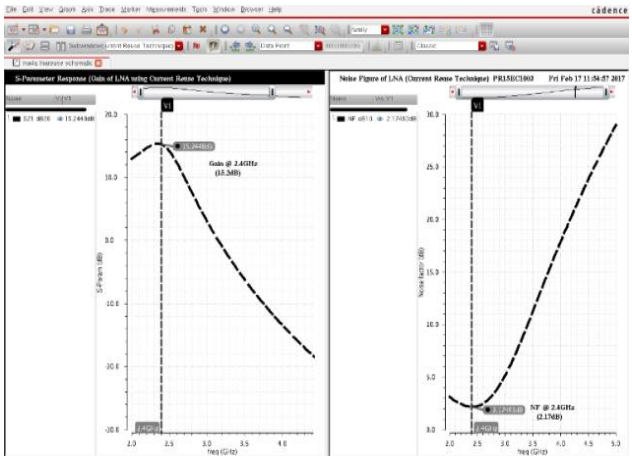

Figure 22 noise figure and gain of Current Reuse LNA

The noise figure obtained for current-reuse LNA is around 2.17dB and gain obtained for current-reuse LNA is around 15.2dB and is shown in figure 22. The power obtained for current- reuse LNA is around 7.14mW.

4.5 Proposed Resistive Feedback & Gain Peaking Technique

The circuit diagram of LNA with Resistive Feedback & Gain Peaking is shown in the figure 23.

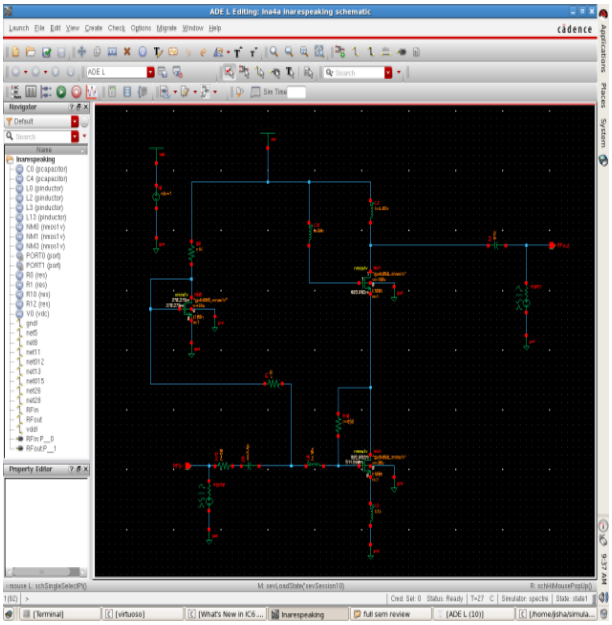

Figure 23 Schematic of proposed Resistive feedback & Gain Peaking LNA

The noise figure of Resistive feedback and gain peaking LNA is around 5.3dB and gain is obtained around 25.4dB and is shown in figure 24. The power of Gain peaking and Resistive Feedback technique is around 3.4mW and it stands lesser than other techniques.

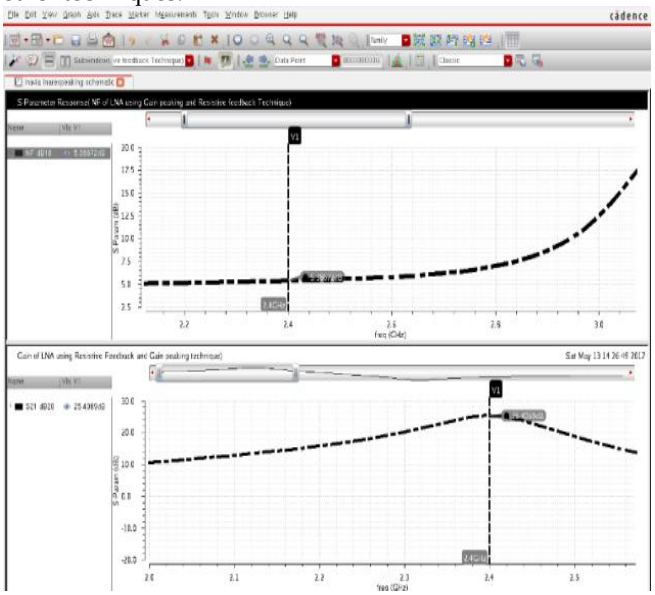

Figure 24 NF and Gain of Resistive feedback & Gain Peaking LNA

4.6 Performance Comparison of various Linearization Techniques.

Table 1 above shows the performance of low noise amplifier using various methods that includes single ended LNA, PD-LNA, Capacitive Feedback LNA, Current-Reuse LNA and Resistive Feedback –Gain Peaking LNA. The power consumption of Resistive feedback-gain peaking LNA is 3.4mv which is lesser Compared to other techniques.

While considering the parameters like gain and noise figure, using resistive feedback-gain peaking technique by a gated inductor, we obtained an adequate noise figure and enhanced gain of 25.4dB which is higher compared to other linearization methods.

Table 1 Analysis of Linearization Methods

Parameters	Single Ended LNA	Post Distortion - LNA	Capacitive Feedback LNA	Current-Reuse LNA	**Proposed** (Resistive Feedback & Gain Peaking LNA)
Gain (dB)	5.5	8.7	4.1	15.2	**25.4**
NF (dB)	3.8	3.4	5.1	2.17	5.3
Power (mW)	4.8	14.5	6.1	7.1	**3.4**
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4
Voltage	1V	1V	1V	1V	1V
process	90nm	90nm	90nm	90nm	90nm

V.CONCLUSION

This paper gives an improved design of LNA circuit using resistive feedback and gain peaking technique which uses a gated inductor to compensate the gain loss and to increase transistor's trans conductance. It is simulated and designed using 90nm CMOS technology in cadence. The prime goal of this work is to attain a high performance LNA design with high gain and minimum power usage. This work is compared with few other divergent grades of CMOS LNA methods like single ended LNA, Post distortion LNA, Capacitive feedback LNA, current re-use LNA ; and it is found that Resistive feedback-Gain Peaking technique is better when compared with other linearization methods for LNA. The Resistive Feedback-Gain Peaking method obtains a gain of 25.4dB and a noise figure of 5.3dB and power consumption of 3.4mW for 1V power supply which shows proposed method has higher gain and lesser power consumption compared to other linearization methods. Depending on the results obtained, the proposed LNA is suitable for multi-standard applications.

REFERENCES

1. Chun-Hsiang Chang, Marvin Onabajo, "A 0.77Mw 2.4GHz RF Front-End with -4.5dBm In-Band IIP3 Through Inherent Filtering", IEEE Microwave and wireless communication, VOL.26, NO.5,PP.352-354,May 2016.
2. BehzadRazavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's", IEEE Journal of solid state circuits,VOL. 34, NO. 10,PP.1382-1385,Oct. 1999.
3. A. Wheeler, "Commercial applications of wireless sensor networks using Zig Bee", IEEE Communication magazine, PP 70-77,April 2007.
4. B. Razavi, "CMOS technology characterization for analogm and RFdesign", IEEE J. Solid-State Circuits, VOL. 34, NO.3, PP. 268–276, Mar. 1999.
5. Bonkee Kim, Jin-Su Ko," A New Linearization Technique for MOSFET RF Amplifier Using Multiple Gated Transistors," IEEE Microwave and Guided Wave Letters, Vol. 10, no. 9, pp. 371-373,Sep. 2000.
6. Heng Zhang, Edgar Sánchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial" IEEE Transactions on circuits and systems,VOL. 58, NO. 1,PP.22-36, Jan. 2011.
7. B. Prameela and Asha Elizabeth Daniel," Design of Low Noise Amplifier for IEEE Standard 802.11b Using Cascode and Modified Cascode Techniques," Procedia Technology, Vol. 25, 2016, PP.443-449.
8. M.H. Misran and ,M.A. MeorSaid," Design of Low Noise Amplifier using Feedback and Balanced Technique for WLAN Application," Procedia Engineering, Volume 53, 2013, PP. 323-331.
9. S. Udaya shankar and M. Davidson Kamala dhas," Design and Performance Measure of 5.4 GHZ CMOS Low Noise Amplifier Using Current Reuse Technique in 0.18µm Technology," Procedia Computer Science,Vol. 47, 2015, Pages 135-143.
10. Mohammed K. Salama, Ahmed M. Soliman," 0.7 V, 5.745 GHz CMOS RF low noise amplifier for IEEE 802.11a wireless LAN," Int. J. Electron. Commun. (AEU), 1434-8411, Vol. 64, PP. 29 – 35, Elsevier, 2010.
11. I. Bastos, L.B. Oliveira," Noise canceling LNA with gain enhancement by using double feedback," Integration, the VLSI Journal,Vol. 52, January 2016, PP. 309–315.
12. Jun Chen, Benqing Guo," An inductorless wideband common-gate LNA with dual capacitor cross-coupled feedback and negative impedance techniques,"Integration, the VLSI Journal,Vol. 56, January 2017, PP. 53–60.
13. Atiyeh Karimlou, Roya Jafarnejad," An Inductor-less Sub-mW Low Noise Amplifier for Wireless Sensor Network Applications," Integration, the VLSI Journal,Vol. 52, January 2016, PP. 316–322.
14. San-Fu Wang, Yuh-Shyan Hwang," A new CMOS wideband low noise amplifier with gain control," Integration, the VLSI Journal,Vol. 44, Issue 2, March 2011, PP. 136–143.
15. Z. Li and K.K. O, "Packaged single-ended CMOS low noise amplifier with 2.3 dB noise figure and 64dBm IIP2,"Electronics Lett., vol. 40, no. 10, 2004, pp. 712–713,.
16. Benqing Guo and Xiaolei Li,"A 1.6–9.7 GHz CMOS LNA Linearised by Post Distortion Technique,"IEEE Microwave and wireless components letters,vol.23, no. 11,Nov. 2013, pp.608-610.
17. N. Kim, V. Aparin, K. Barnett, and C. Persico, "A cellular-band CDMA CMOS LNA linearized using active post-distortion,"IEEE J. Solid-State Circuits, vol. 41, no. 7,Jul. 2006, pp. 1530–1534.
18. Abolfazl Zokaei, Amir Amirabadi," A 0.13µm dual-band common-gate LNA using active post distortion for mobile Wimax," Microelectronics Journal 45 (2014) 921–929.
19. F.-T. Chien and Y.-J.Chan, "Bandwidth enhancement of transimpedance amplifier by a capacitive-peaking design," IEEE J.Solid-State Circuits, vol. 34, no. 8,Aug. 1999, pp. 1167–1170.
20. Y. Lin, H. Chen, T. Wang, Y. Lin and S. Lu, "3-10GHz Ultra-Wideband Low-Noise Amplifier Utilising Miller Effect and Inductive Shunt-Shunt Feedback Technique," IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No. 9, Sep. 2007,pp. 1832–1843.
21. Fadi Riad Shahroury , Chung-Yu Wu," A 1-V RF-CMOS LNA design utilizing the technique of capacitive feedback matching network," Integration, the VLSI Journal, Vol. 42, Issue 1, Pages 83–88, Jan. 2009.
22. Muhammad Khurram and S. M. RezaulHasan,"A 3–5 GHz Current-Reuse gmBoosted CG LNA for Ultrawideband in 130 nm CMOS,"IEEE Techniques, vol. 52, no. 5, May 2004, pp. 1433-1442.
23. A. Selvakumar, M. Zargham, and A. Liscidini,"Sub-mW current reuse receiver front-end for wireless sensor network applications," IEEEJ. Solid-State Circuits, vol. 50, no. 12, Dec. 2015, pp. 2965–2974.
24. Hyouk-Kyu Cha, M. KumarasamyRaja,"A CMOS MedRadio Receiver RF Front-End With a Complementary Current-Reuse LNA,"IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 7, July 2011,pp.1846-1854.
25. S.Udayashankar ,M.Davidson Kamala dhas," Design and Performance Measure of 5.4 GHZ CMOS Low Noise Amplifier using Current Reuse Technique in 0.18µm Technology," Procedia Computer Science,vol.47,2015,pp.135 – 143.
26. T. Chang, J. Chen, L. A. Rigge, and J. Lin, "ESD-protected sideband CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging,"IEEE Trans. Microw. Theory Tech, vol. 56,no. 5, Aug. 2008, pp. 1817–1826.
27. D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," IEEE J. Solid-State Circuits, vol. 32, no. 5, May 1997, pp. 745–759.
28. H.-K. Chen, D.-C.Chang, Y.-Z.Juang, and S.-S. Lu, "A compact wideband CMOS low-noise amplifier using shunt resistive-feedback and series inductive-peaking techniques ,"IEEE Microw. Wireless Compon.Lett.,vol. 17, no. 8,Aug. 2007, pp. 616–618.

29. Amir Nakhlestani, Ahmad Hakimi," A novel configuration for UWB LNA suitable for low-power and low-voltage applications," Microelectronics Journal, Vol. 43, Issue 7 , July 2012, pp. 444–451.
30. Tae Hwan Jin, Hong Gul Han, Tae Wook Kim, "A 0.7-dB NF, +8.2-dBm IIP3 CMOS low noise amplifier using frequency selective feedback", International Journal of Circuit Theory and Applications, Volume 44, Issue 1, January 2015.
31. Zahra Haddad Derafshi, Javad Frounchi, "Low-noise low-power front-end logarithmic amplifier for neural recording system" International Journal of Circuit Theory and Applications, Volume 42, Issue 5, April 2014.
32. Gino Giusi ,Gianluca Cannatà, Graziella Scandurra, Carmine Ciofi, "Ultra-low-noise large-bandwidth transimpedance amplifier" International Journal of Circuit Theory and Applications, Volume 43, Issue 10, August 2014.
33. Jhen-Ji Wang, Duan-Yu Chen, San-Fu Wang, Rong-Shan Wei, "A multi-band low noise amplifier with wide-band interferencerejection improvement", International Journal of Electronics and Communications (AEÜ), 1434-8411, Elsevier, ,2015.
34. Qiuzhen Wan, Qingdi Wang, Zhiwei Zheng, "Design and analysis of a 3.1–10.6 GHz UWB low noise amplifier withforward body bias technique", International Journal of Electronics and Communications (AEÜ), 1434-8411, Elsevier, 2014.
35. A.I.A. Galala,∗, R. Pokharelb, H. Kanayaa, K. Yoshida, " High linearity technique for ultra-wideband low noise amplifier in 0.18 m CMOS technology", International Journal of Electronics and Communications (AEÜ), 1434-8411, Elsevier, 2012
36. Chun-Yi Lin , Ching-Piao Liang, Jenn-Hwan Tarng, Shyh-Jong Chung," Compact composite noise-reduction LNA for UWB WPAN and WBAN applications", The Institution of Engineering and Technology 2017, ISSN 1751-8725, Vol. 12 Iss. 6, pp. 903-908, IET Microwaves, Antennas & Propagation, 2018.
37. Ramya Vijay, Thipparaju Rama Rao, "Design of penta-band antenna with integrated LNA circuit for vehicular communications", The Institution of Engineering and Technology 2017, ISSN 1751-858X, Vol. 12 Iss. 3, pp. 221-225, IET Circuits, Devices & Systems, 2018.
38. Muyeon Lee, Ickjin Kwon, "3–10 GHz noise-cancelling CMOS LNA using gm-boosting technique", The Institution of Engineering and Technology 2017, ISSN 1751-858X, Vol. 12 Iss. 1, pp. 12-16, IET Circuits Devices Syst., 2018.
39. R. Eskandari, A. Ebrahimi, J. Sobhi, "A wideband noise cancelling balun LNA employing current reuse technique", Microelectronics Journal, 0026-2692, Elsevier, 2018.
40. AliSahafi, JafarSobhi, ZiaddinDaeiKoozehkanani, "Linearity improvement of gm-boosted common gate LNA: Analysis to design", Microelectronics Journal, 0026-2692, Elsevier, 2016.
41. Guoxiao Cheng, Zhiqun Li, Lei Luo, Zengqi Wang, Xiaodong He, Boyong He, "A low power and high gain current-reused LNA using cascaded L-type input matching network", Microelectronics Journal, 0026-2692, Elsevier, 2018.