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Analysis of Current Steering Digital to Analog Converter

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Abstract: ***The current steering Digital to Analog Converter (DAC) with a Digital random return to zero technique in order to improve the namic performance is presented in this research paper. In order to demonstrate the proposed technique, an 8 bit CMOS DAC is designed and the layout is prepared in 90 nm technology. The chip layouts run on low power and have small area overhead.***

Keywords: DAC, Current Steering, Converter

I. INTRODUCTION

Current Steering DAC means the current DAC. As compared to other DAC current steering DAC are faster and consumes less power. A wide range of digital-to-analog converters (DAC) exists; each has its own advantages. The DAC can be categorized into R2R ladder DAC, Delta-Sigma DAC, Segmented DAC, Binary weighted DAC, Current Steering DAC. The Binary weighted DAC, R2R ladder DAC, Delta-Sigma DAC has a disadvantage of medium conversion rate. The current-steering DAC can achieve a high conversion rate and thus are used in high frequency signals [1][2][3]. Figure 1 shows a generic form of the current steering DAC. There is Z equally weighted current cells each with I_u as the output current. Each current cell has a pair of p-channel MOSFET's functioning as a current switch and a clock CK driven latch. The complementary output of the latch controls the current switch directing the current I_u to either the loads R_L at V_{o1}or at V_{o2}. The decoder converts the digital input $L_i[k]$ into Z thermometer-code $T_j[k]$ signals where $1 \leq j \leq Z$, such that $L_i[k] = \sum_{j=1}^{M} T_j[k]$. The $T_j[k]$ signal has the binary value of either (+1) or (-1) [2][3][4]. Figure 2 illustrates the DAC differential non-return-to-zero (NRZ) waveform where the output voltage V_o is given by V_{o1}-V_{o2}. The V_o voltage range is in between $+ZI_uR_L$ and $-ZI_uR_L$ with a step size of $2I_uR_L$. The static linearity of DAC which is specified as the Differential Non-Linearity (DNL) and the Static Non-Linearity (INL) is determined by matching of I_u among the different current cells and the output resistances of I_u current sources. The Return-to-Zero (RZ) technique has been proposed in order to improve the DAC dynamic performance [1][2][3][4].

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The proposed technique adds an output buffer in order to isolate the loads from the current switches and executes the current switching operation during the zero phases. In this brief article, a digital random return to zero (DRRZ) technique has been proposed in order to minimize the effect of the switching transients on the DAC dynamic performance [5].

An 8 bit 1.6 Gs/S current steering DAC is designed. Figure 1 shows the generic form of the current steering DAC. It consists of $2^N - 1$ current cells of constant I_u output current. Each current cell consists of a clock CK driven latch, a pair of p-channel MOSFET functioning as a current switch and a constant current source. Each latch is driven by CK with an input from the encoder. The complementary outputs of the latch drive the PMOS [1][3][4].

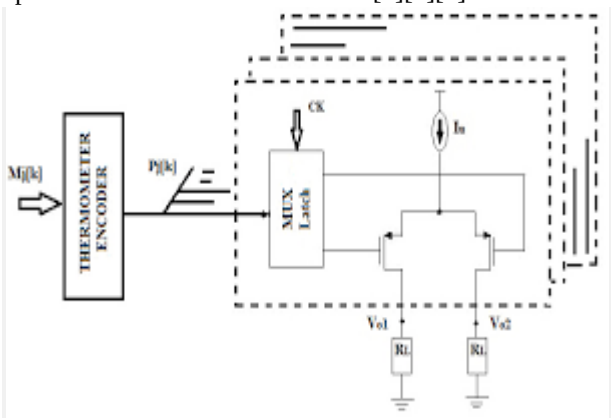

Figure 1 Current Steering DAC Generic Form

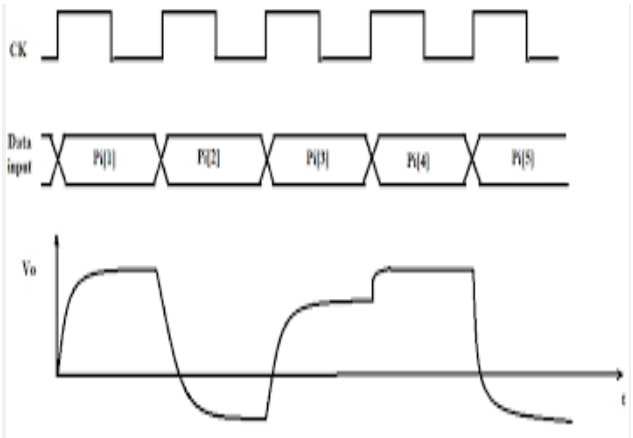

Figure 2 Non Return to Zero Output Waveform of a Current Steering DAC

II. DYNAMIC RANDOM RETURN TO ZERO TECHNIQUE

Wherever consider the jth current cell of the DAC shown in Figure 3, where the current switch is driven by $T_j[k] = \{-1,+1\}$. When the clock CK changes from low to high, the current switch may

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remain unchanged or make the switching from (+1) to (-1) or from (-1) to (+1) [2][3][4]. When the current switch makes a switching, the DAC output V_o experiences a transient disturbance called as the switching transient. The switching transients (-1) to (+1) and (+1) to (-1) have the opposite polarities. In the NRZ DAC, the switching of the current cell is determined by the input $L_i[k]$ [3][4][5]. Thus, the switching transition are the input dependant and will result in the DAC dynamic distortion. Figure 4 shows the proposed DRRZ scheme waveform which randomizes the switching transients appearing in the DRZ. In this scheme, a pseudo random number generator (PRNG) is used to randomize $F_j[k]$ in the Z[k] phase such that $\sum_{j=1}^{M} F_j[k] = 0$.Consider the jth current cell and the operation sequence which is shown in Figure 3 [2][3][5]. When the clock CK is high, $T_j = T_j[k]$ is determined by the input $L_i[k]$. When the clock CK is low, $T_j[k] = F_j[k]$ becomes a binary random variable which has a value of either (+1) or (_!). In the waveform shown in Figure 3, the $T_j[1] = -1$ and $T_j[2] = -1$ has the same value thus switching transitions occurs only if $F_j[1] = +1$. Also from the waveforms shown in Figure 4, $T_j[2] = -1$ and $T_j[3] = +1$ have different values thus the switch transition occurs only at the right edge of R[2] phase if $F_j[2] = -1$or the switch transition occurs at the left edge of the R[2] phase if $Z_j[2]= +1$ [2][3][5]. Thus, the DRRZ scheme makes $Z_j[k]$ a random sequence, randomizing the transition scheme of the current switches. Thus, the switching transients become independent of the input $L_i[k]$ and will not cause distortion [2][3][5]. Figure 5 shows the block diagram of the proposed DRRZ scheme. It consists of 8 bit thermometer decoder, pseudo random number counter (PRNG) and 35 current cells. It is divided into 5 bit equally weighted most significant bit (MSB) DAC (M-DAC) comprising of 31 identical current cells each output current of 81 and 3 bit binary weighted Least Significant Bit (LSB) DAC (L-DAC) comprising of four different current cells with an output current of value 1I, 1I, 2I and 4I respectively [3][4][5]. There are two 1I current cells in L-DAC so that a differential output of zero can be realized. The nodes i_{o1} and i_{o2} of all the current cells are tied together in order to forma two differential DAC output terminals [2][4][5]. This two output terminal is connected to two R_L in order to generate the output voltage V_{o1} and V_{o2}. When the clock CK is high, the decoder controls both the M-DAC and the L-DAC [4][5]. The DAC output is expressed as $V_{ok} = (L_i[k] – 127) \times 2IR_L$, where I = 80 µA and R_L = 25 Ohms yields V_o with a differential signal range of 1 V_{pp} [3][5].

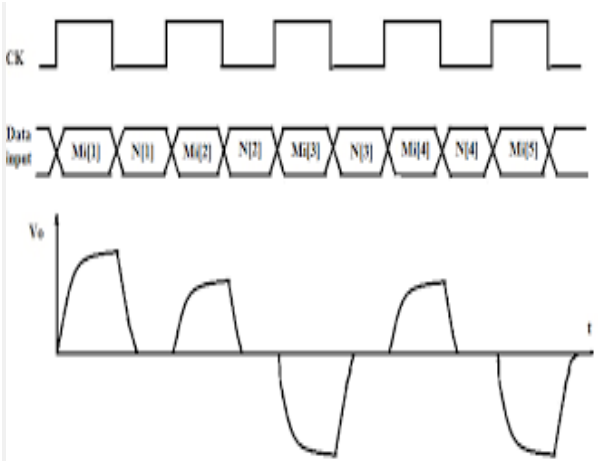

Figure 3 Waveform of Return to Zero DAC

Each current cell consists of multiplexing (MUX) latch. When the clock CK goes high, the latch selects the $T_j[k]$ control from the $L_i[k]$ decoder for a normal DAC output. When the clock CK goes low, the latch selects the $F_j[k]$ control from PRNG. The decoder is a 8 bit thermometer decoder and the PRNG is a 16 bit linear shift register [4][5]. Its 16 outputs and their complements form the 32 $F_j[k]$ zero-phase controls. This arrangement ensures that $\sum_{j=1}^{32} F_j[k] = 0$. During the zero phase the entire L-DAC is treated as a single MSB current cell which is controlled by a single $F_{32}[k]$ signal [2][3][4]. Figure 6 shows the schematic of a current cell. The MOSFET C1 and C2 form the cascade current source. The MOSFETC3 and C4 function as current switches. The current source is operated at 2.5 Volts supply. The MOSFET A11-A18 and two inverters form a level-sensitive MUX latch [5]. When the clock is high, the $T_j[k]$ signal corresponding to $L_i[k]$ signal to the decoder is loaded into the latch [1][3][4]. When the CK is low, the $F_j[k]$ signal from the PRNG is loaded into the latch. For example, when $T_j[k] = 1$, then the current switch C3 is ON. The whole MUX latch is operated under the 1.2 Volts power supply [1][2][5].

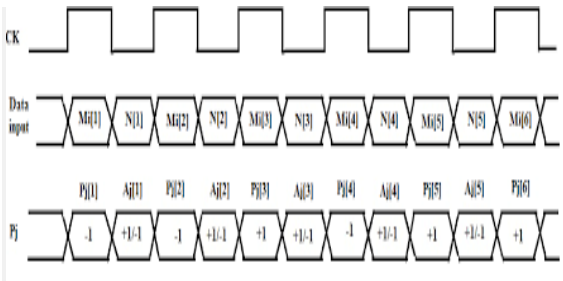

Figure 4 Switching Behavior of Current Cell in Dynamic Random Return to Zero DAC

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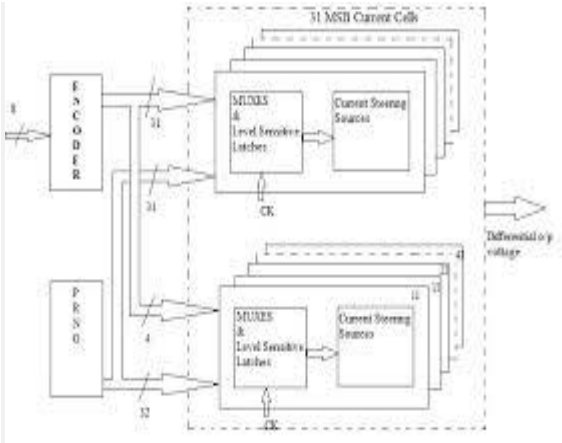

Figure 5 Block Diagram of Current Steering DAC

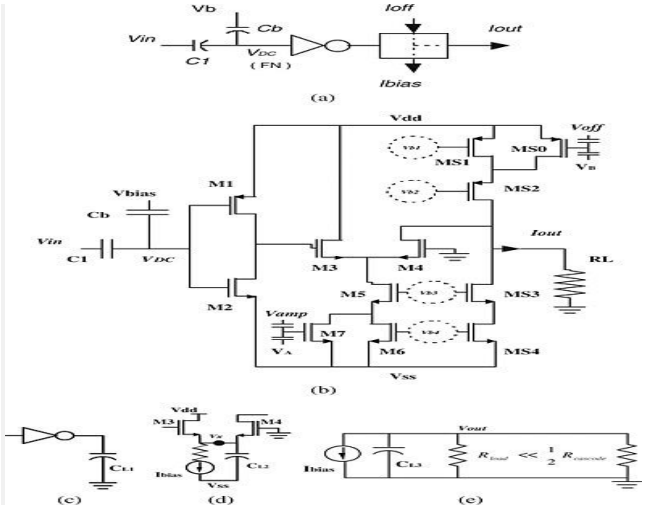

Figure 6 Schematic of a Current Cell

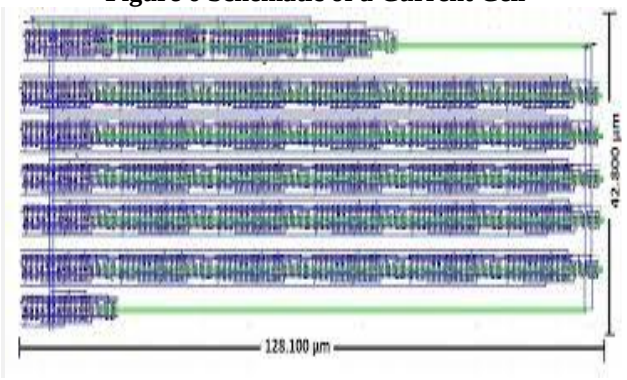

Figure 7 Layout of Current Steering DAC

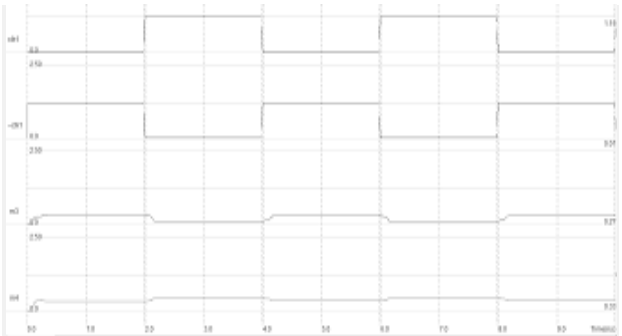

Figure 8 Output Waveform of Current Steering DAC

Table 1 DAC Performance Summary

Technology	CMOS 90 nm
Sampling Rate	1.6 GS/second
Resolution	8 bit
Load Current	19 mA
Output Swing	1 V_{pp}
Supply Voltage (Analog/Digital)	2.5 V/1.2 V
Total Power Consumption	57 mW
Core Area	5483 $(\mu m)^2$

III. CONCLUSION

The DAC has been prepared in the standard 90 nm CMOS technology. The prepared layout for the same is shown in Figure 7. The DAC core area is 5598 μm^2. Figure 8 shows the output waveform of the DAC for an input $D_i[k]$ of 00001100 and for this the power consumption is of 51 mW. Table 1 gives the performance summary of the DAC.

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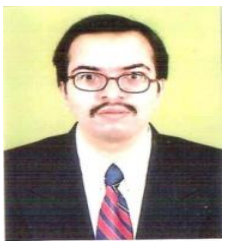
AUTHOR'S PROFILE



Mr. Abhinav V. Deshpande, My name is Mr. Abhinav V. Deshpande. I have done B. E. in the branch of Electronics & Telecommunication Engineering from G. H. Raisoni College of Engineering, Nagpur in the year 2010 with an aggregate of 63%. I have also done M. Tech. from the same institute in the branch of Electronics Engineering in the year 2012 with a CGPA of 7.90 on a scale of 10.00. I have also passed the Ph. D. Entrance Test (PET) which was conducted by RTM Nagpur University in the years 2013 as well as 2015 with a valid scores of 55 marks and 55.75 marks out of 100 marks respectively. I have also passed the Ph. D. Entrance Test (PET) which was conducted by Gondwana University, Gadhchiroli in the year 2015 with a valid score of 51 marks out of 100 marks respectively. I have published 32 research papers in different International Journals and 1 research paper is presented as well as published in International Conference. I have also published 1 book which was published by Lambert Academic Publishing (LAP) Publishing House in Saarbrucken, Germany in the year 2012. I worked previously as an Assistant Professor on Contract Basis in the Department of Electronics & Telecommunication Engineering at Prof. Ram Meghe Institute of Technology & Research, Badnera, Amravati-444701 for 1 year. I am having the memberships of different and reputed Professional Organizations to my credit. I want to do Ph.D. in the branch of Electronics Engineering since I am very much interested in the domain of research and development in the core branch of Electronics Engineering and want to take up the sector of R & D as a future career option.

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