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High Speed EX_NOR Gate At 22nm High K Metal Gate Strained Si Technology Node

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***Abstract*— The propagation delay of the normal Ex_Nor circuit is calculated to be ---with reverse body bias. Also the propagation delay of the same exnor circuit is calculated with its body bias forward biased of Vdd/2. With forward body bias the propagation delay is reduced by 55.89% and this high speed Exnor circuit finds its application where power penalty is acceptable.**

***Index Terms*—22nm, high speed, X-nor gate, X-or gate.**

I. INTRODUCTION

In today's scenario it is necessary to have low power and high speed circuit. Sometimes only either of the two qualities is sufficient, which means either only high speed or only low power circuit. Due to increased need of small devices like mobile phone etc, power consumption/dissipation is becoming important parameter to be optimized as well as area and speed [1].Research paper [2] explores power consumption in XOR and EX-Nor dominated logic. It says that all the inputs that are sensitizing in-outs, XOR gates become more testable. But from power dissipation point of view, this property can be a drawback.

There is always a switching transition at the output, whenever switching transition takes place at the input of ex-or/ex-nor gates. In general circumstances, switching activity is more in XOR (and hence in x-nor) dominated circuits. It was stated that power dissipation is dependent on the actual implementation of logic gates. There is large difference depending on whether x-or/x-nor gate is implemented as basic gate or complex gate. There are xor gates with two inputs and 8 transistors in all. Other types of xor logic gates are made of complementary pass logic and has 4 transistors and is popular design. There are designs in which xor gate is made of mix of pass logic and static cmos style.

The area of xor gate in both the above implementation can be compared with two input nand or nor gate [2].That is why it is more wise to model xor gate as basic one. For large fanin complex gate, one should consider the internal capacitance of the logic gate but also consider the power consumption for charging and discharging of the output node. In static NAND gate, let A=1 and B=0 at time to, where B is the transistor close to the ground and A is the gate of transistor close to the output node. In this condition the output node is charged to high and also the internal node (the node between transistor with A gate and transistor with B gate). At t1 when A=0 and B=1, the internal node (the node between transistor A and transistor B) is discharged to low voltage and the output node continues to be at high voltage. When A=1 and B=0 at time t2, the internal node voltage Vint is charged to high voltage. Thus internal voltage at the internal capacitance is getting charged and discharged in three cycles of the clock, even though there is no transition at vout.

II. EXPERIMENTAL SETUP AND SIMULATION

The following circuit is taken as the experimental circuit. The output is taken at the output of ExNor circuit. The output is noticed with normal reverse body biased ExNor circuit and also with forward body biased (biasing of 0.45V=Vdd/2).

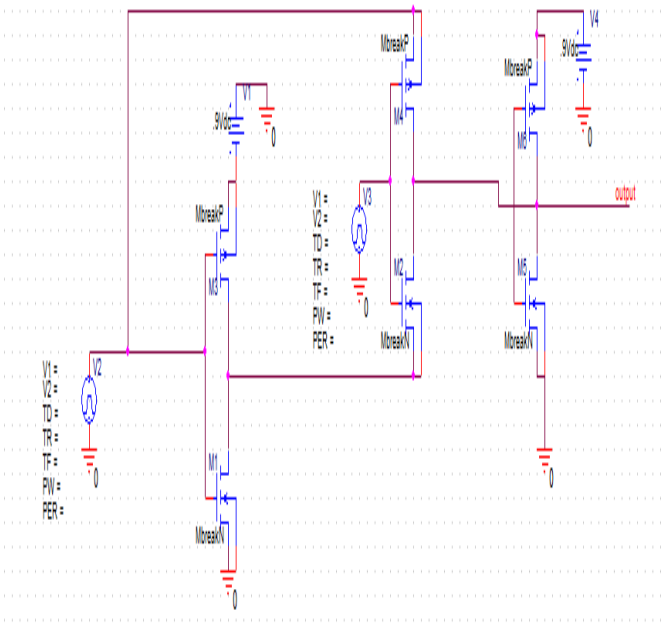

Table I below shows the comparison of propagation delay of the circuit with reverse body bias and with forward body bias of Vdd/2.

TABLE I of ExNor circuit

Parameters	Exnor with reverse Body Bias	Exnor with forward Body bias
Propagation delay(ps)	34.605	14.226

Waveform of Exnor with reverse Body Bias is shown below in Fig.2

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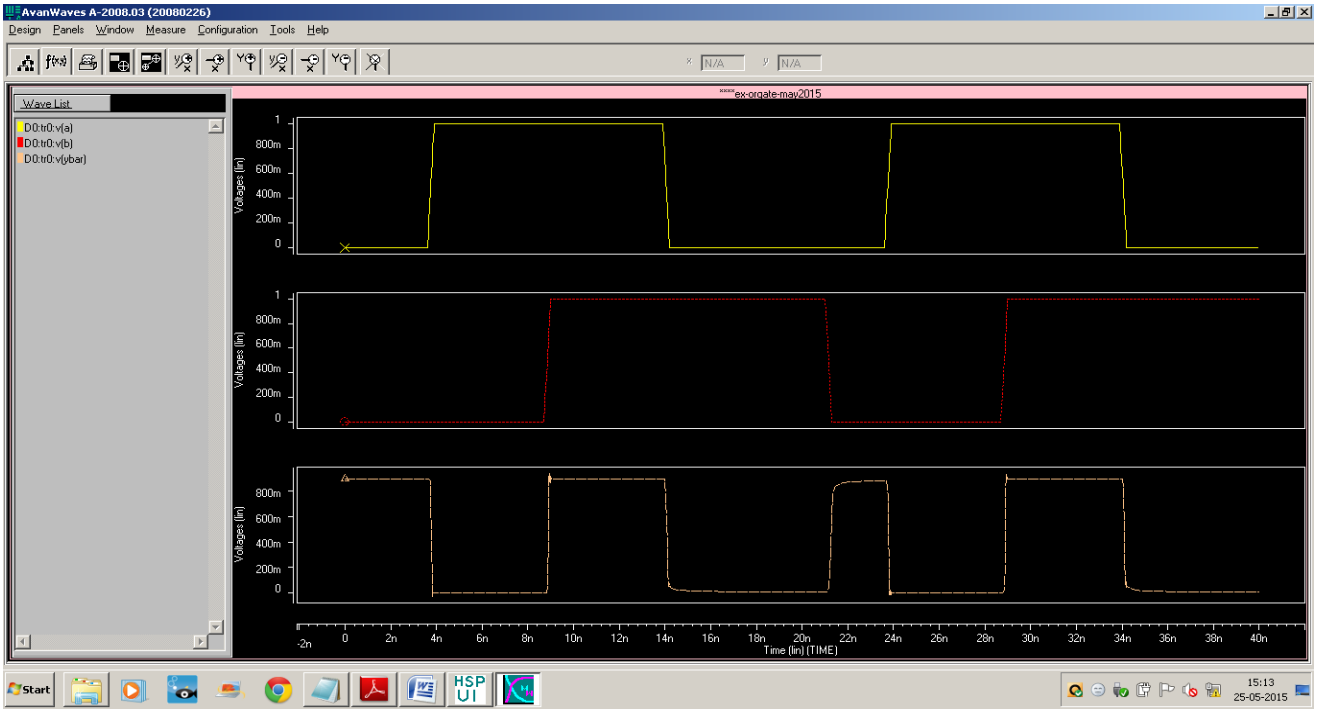

Fig,2. And the waveform of Exnor with forward Body bias is shown below in Fig. 3.

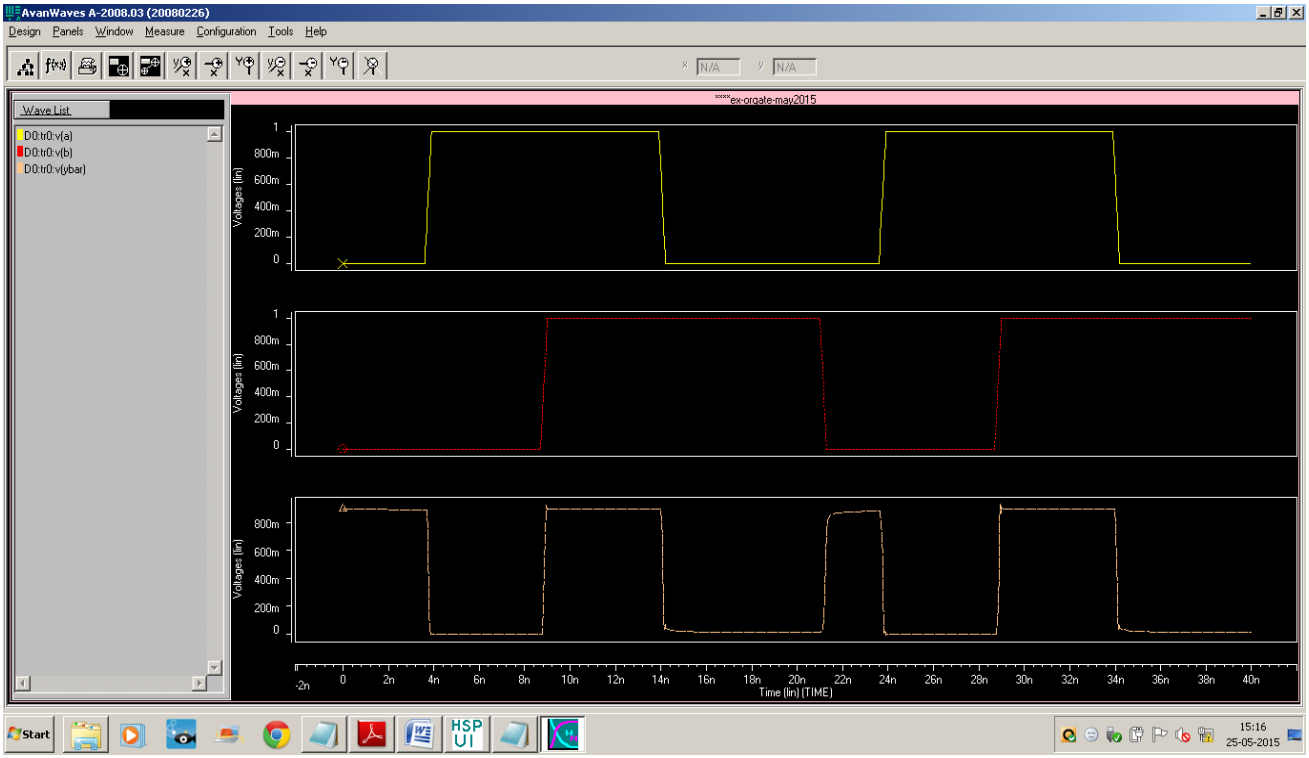

Fig.3

III. CONCLUSION

The reduction in the propagation delay of Exnor circuit with forward body bias is 55.89% compared with propagation delay with reverse body bias.

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