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High Speed EX-OR Gate at 22nm High K Metal Gate Strained SI Technology Node

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Abstract- Four transistor exor gate is chosen and made to work with reverse body bias in all the four transistor. In an another setup, the same exor gate is made to work with forward body bias of 0.45V in all the transistors of the ex_OR gate. The propagation delay is observed to be reduced by 25.146% in the case of all transistors forward body bias. The propagation delay in the normal reverse body bias is 26.096X10-12 sec whereas in the all transistor forward body bias, it is 19.534X10-12 Sec. This high speed Ex-OR gate finds it's application where power penalty is acceptable.

Index Terms— exor gate, ex_OR, Ex-OR, transistor,

I. Introduction

Xor is one of the basic circuit used in half adder, full adder , half subtractor, full subtractor and comparators[1]&[2].With the increase in technology node, power dissipation becomes one of the most important point of considerations as well as the speed taken separately. Earlier speed ,area, reliability were of main concern but now with the requirement of small portable and wireless devices, even power dissipation is main concern. High speed devices consume high power. These all come with increased cooling cost. With increased speed comes the increased power dissipation and with this comes the increased temperature related failures[3]-[5].Theses temperature related failures include various Silicon related failures such as electromigration, decrement in transconductance, thermal runaway, threshold voltage shift, junction diffusion, electrostatic discharge, electrical parameter shift, electrical overstress, Silicon interconnect failures[6]. The research paper [7] on mixed threshold voltage cmos circuits, transistors in a gate have different threshold voltage [8].Two types of MVT are existing in the research literature. The first one in which a single Vth is in either pull-up or pull down trees and the second one in which mixed vth is allowed to be put in both pull up and pull down network. Research paper [7] proposes xor gate with three transistor using mixed threshold voltage topology. The two transistorsM1p and M2n are connected as an inverter circuit with drains of P type and N type are connected together.

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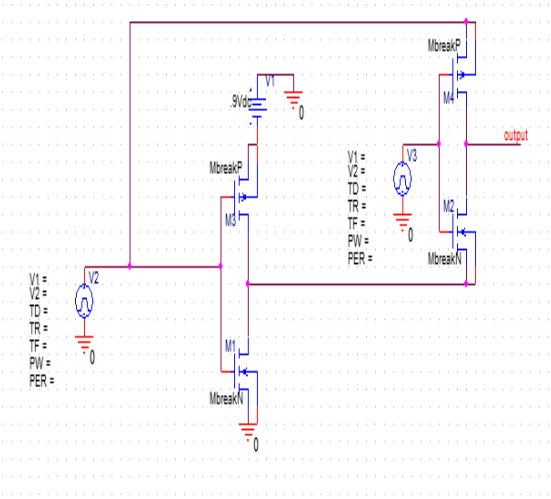
Source of M1p is connected to signal B and gates of M1p and M2n are tied together and connected to signal A. The third transistor M3p (p type) has it's source connected to A signal, it's drain is at the output of M1p and M2n inverter and gate of M3p is connected to B signal. M1p(p type) and M2n(n type)transistors have low vth whereas M3P has high Vth. In general [7],high Vth is to reduce leakage current and low vth is to increase the performance and speed. Following section shows the xor gate as a normal reverse biased substrate and also the Xor gate with forward body bias

II. II Experimental setup and simulation

The following circuit is implemented in which output node is the A ex-orB output. Signal A and signal B are given so as to have all 4 combinations. Output waveforms are noted for this circuit in which reverse body bias is given and also output waveform is noted in which 'half vdd' forward body bias is applied.



Following table is the table of comparison and it shows that propagation delay is reduced in the forward body bias case and hence there is increase in speed of the circuit. Although with forward body bias the average power is increased.

TABLE-1

parameter	With forward body bias of 0.45V	With normal reverse Body bias
Propagation delay(psec)	19.534	26.096

Following waveform is of normal reverse body biased ex_or gate.

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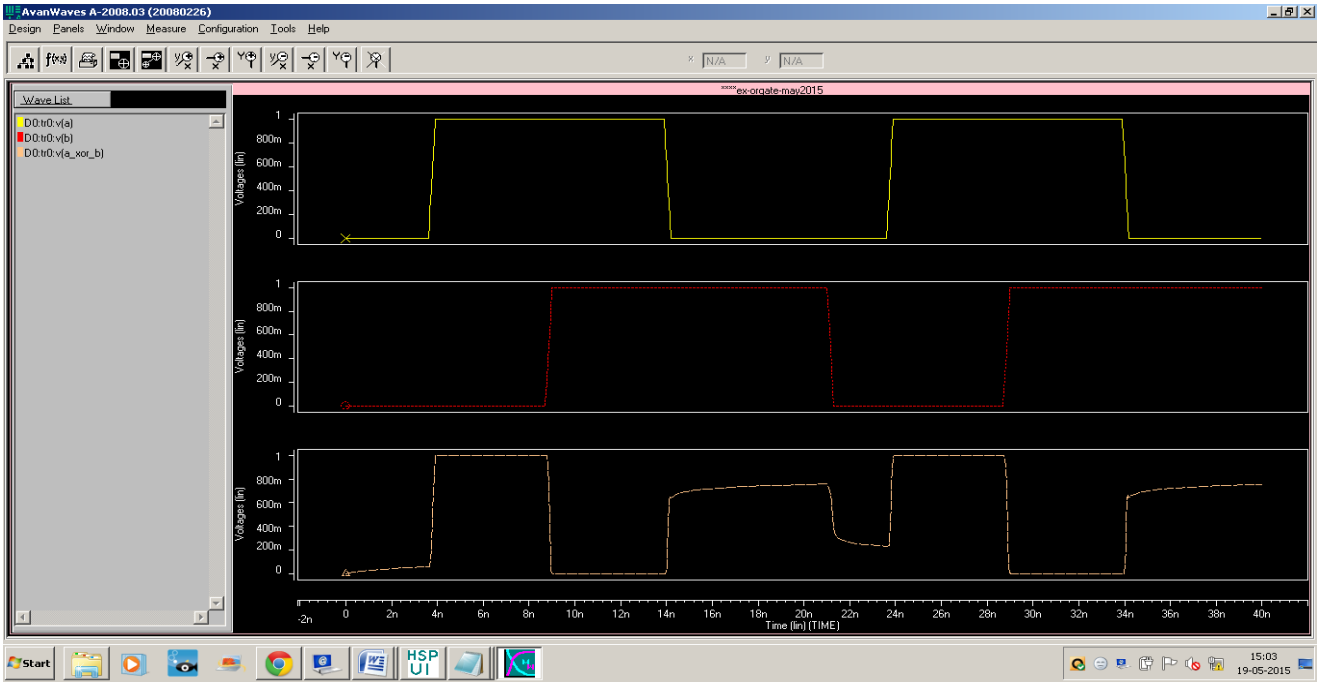

Fig. 1

Fig. 2 is the waveform of EX_OR gate with forward body bias

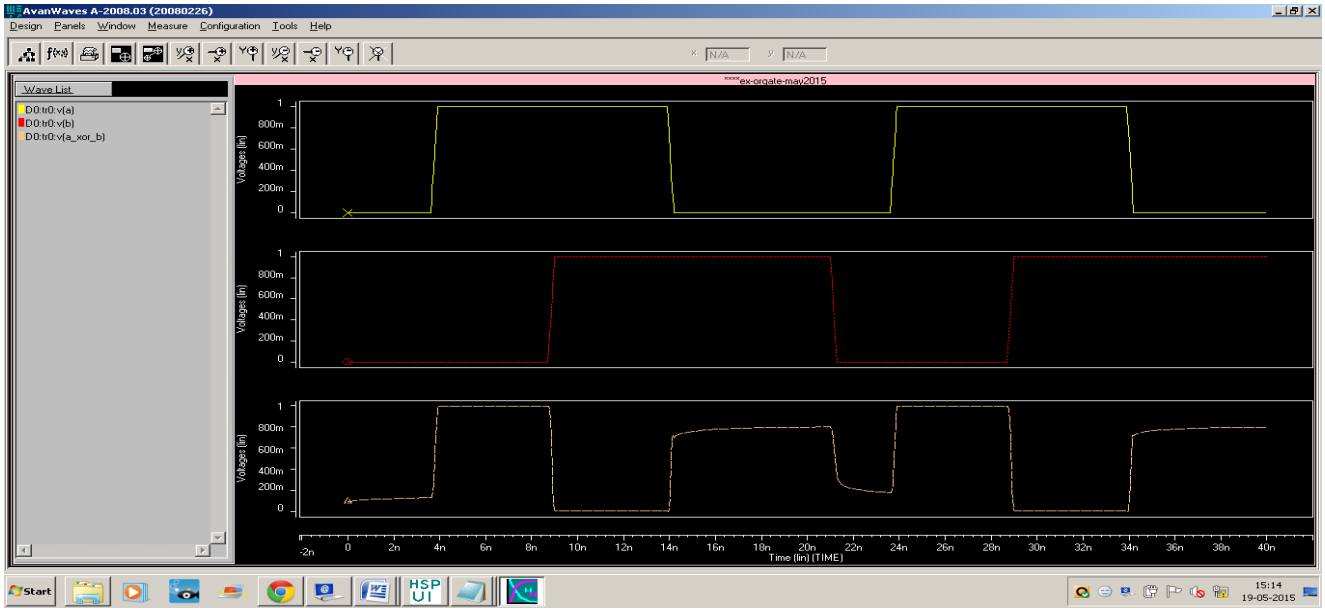

Fig. 2

III. Conclusion

The proposed EX_OR gate with forward substrate biasing of 0.45v is having propagation delay of 19.379PSec and the original EX_OR gate's propagation delay is of 25.88 with normal reverse biased substrate biasing. So the proposed Ex-Or gate is 25.146% times faster

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