# Design and Implementation of Modified Booth Encoder Multiplier using Carry Select Adder

**K. Jeswanth Singh, B. Vamsi Krishna**

***Abstract-Booth encoded Multiplier is used to reduce the hardware utilization in chip level designing in VLSI projects. The present project is focusing on designing and developing a powerful Booth encoded multiplier integrated with Carry Select Adder [CSLA]. Primarily the on hand Booth encoding multiplier is used in multiplication operations based on signed numbers only. The multipliers such as braun array multiplier and array multiplier are used for multiplication operation which is based on unsigned number. There is no specific method to do the multiplication operations based on signed and unsigned numbers. The current project is focusing on design and development of a novel booth multiplier which is enhanced with signed bit operands to produce half the partial products in parallel. Current paper is also concentrating to increase the speed of the multiplier operations by using a method called Carry Select Adder. The use of these integrated technologies is going to reduce the time for multiplication of signed and unsigned numbered operations. The original or modified Booth Encoder Multiplier with Carry Select Adder aims at utilize minimum hardware, reduced chip area, low power dissipation and reduced cost of system.***

***Keywords: Carry Select Adder [CSLA], Modified Booth Multiplier, Xilinx, verilog,***

## I. INTRODUCTION

Multipliers are essential components widely used in multimedia and Digital Signal Processing chips. These are used to give raise to the power and performance of the Chip. Parallel multipliers are predominantly used to increase the speed and reduce the cost of high area complexity. Many multiplication architectures are used to increase the speed and performance of the chips used in multimedia and digital signal processing. In these architectures predominantly modified booth algorithms have implemented significant multiplication in DSP and other multimedia applications. The important and significant Multipliers used in DSP and other multimedia applications are modified booth multipliers with the combination of low error fixed-width, fixed-width, high-accuracy error compensation circuit and low-error reduced-width architectures. All these combinations of architectures with Booth Encoder Multiplier have reduced remarkably the cost of systems and enhanced the speed of the multiplication operations. The better utilization of chip operations in applications such as Digital signal processing and multimedia has improved speed in multiplication chip process, low power utilization and less hardware with increased performance and least chip area.

**Manuscript Received on November 2014.**

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To achieve this target the present paper has focused in designing and developing novel multiplication algorithm with the combination of Booth Encoder Multiplier with Carry Select Adder. The present paper has described the insights of the architecture with simulation results and evaluation reports.

## II. EXISTING SYSTEM

The present Booth Encoder Multiplier is used to perform multiplication operations with the help of two n-bit signed numbers. These can be identified with A and B. A denotes n-bit multiplicand Where as and B stands for n-bit multiplier.

A = $a_{n-1}a_{n-2} \ldots a_0$ ---- [1]

B = $b_{n-1}\, b_{n-2} \ldots b_0$ --- [2]

The above expressions can generate an equation to generate multiplications of chip level operations.

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i, \quad B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i. \qquad (3)$$

The following modified Booth Encoding truth table is shown below.

| $b_{2i+1}$ | $b_{2i}$ | $b_{2i-1}$ | Operation | $neg_i$ | $two_i$ | $one_i$ | $zero_i$ | $cor_i$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | +0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | +A | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | +A | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | +2A | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | −2A | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | −A | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | −A | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | −0 | 1 | 0 | 0 | 1 | 0 |

This existing system is rich with modified Booth Encoding with multiplier's bit and multiplicand bits. The groups of bits have generated five outputs. These are Zeroi, Onei, Twoi, Negi and Cori. Negi.. After all calculations B can be expressed as follows:

$$B = \sum_{i=0}^{n/2-1} M_i 2^{2i} = \sum_{i=0}^{n/2-1} (-2b_{2i+1} + b_{2i} + b_{2i-1})2^{2i} \qquad (4)$$

The existing low power consuming Booth Encoder Multiplier is developed with the encoder and decoder architecture as follows.

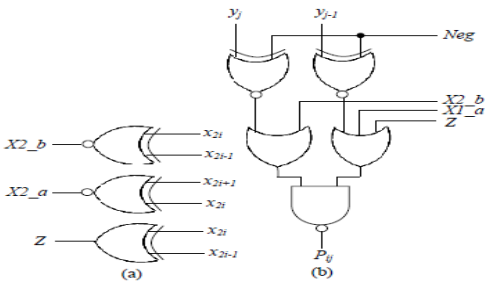


**Fig. 1. Shows the Architecture for Encoding and Decoding**



*Published By:*
*Blue Eyes Intelligence Engineering*
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The modified Booth Encoder partial product array can be revealed from the following figure

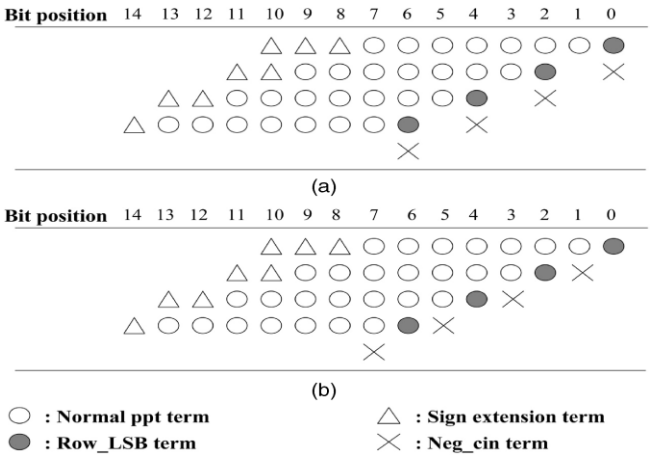



**Fig. 2. Illustrates the Array of Partial Products and Conventional Array of Partial Products**

The latest Booth Encoder Multiplier enriched with t eh 8X8 bit multiplier has given increased performance than other previous systems. The following partial product array illustrates the details.

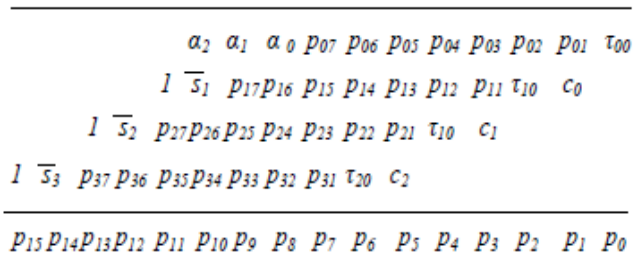
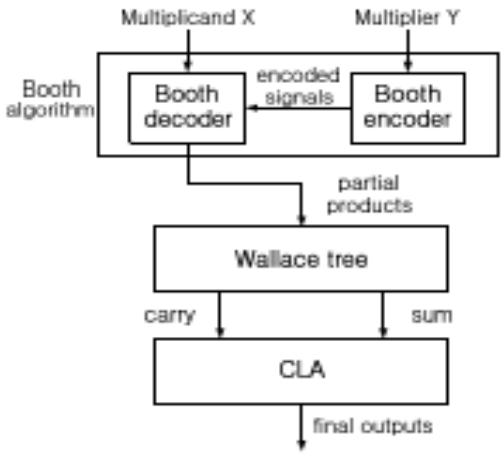



**Fig. 3. Illustrate the Product Array of Latest Existing Booth Encoder Multiplier**

## III. PROPOSED SYSTEM

The proposed Booth Encoder Multiplier using Carry Select Adder is designed and developed with improved architecture and more powerful algorithms. In this architecture X is used as multiplicand and Y is used as Multiplier. The Booth Encoder which is going to be implemented encodes the input Y and extracts the encoded signals. The detailed architecture is shown below.




| $b_{i+1}$ | $b_i$ | $b_{i-1}$ | value | X1_a | X2_a | Z | Neg |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 2 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | -2 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | -1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | -1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

**Fig. 4. Illustrates the Architecture of the Projected Booth Encoder Multiplier**

The main objective of the proposed project is to design and develop a 32X32 multiplier used for signed and unsigned numbers. The modified encoding scheme revealed by the following table.

## IV. MODIFIED BOOTH MULTIPLIER

The projected Modified Booth Multiplier is planned with the following architecture.

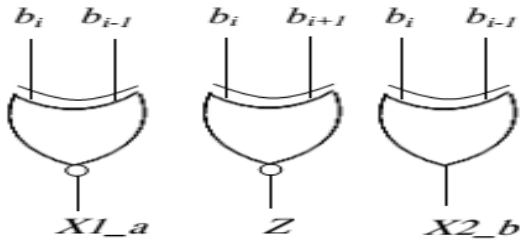



**Fig. 5. Logic Diagram of Proposed MBE Multiplier**

The following equation can gives the solution for SUMBe multiplier to support the encoder and decoder logic.

$$pij = \overline{(ai \oplus bi+1+bi-1 \oplus bi)\,(ai-1 \oplus bi+1+bi \oplus bi+1+ bi-1 \oplus bi)}$$

For boolean equations the logic diagram can be drawn. The following equations are essential for developing the proposed system.

$$Ni = bi+1(\overline{bi-1\ bi}) \quad \text{--- (6)}$$

$$a8 = s\_u \cdot a7 \quad \text{--- (7)}$$

$$b8 = s\_u \cdot b7 \quad \text{--- (8)}$$

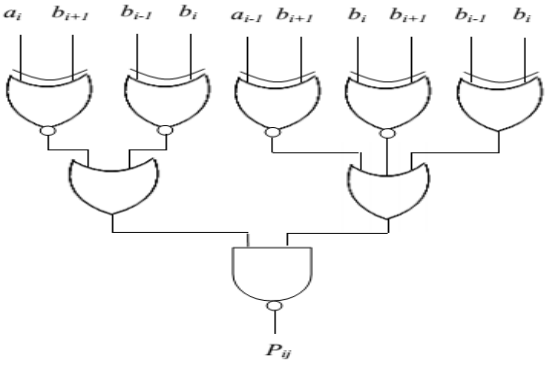



**Fig. 6. Logic Diagram of 1- Bit Partial Product Generator**

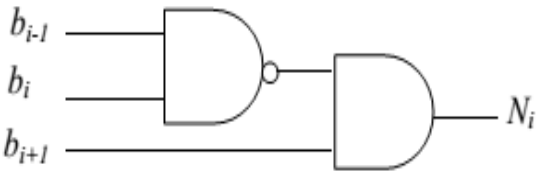



**Fig. 7. Logic Diagram for Negate Bit Generater**

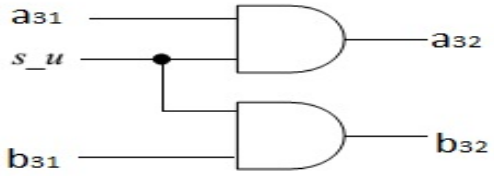



**Fig. 8. Logic Diagram for Sign Converter**

The process involved in the sign extension converts multipliers from signed to the unsigned multiplier.This prrocess is carried out by the multiplication of signed or unsigned numbers.There exists a two condition for both signed and unsigned number

1.) If su=0 (i.e signed,unsigned=0) it represents the unsigned number multiplication.
2.) If su=1 it represents the signed number multiplication.

If the operation invoved signed multiplication the extended bits of the sign relays on mltiplier and multiplicand bits.If multiplicand and multiplier are negative are individually negative or if both operand are negative the multiplier operand is positive .The sign extended bits are b gnereated as su=1, a31=1, b31=0, a32= a33 =1, and b32= b33=0. If multiplicand is positive and multiplier is negative the extended bits should be generated as su = 1, a31=0, b31= 1, a32=a33=0,andb32=b33=1.

| Sign-unsign | Type of operation |
|---|---|
| 0 | Unsigned multiplication |
| 1 | Signed multiplication |

Table represents the signed and unsigned modified booth encoding operations.

a31 a30---------- a8 a7 a6 a5 a4 a3 a2 a1 a0

b31 b30---------- b8 b7 b6 b5 b4 b3 b2 b1 b0

$\overline{p032}$p032p032p031p030--------p07p06 p05 p04 p03 p02 p01 p00 *x1*

1 $\overline{p132}$p131p130p129 -------- p17p16 p15 p14 p13 p12 p11 p10 N0 x2

1 $\overline{P1532}$ P1531P1530 ----------P155P154P153P152P151P150 N14 x16

P1631P1630P1629----------P164P163P162P161P160 N15 x17

P63P62P61P60----------P15P14P13P12P11P10P9P8P7P6P5P4P3P2P1P0

**Fig. 9. Represents the Partial Products Generated by 32X32 Multiplier for Signed – Unsigned Number**

The partial products used in this operation namely X1,X2,X3,X4,X5,X6,X7,X8,X9,X10,X11,X12,X13,X14,X 15,X16 and X17. These partial products can be added by the Carry select Adder (CSLA).

## V. CARRY SELECT ADDER

In the proposed system the predominant feature is Carry Select Adder [CSLA]. CSLA predominantly perform RCA (Cin=1) is replaced by Binary to Excess -1 converter BEC. BEC design is rich with AND, XOR and NOT gates as its structure. The following figure illustrates the architecture and functionality of CSLA.

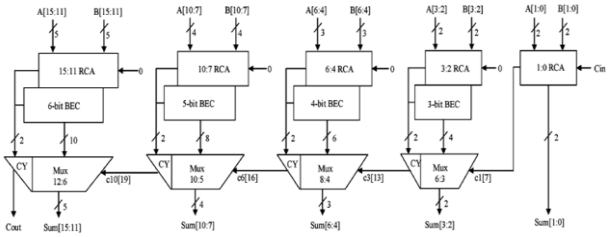



**Fig. 10. Shows Proposed Modified Carry Select Adder**

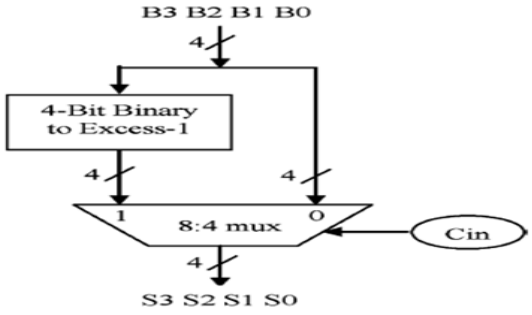



**Fig. 11. Shows 4 Bit BEC with 8:4 MUX**

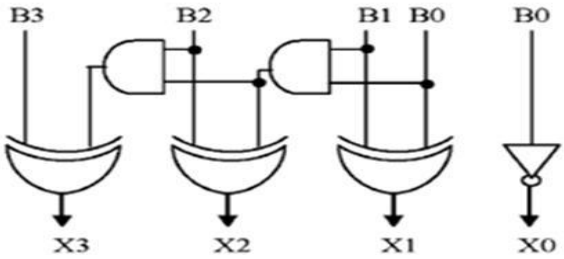



**Fig. 12. Logic Diagram for BEC**

In this structure the XOR gate is replaced by MUX. This is also replaced by NOT gate. The least significant bit of the input is given to NOT gate and it is given as control signal to the MUX for the next input value. The LSB and the next immediate bit is provided as input to the AND gate where its corresponding output value is given as a control signal to the Multiplexer

## VI. RESULTS AND ANALYSIS

The proposed Modified and Improved Booth Encoding Multiplier is designed with the help of Verilog and simulated using Modelsim PE 6,4. The project is synthesized using Xilinx ISE tool.

The results have obtained for Modified Booth Multiplier using CLA and CSLA. The obtained results have been evaluated. The fact is that the results obtained with CSLA have proved to be good with less delay and less hardware utilization.

The following picture illustrates the RTL Schematic Generated by Xilinx ISE tool. This illustrates the comparison of area and delay of Modified Booth Encoding Multiplier using Carry Look ahead adder and Carry Select Adder.

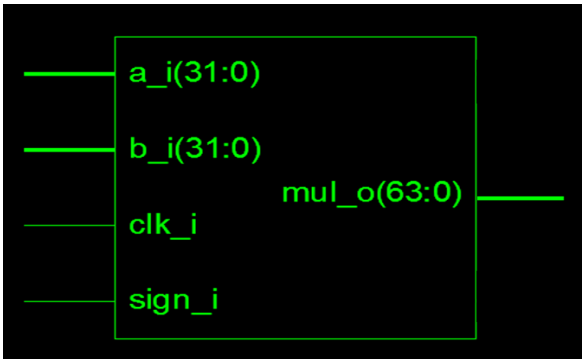



**Fig. 13. RTL Schematic**


**Fig. 14. Simulation Result**

Following tables shows the results

| Logic Utilization | Modified Booth Multiplier Using CLA | Modified Booth Multiplier with CSLA |
|---|---|---|
| **No.of LUT's** | 1272 | 1794 |
| **Delay** | 34.023 ns | 24.529ns |

Table demonstrate the results for Logic Utilizations

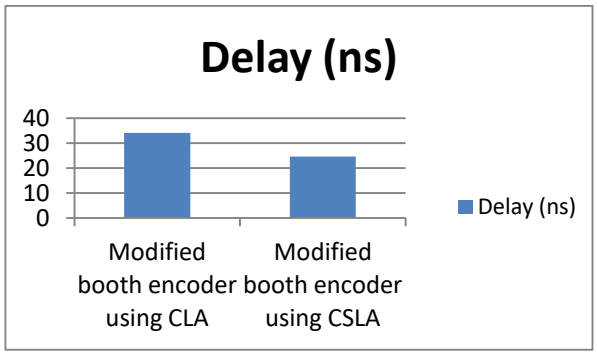



**Fig. 15. Graphical Representation of Results**

## VII. CONCLUSION

The present paper successfully achieved the target in designing and developing a modified Booth Encoder Multiplier with Carry Select Adder to improve the speed of the chip level signed and unsigned multiplication operations. The multiplication operations are tested and recorded the results with previous algorithms and novel Booth Encoder Multiplier with Carry Select Adder method. The results have been evaluated and obtained the results. The results obtained shows that the new method developed increases the pace of multiplication operations of signed as well as unsigned numbers. The observations have exposed that the operations have utilized minimum hardware requirements, low power dissipation and reduced cost for system.

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