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AXI Acquiescent DDR3 SDRAM Memory Controller

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Abstract: ***This paper describes the implementation of AXI acquiescent DDR3 memory controller. It discusses the overall architecture of the DDR3 controller; it also discusses the AXI protocol operation. The DDR3 memory controller compares with DDR1 and DDR2 in performance wise. The design is simulated and synthesized on Xilinx ISE 13.2 successfully.***

Index Terms: AXI Interface, DDR3 memory, AXI protocol operation, AXI access Manager

I. INTRODUCTION

The AXI acquiescent DDR3 Controller allows access of DDR3 memory via AXI Bus interface [1-4]. The DDR3 controller labors as an essential bridge between the AXI host and DDR3 memory. It takes concern of the DDR3 initialization and various timing requirements of the DDR3 memory. The DDR3 controller operates multiple schemes to increases the effective memory throughput [3]. These procedures comprise combining and reordering the Read/Write commands. For accomplishing the maximum throughput from the memory, it functions all the memory banks in parallel and minimizes the result of precharge/refresh and other DDR3 interior actions [2].

II. AXI ACQUIESCENT DDR3 CONTROLLER ARCHITECTURE

The architecture of the design is shown in the fig.1. The design consists of blocks as follows:

- AXI interface
- AXI access Manager
- DDR3 Controller

A. AXI Interface

AXI-Interface block networks with HOST processor and AXI access manager. It is accountable for agreeing and deducing the AXI commands subjected by the processor and responding to Read/Write requests in AXI protocol as requested by processor. It also preserves an arbiter block which is responsible for arbitrating between Read/Write commands. Arbitration is needed between the commands because of parallel/independent Read/Write command obtained at the AXI interface. It upholds asynchronous FIFO's to store the command and the data.

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The Read command gets accumulated in (Read Command Block), Write command gets accumulated in (Write Command block), Read data gets accumulated in (Read Data block), and Write data gets accumulated in (Write Data Block).

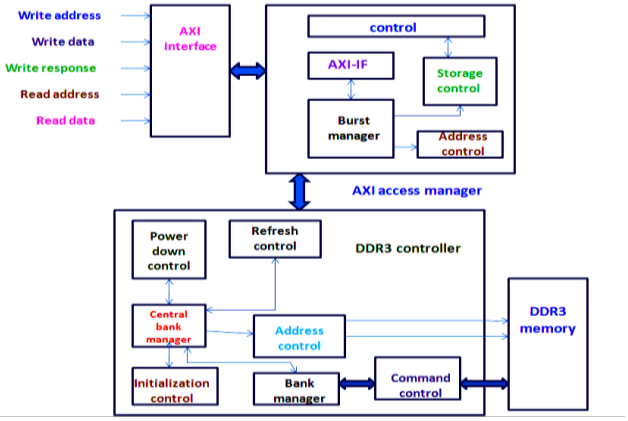

Fig. 1 AXI Acquiescent DDR3 Controller

The accumulated commands are supplied to the AXI access manager whenever AXI access manager is free. Now in view of the fact that the storage can have both Read and Write commands in the respective block hence it keeps an arbiter which arbitrates between Read/Write commands and whenever Burst Manager is free one of the present command is provided to the Burst Manager.

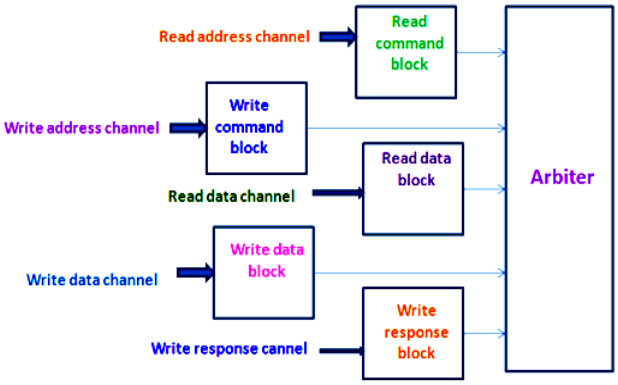

Fig. 2 AXI Interface Block

B. AXI Access Manager

The most important task of the AXI-Access Manager is to translate the AXI commands into memory access commands for utmost use of the DDR3 Band Width. The DDR3 memory receives command only in burst 4 or 8 mode while the AXI command could be a smaller or longer burst. The AXI access manager unites the command wherever possible to improve the performance and transfers the final command to DDR3 controller.

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To assure maximum throughput it pre-fetches the commands from AXI interface translates into memory transactions and preserves locally. These accumulated commands are supplied to the DDR3 Controller whenever DDR3 Controller is not eventful in the very next clock. The AXI-IF block cooperates with the AXI interface block and accepts commands. The accepted commands are accumulated in the storage control block. The Burst Manager translates the AXI command into DDR3 burst. The address control block is accountable for creation of address. The overall action of various blocks in the AXI access manager is directed by the Control Logic. The fig.3 shows the AXI Access Manager Block.

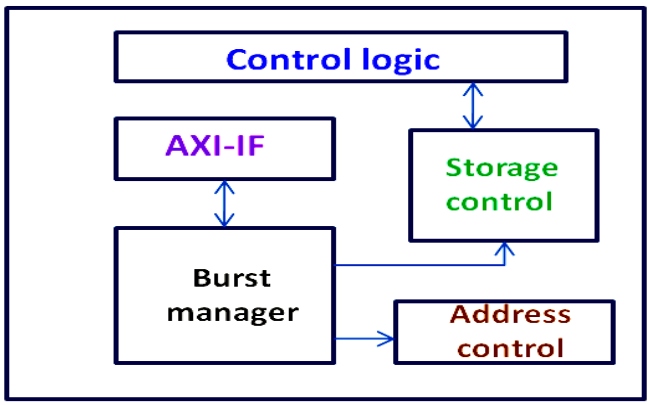

Fig. 3 AXI Access Manager Block

C. DDR3 Controller

The core function of DDR3 controller is to cooperate with the DDR3 memory. This is the heart of the AXI acquiescent DDR3 controller and accountable for realizing the DDR3 protocol and communicating with the DDR3 memory [4]. DDR3 Controller also subjects Refresh, Power down, Self refresh command along with the read or write command as per the user design [1]. The interior blocks of DDR3 controller are shown in the fig.4.

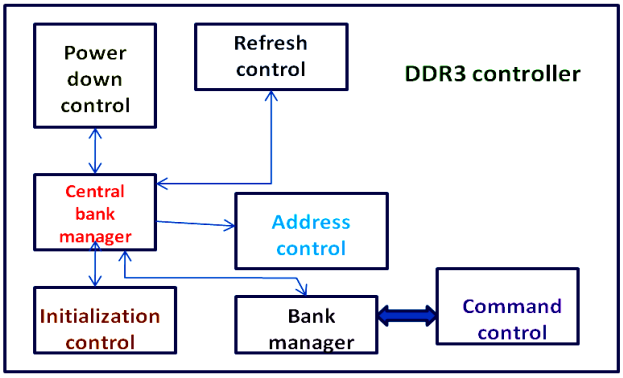

Fig. 4 DDR3 Controller Block

The Power down control block acquires care of generating the power down command to the DDR3 memory at any time the host commands it to go to Power saving mode. The refresh control block performs refreshing the DDR3 memory as per the user supplied design. The initialization control block performs initializing the DDR3 memory after reset. To control the timings of individual DDR3 banks it contains Bank manager which follow the timing requirements for the individual DDR3 banks. The address control block is accountable for creating the address to the DDR3 memory. The Command control block work together with the DDR3 memory and based on the Bank manager inputs constrains the DDR3 bus. It is also accountable for receiving the data during the Read operation. The Central Bank manager synchronizes between the individual Bank Mangers and upholds the overall timing requirement of DDR3 memory.

III. DDR3 CONTROLLER FSMS

DDR3 memory controller converts bus master commands in to memory commands. There are 3 FSMs involved in this controller such as

- Data path FSM
- Refresh FSM
- Command FSM

A. Data path FSM

This carry outs the read and write operations between bus master and DDR3 SDRAM memory. The fig.6 shows the data path FSM. After reset when w=1/r=0 & wreq=1 then the data is written in to DDR3 and comes to idle state or again read or write operation takes place. If r=1/w=0 & rdreq=1 then the data is received from data bus in to controller and look for another read or write operation or comes in to idle state.

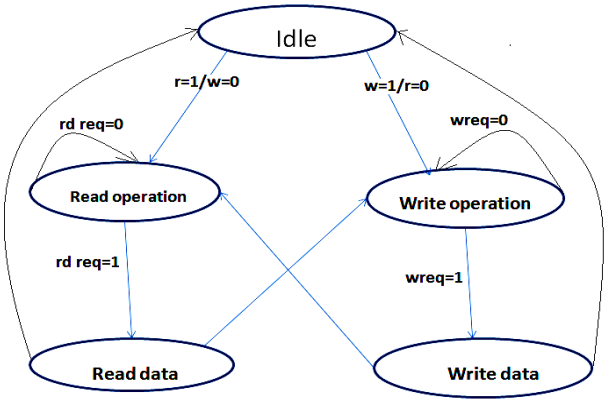

Fig. 6 Data Path FSM

B. Refresh FSM

It initializes memory, resets the command signals. Refreshing memory in two ways i.e. using counter (to refresh continuous sequence) or LFSR (to refresh randomize sequence). The fig.7 shows the Refresh FSM. After reset when sel=1 then refreshing memory through counter or sel=0, is through LFSR.

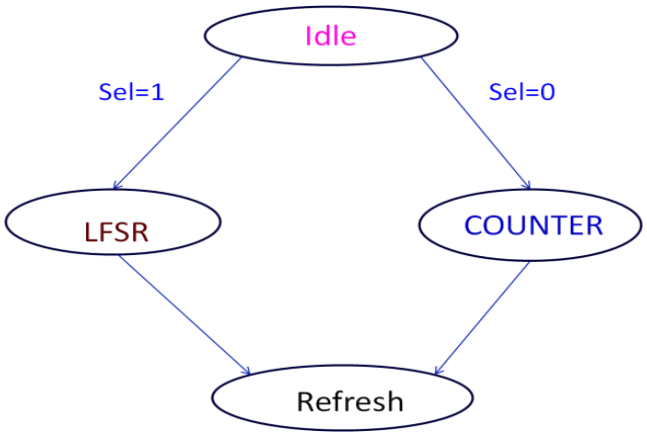

Fig. 7 Refresh FSM

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C. Command FSM

This control commands to memory, receives commands of master and passes commands to memory. The fig.8 shows the data path FSM. After reset if w=1 and wreq=1 then write command is issued to memory. Otherwise, if r=1 & rdreq=1 then the read command is issued.

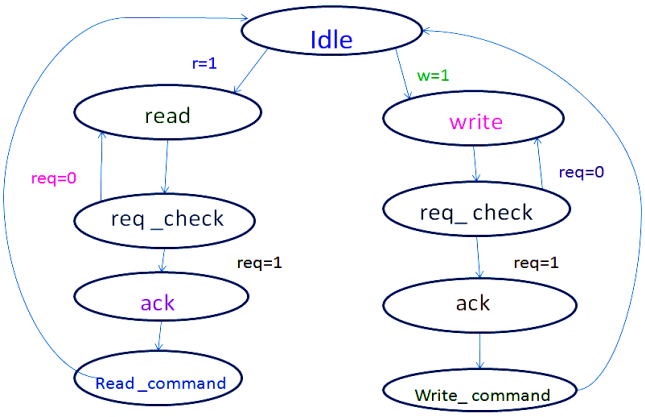

Fig. 8 Command FSM

IV. COMPARISON OF DDR1, DDR2 & DDR3 CONTROLLERS

DDR3 suggests a significant performance development over previous DDR1 & DDR2 memory systems. New DDR3 features, all clearly realized in the memory controller, improve the signal integrity characteristics of DDR3 configurations so that higher performance is attained without an excessive load for the system designer. If proper deliberation is given to any new DDR2 memory design, it can be a comparatively easy improve to hold up DDR3 in the next generation design.

TABLE I

DEVICE UTILIZATION SUMMARY OF DDR1 CONTROLLER

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	8,764	21,504	40%
Number of 4 input LUTs	5,703	21,504	26%
Number of occupied Slices	6,879	10,752	63%
Number of Slices containing only related logic	6,879	6,879	100%
Number of Slices containing unrelated logic	0	6,879	0%
Total Number of 4 input LUTs	5,718	21,504	26%
Number used as logic	5,703		
Number used as a route-thru	15		
Number of bonded IOBs	87	240	36%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	3.27		

TABLE II

DEVICE UTILIZATION SUMMARY OF DDR3 CONTROLLER

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Total Number Slice Registers	8,350	21,504	38%
Number used as Flip Flops	126		
Number used as Latches	8,224		
Number of 4 input LUTs	12,881	21,504	59%
Number of occupied Slices	6,607	10,752	61%
Number of Slices containing only related logic	6,607	6,607	100%
Number of Slices containing unrelated logic	0	6,607	0%
Total Number of 4 input LUTs	12,896	21,504	59%
Number used as logic	12,881		
Number used as a route-thru	15		
Number of bonded IOBs	88	240	36%
Number of BUFG/BUFGCTRLs	3	32	9%
Number used as BUFGs	3		
Average Fanout of Non-Clock Nets	4.32		

V. SIMULATION RESULTS

The underneath figures are showing snapshots of AXI bus master, DDR1, DDR2 and DDR3 Controller functions. The design has been coded in "Verilog HDL" language. Our design has been implemented with respect to low area and high performance parameter and the design is simulated and synthesized on Xilinx Virtex-4, 4vlx25sf363-12 series successfully about 60% area utilization has been achieved.

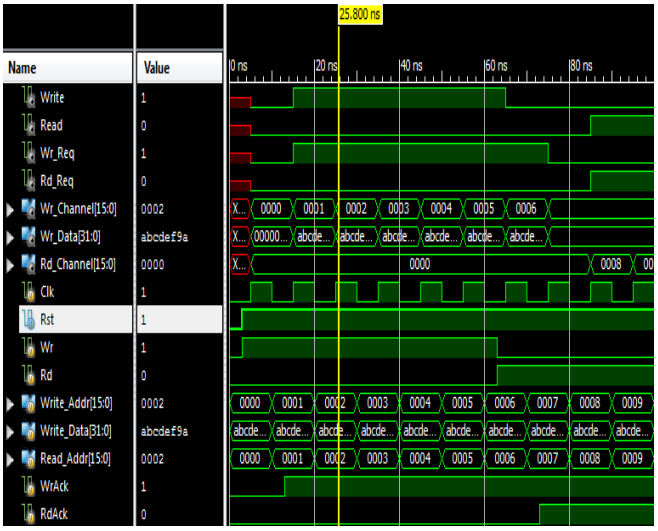

Fig. 9 Simulation of AXI Bus Master

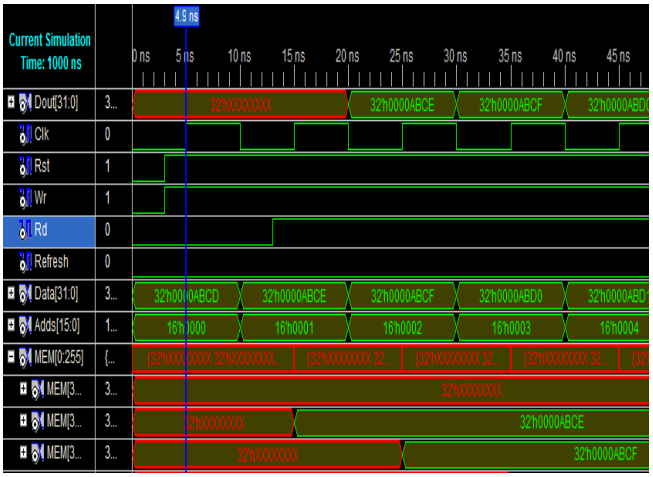

Fig. 10 Simulation of DDR/DDR1 Memory

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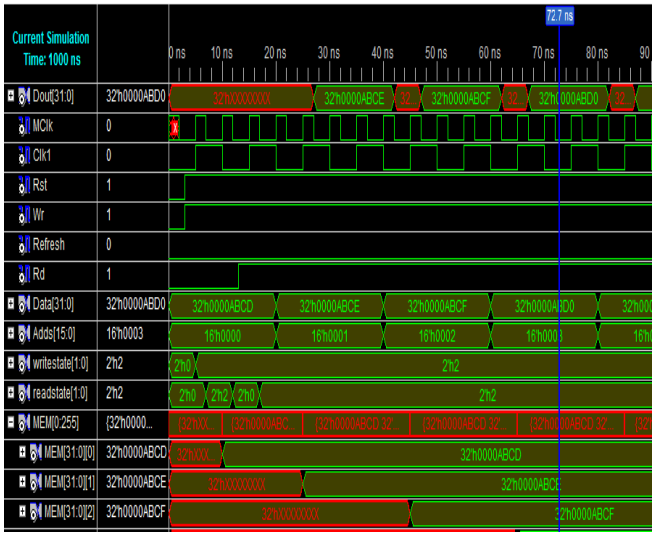

Fig. 11 Simulation of DDR2 Memory

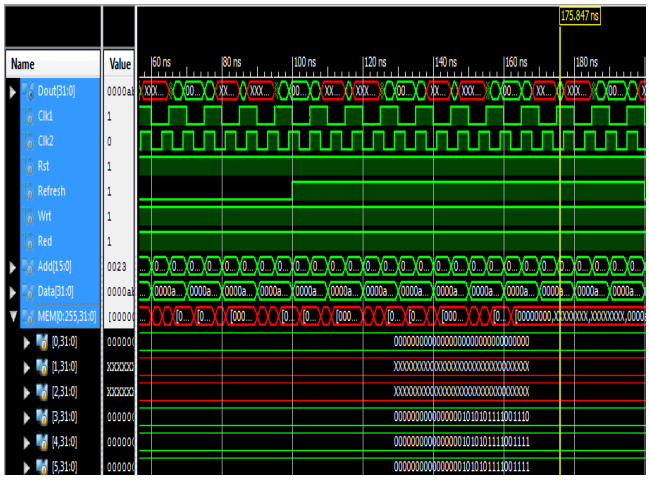

Fig. 12 Simulation of DDR3 Memory

VI. CONCLUSION

In this paper we have designed a High speed DDR3 SDRAM Controller with 32-bit data transfer which coordinates the transfer of data between DDR3 SDRAM and AXI bus master. The benefits of this controller contrast to DDR1 SDRAM and DDR2 SDRAM is that it coordinates the data transfer, and the data transfer is twice as fast as previous, the production cost is also very low. We have successfully designed using Verilog HDL simulated and synthesized using Xilinx ISE 13.2 tool.

VII. FUTURE SCOPE

Future enhancements in AXI interface block is to affix more aspects like fixed address mode, address wrapping mode and write response signal creation other than OKEY response. In fixed burst, the address stays all the same for every transfer in the burst. This burst type is for every repeated admittances to the same location such as when filling or emptying a marginal FIFO and wrapping burst is similar to an rising burst, in that the address for each transfer in the burst is an growth of the previous transfer address.

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