A CMOS Class-E Cascode Power Amplifier for GSM Application

Manoj Sharadrao Awakhare

Abstract*— The design of A 2.4-GHz CMOS Class E cascode power amplifier (PA) for GSM applications in TSMC 0.18-µm CMOS technology present in this paper. Proposed Class E cascode PA topology is a single-stage topology in order to minimize the device stress problem. A parallel capacitor is connected across the transistors for efficiency enrichment also for dominating the effect of parasitic capacitances at the drain node. The simulation results point to that the PA delivers 12 dBm output power with 43.6% and 46.6% of power added efficiency (PAE) and drain efficiency (DE) respectively with 2.5-Volt power supply into a 50-Ω load.

Index Terms* —Class E, CMOS power amplifier, power added efficiency, switching amplifier.

I. INTRODUCTION

Nowadays wireless communications stress a wireless standard that is capable of supporting a variety of services including voice, video and other multimedia, which in turn calls for low cost handheld electronics of high integration, high power efficiency yet with great performance. In wireless communications infrastructures employ increasingly complex functionalities to optimize the use of bandwidth, minimize the cost, and enhance the portability of wireless personal communication systems. A majority of modern telecommunication protocols require the transmitter power to be in tune over a wide range. This feature, commonly called as power control, ensures that base station received ample power, while saving power by reducing the transmitted power when the maximum transmitted power is not required [14]. PA is the most critical component in RF transmitter. Thus, highly efficient PAs are necessary to improve overall efficiency because it consumes the largest portion of dc power in the transmitter. A class-E PA is adaptable for a high-efficiency transmitter due to its high efficiency and simplicity. As a kind of switching amplifier, it can achieve the ideal 100% drain (or collector) efficiency by shaping the voltage waveform and current waveform so that they do not overlap, making it a highly efficient RF PA.

II. PRIMARY THEORY OF CLASS E PA

A typical equivalent circuit of an ideal single-ended Class-E power amplifier depicted in Fig.1 contains an ideal voltage-controlled switch, a shunt capacitor at the output, a RF choke and a series-tuned R-L-C circuit as the load. The RF choke allows constant DC current to flow through when the switch is on, while blocks ac signals as an open circuit when the switch is off. The shunt capacitor is charged and discharge during ON-OFF cycle. The series-tuned tank allows the fundamental sinusoid appears at the output.

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If no charge is stored in the capacitor and no current flows through it at the turn on instant, the optimum Class-E is obtained. Class-E shapes the drain voltage and current waveforms by the load network to avoid simultaneous high voltage and high current in the transistor. The optimum working conditions require the switch voltage and the charges in the shunt capacitor are reduced to zero at the instant of turn-on. By doing so, the power consume an ideal Class E power amplifier has 100% drain efficiency, but this number will be reduced by many practical factors including finite circuit Q, breakdown voltage limitation, non ideal parasitic in transistor, and non ideal RF choker .These conditions ensure that no large energy is dissipated even during the switching transition. For this reason, optimum Class-E amplifiers are also called zero current or zero-voltage switching amplifiers.

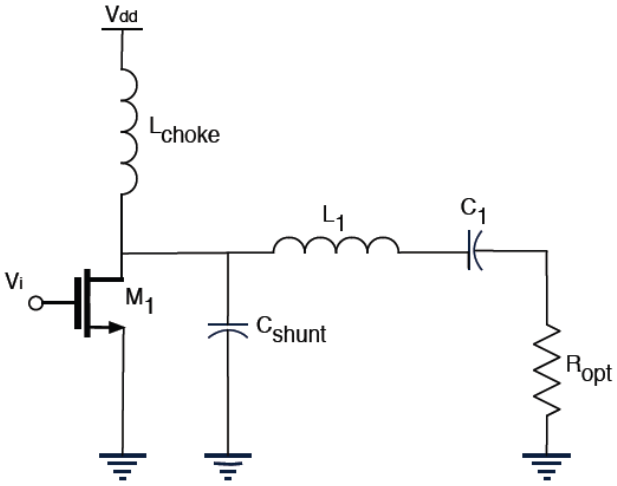

Fig.1. Schematic of Single-Ended Class -E Power Amplifier

III. WHY CASCODE TOPOLOGY?

There are some issues related to power amplifier using single transistor are limitations of Breakdown Voltage with a single transistor, the swing from input voltage will cause tremendous stress on the gate oxide. The cascode structure allows the top transistor to have its gate oxide stress reduced by providing it a constant gate biasing. With biasing voltage at cascode transistor is a constant then breakdown voltage is given by

$$Breakdown\ voltage(B.V) = 2.56 * Supply\ volta \quad [32]$$

Additionally, this method reduces the drain-source voltage at both transistors. It also provides large output impedance than single stage amplifier which is helpful to increased gain at output stage. The drain and gate voltages are out of phase and due to class-E operation, the peak drain voltage when the device is off can be as large as 3.56 times the DC supply value [11], [12].

Assuming the power device in Fig. 2 is biased at threshold voltage for a 50% duty cycle, and supply voltages for the PA, the maximum gate-drain voltage is as large as 4.56V. Although the maximum voltage for safe device and circuit operation has not been recognized yet when switching is at RF, common practice is keeping the maximum voltagedrops across devices below to assure reasonable device/circuit life-times [4], being the nominal supply voltage. In this way, oxide fields never exceed the critical oxide field, thus avoiding unrecoverable oxide breakdown to occur in DC conditions assuring safe operation also at RF.

Optimizing the cascode topology, from the reliability standpoint, requires setting the bias voltage of the common-gate transistor to minimize the voltage drops across the oxide of common gate transistor and common source transistor. However, we expect the common gate device to contribute to power dissipation. Two distinct mechanisms can be identified. When the transistor is on, the resistive channel dissipates. This consumption component is proportional to the triode resistance, and can be minimized by maximizing device width, i.e., making the drain to substrate capacitance equal to the shunt capacitance. Since the device works in the triode region, a resistance formed by the conduct channel therefore can be determined as

$$\text{Ron} = (\text{Vds}/\text{Ids}) = \frac{L}{\mu n \text{Cox} W (\text{Vgs} - \text{Vth} - (\frac{\text{Vds}}{2}))} \qquad [32]$$

Where Vds is voltage across drain to source of transistor, Ids is current flowing through same and Vgs is gate to source voltage. The second mechanism, taking place when switch is turned off, is associated to charging and discharging transients of the parasitic capacitance, which is comprised of drain-bulk and drain-gate capacitances and source-bulk and gate-source capacitances, during transients the active devices dissipate power. The resulting power loss is not negligible at all and can vanish the advantages of an increased supply voltage. With the device width known, we can evaluate the impacts of the parasitic capacitances Cg and Cd. Since the effect of the gate-to-drain capacitance is eliminated by the cascode topology, the gate capacitance Cg in the resistive mode is Cg = Cox*W*L.

For the cascode topology, the common gate transistor works within the saturation region. The drain capacitance Cd is then composed of the gate-to-drain overlap capacitance, the junction capacitance and the sidewall capacitance

$$\text{Cd} = \text{Cgdo} + \text{Cdb}$$

$$= \text{WCgd0} + \text{WLd}*\frac{Cj}{(1+)\left(\frac{Vd}{Vbi}\right)^{MJ}} + (\text{W} + 2\text{Ld})*\frac{Cjsw}{(1+)\left(\frac{Vd}{Vbsw}\right)^{MJsw}}$$

IV. CIRCUIT DESIGN

In class E design method, the switch is replaced by TSMC's real NMOS transistor M1 and the cascode device M2 is added in this topology. The bottom transistor (M1) is connected as a common-source transistor. The cascode transistor (M2) operates as a common-gate transistor. The size of M2 is chosen so that the shunt capacitor Cp is fully absorbed by the output capacitance of the NMOS transistor. The most important feature of the cascode class-E PA is the ability to control the output power by changing the cascode voltage Vg. The M1 transistor is operated as a switch. That means it is either OFF or in the deep triode region. The M2 transistor operates either in saturation or in the triode region. The mode of the operation of the M2 transistor depends on the Vg voltage. For a given standard 0.18um CMOS process, foundry provided by TSMC. Detailed shown in figure2 below

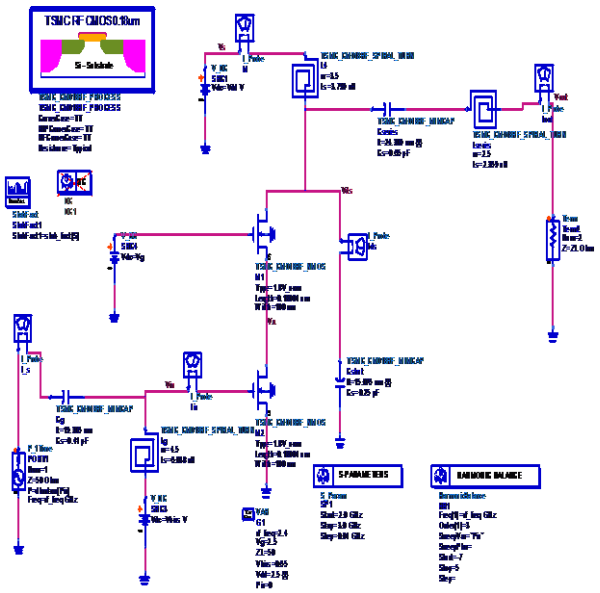

Fig.2. Practical Schematic of Cascode Class E Power Amplifier

Table.1 Parameters /Components Specification

Sr.no	Parameters/component	Value
01	Aspect ratio of M1 and M2	100um/0.18um
02	Cg and Lg	0.41pF and 6.038nH respectively
03	Ls , Vdd and Vdc	3.799nH and 2.5V,2.5V respectively
04	Cshunt, Cs and Ls	0.25pF, 0.65pF and 2.369nH respectively
05	Load and source impedance	50 Ω

Here as per gate oxide breakdown consideration, supply voltage is taken as 2.5V. The biasing of Cascode transistor means common gate transistor can be taken as equal as supply voltage. In this design procedure it (Vg) taken as 2.5V.The common source transistor biasing is done such that it work in saturation mode and in deep triode region. Termination on input side and output side is standard 50Ω. Impedance matching network is used to match load resistance here it is 6.27 Ω to termination of 50 Ω. It is up matching series tuned Ls-Cs are used. Here spiral inductor and MIM capacitor is used for designing. These have less parasitic losses and easy fabrication. Similarly input impedance 27.7 Ω matched with source termination.

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Lg-Cg high pass filter matching network is used on input side.

V. PERFORMANCE PARAMETERS OF CLASS-E PA

There are several kinds of efficiencies in use: drain/collector efficiency and power added efficiency are the most commonly used.

A) *Drain Efficiency*: It is ratio of output power (Pout) to dc input power (Pdc) i.e. how much dc power is converted to AC power at output.

$$\eta drain = Pout / Pdc$$

This efficiency definition does not provide information about the input. An amplifier of low power gain could exhibit high efficiency.

B) *Power Added Efficiency (PAE)*: takes the input driving power into account and thus can better evaluate the performance of some high-efficiency power amplifiers. The power added efficiency is defined as:

$$PAE = (Pout – Pin)/ Pdc$$

C) *Stability Factor*: This is the factor which defines the ability of amplifier to work in different conditions and produce a quality output. This actually refers to the biasing of the devices and the operation on the structure.

VI. EXPERIAMENTAL RESULT

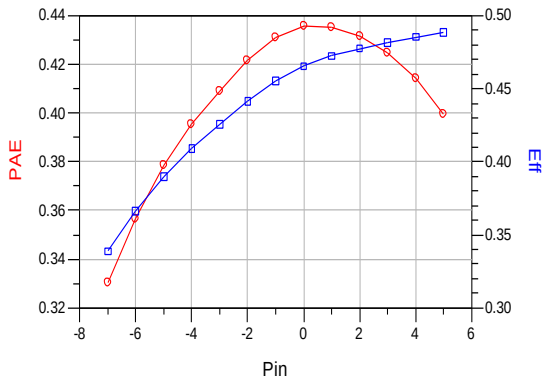

Fig.3. Output Power Added Efficiency (PAE) and Drain Efficiency (Eff.) Versus Input Power (Pin)

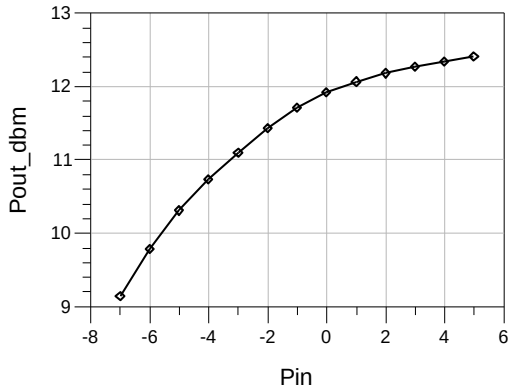

Fig4.Output Power Pout in dbm Versus Input Power (Pin)

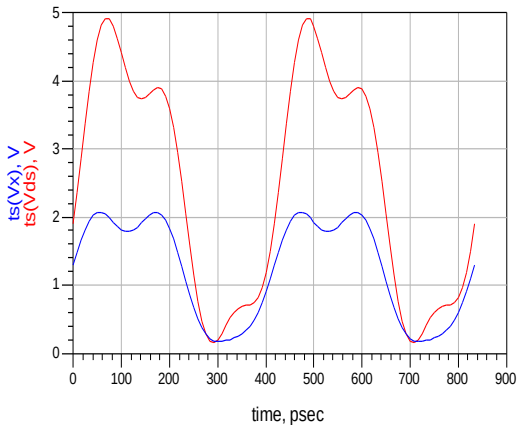

Fig.5. Drain Voltage Waveforms of the Common Gate and the Common Source Transistors

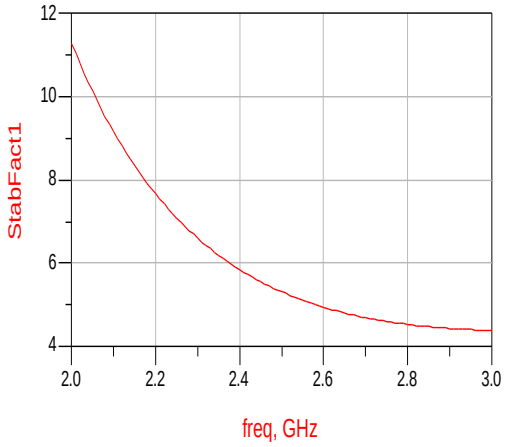

Fig.6. Stability Factor of Power Amplifier

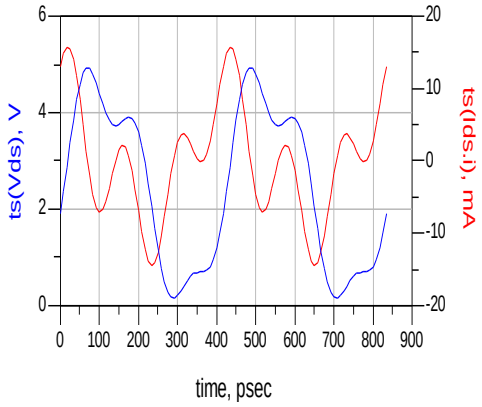

Fig.7. Voltage (Vds) and Current (Ids) waveform

Table2. Comparison between this Work and Previous Literature

Reference	Centre Frequency(GHz)	Technology[um]	Supply voltage [V]	Pout(dBm)	PAE[%]
[24]	0.9	1.5	5	23	49
[25]	2.4	0.35	1.5	23	37
[26]	1.9	0.6	3	23	42
[4]	1.4	0.25	1.5	24.87	49
[27]	0.835	0.8	2.4	26.5	67
This work	**2.4**	**0.18**	**2.5**	**12**	**43.5**

From the simulated result it is observed that there are 43.6% Power Added Efficiency (PAE) and 46.6% drain efficiency (Eff.) with 12dbm output power (Pout_dbm) is obtained. There is also try to maintain non overlapping of drain current and voltage across Cshunt. Stability factor shows the stability of power amplifier which has minimum value is 1. As per result it is greater than 1 at centre frequency of 2.4 GHz.

VII. CONCLUSION

In this paper, we presented cascode class E power amplifier which reduced voltage stress on transistors. From result it clears that stress on switch is released because of cascode transistor and swing is also increased up to 5V. We also used negative parallel capacitance across the switch and cascode transistors to compensate for surplus capacitance on the drain of class E amplifier in order to achieve high efficiency with cascode topology. Non overlapping of drain current and voltage across shunt capacitor also achieved which is basic criteria for switch mode class E power amplifier.The prototype realized in 0.18um CMOS technology, with TSMC foundry file has demonstrated 43.6% of PAE when delivering 12 dBm output power at 2.4 GHz having best stability of power amplifier.

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