International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-3, Issue-1, March 2014

Data Aware Dynamic Low Power Reconfigurable FIR Filter Design

M. Bharath Reddy, M. Sai Sarath Kumar, B. Suresh Kumar

Abstract: ***This paper aims for developing a new architecture for finite impulse response (FIR) filter, which will reduce dynamic power consumption based on the concept of dynamic filter order change. The dynamic changing of the filter order is based on the fact that FIR filter has large amplitude variations in both the input sequence and impulse response (filter coefficients). Trade off between filter performance and dynamic power consumption presented in this paper suggests that a significant reduction in the dynamic power can be achieved without much compromise in the filter performance. The required area overhead is also much less when compared to the conventional approach. The power savings of up to 25 to 35% can be achieved with the modified FIR filter architecture presented in this paper.***

Index Terms: FIR filter, IIR filter, Convolution, Reconfigurability.

I. INTRODUCTION

A filter is a frequency selective network. There are two types of filter: analog and digital filters. Analog filters are more susceptible to noise and are not easily programmable as compared to digital filters. A digital filter is a discrete time system, designed to reshape the spectrum of the input signal to produce the desired spectral characteristics in the output. The growth in mobile computing and portable digital system applications has increased the demand for low power digital signal processing (DSP) systems.

The most widely performed operations in DSP systems is finite impulse response filtering. There are two types of digital filters: FIR and IIR. FIR filters have finite duration impulse response and IIR filters have infinite duration impulse response (in practical a long duration impulse response is used). The selection of a particular type of filter depends on the nature of a problem and on the specifi- cations of the desired frequency response. For example if one wishes to take advantage of the computational speed of FFT then one need to choose the finite duration impulse response. IIR filters have an excellent amplitude response at the expense of non linear phase whereas FIR filters have exactly linear phase which is the necessary condition for distortion less transmission. Thus the design techniques of low power FIR filters are of significance. An FIR filter is described by the following linear constant coefficient difference equation:

$$Y(n) = b_0 x(n) + b_1 x_1 (n-1) + \ldots + b_{M-1} x(n-M+1) \quad -(1)$$

Where b_k = set of filter coefficient. The lower and upper limits describe causality and finiteness properties of a FIR filters. In this paper we modified, the existing filter architecture by adding reconfigurability and applied pipelining technique for increasing the power efficiency and speed. Reconfigurability here means the filter order can be dynamically changed based on the input data and filter coefficient amplitudes. If the data sample multiplied to the filter coefficient is too small to alter the partial sum in FIR filter, the multiplication operation is cancelled. Pipeline latches are used to improve speed and throughput. The primary goal of this work is to reduce dynamic power and improve the speed at the cost of minimal performance degradation

D: Delay element

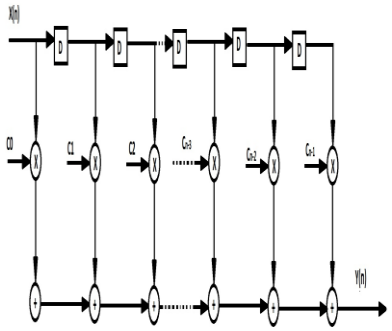

Figure 1. Architecture of the direct form FIR filter

II. PRINCIPLE OF MODIFIED FIR FILTER ARCHITECTURE

In general any filtering operation is done by convolving the input sequence with the impulse response of that particular filter. The selection of impulse response or filter coefficients determine the nature of the frequency response and type of the filter, such as low pass, high pass, band pass and band reject. The degree to which h(n) approximates the given specifications depends on the selection of the filter coefficients b_k, as well as on the number of coefficients (or order N). Since the amount of hardware required (i.e. registers, multipliers and adders) and computation time are directly proportional to the filter order we can dynamically change the filter order by turning off some of the multipliers and hence considerable power savings can be achieved at the cost of nominal degradation in the filter performance. However by carefully changing the filter order, filter performance degradagation can be reduced. Generally in the impulse response of any filter the center coefficient has the longest amplitude, while the amplitude of the rest of the coefficients decreases monotonically as we move far away from the center coefficient.

Revised Manuscript Received on 30 March 2014.
* Correspondence Author
M.Bharath Reddy*, M.Tech. Department of VLSI Design, VIT University, Vellore Institute of Technology, VIT University, Vellore (Tamil Nadu) India.
M.Sai Sarath Kumar, M.Tech. Department of VLSI Design, VIT University, Vellore Institute of Technology, VIT University, Vellore (Tamil Nadu) India.**B.Suresh Kumar,** M.Tech. Department of VLSI Design, VIT University, Vellore Institute of Technology, VIT University, Vellore (Tamil Nadu) India.

The input sequence x(n) of the filter also has large amplitude variations. Therefore the basic idea is that if the amplitude of both input and filter coefficients are small, thus turning off the multiplier has negligible impact on the filter performance. If we carefully select input threshold x_{th} and coefficient threshold c_{th} in such a way that the multiplication of these two numbers is small when compared to the quantization error, then the performance degradation can be minimized.

III. ARCHITECTURE OF MODIFIED FIR FILTER

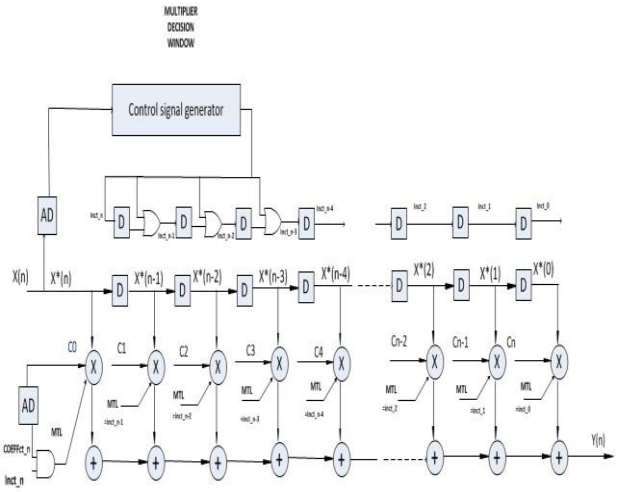

Figure 2.Reconfigurable FIR Filter

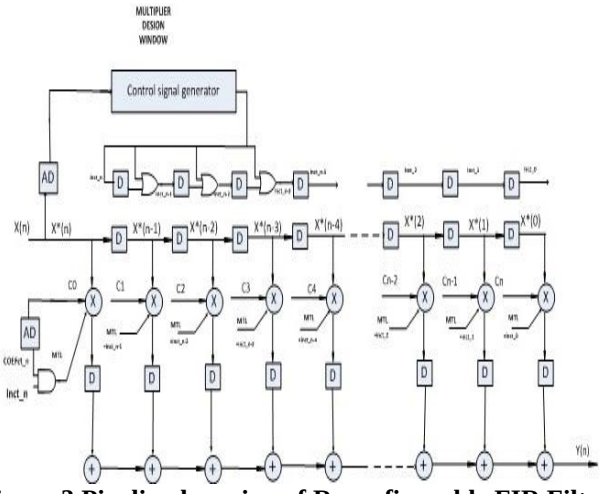

Figure 3.Pipelined version of Reconfigurable FIR Filter.

A. Amplitude Detection Logic (AD):

As shown fig4.The amplitude detection logic can be used to determine whether the absolute value of the input sample is less than data or input threshold (x_{th}) or not. The amplitude detection logic can be done by using a comparator. One input to the comparator is input-threshold and the other input is input sequence. The output of AD block or comparator is set to logic '1' when the value of x (n) is small than x_{th}.

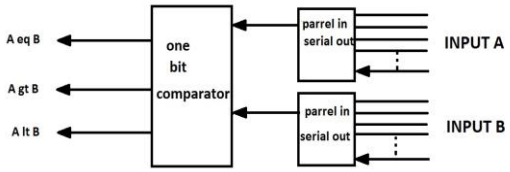

Figure 4. Amplitude Detection Logic

B. Multiplier decision Window (MDW):

Control Signal Generator: The dynamic power dissipation is given by

$$P_{dynamic} = C_{total} * V^2 * f * \alpha \text{—(2)}$$

Where C_{total} = summation of all node capacitances. Since dynamic power dissipation is a strong function of switching factor 'α'. If we turn off multiplier by considering input signal values alone, then if the value of x(n) abruptly varies above and below threshold value in every cycle, switching factor 'α' increases which results in dynamic power increase. Multiplier decision window (MDW) can be used to solve switching problem.The control signal generator inside MDW counts 'm' consecutive input samples that are smaller than x_{th} and turns off multipliers if and only if 'm' consecutive input samples are smaller than x_{th} and the coefficients of the corresponding multipliers are also less than Coeff_threshold.

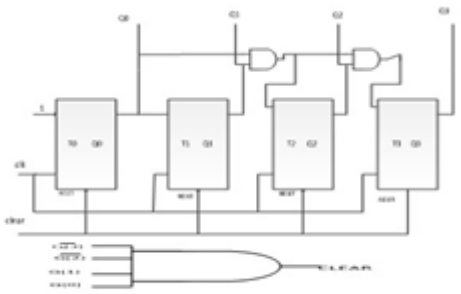

Figure5. Schematic diagram of Ctrl signal Generator.

The in_{ct} signal (from fig.3) is added to the input sequence to indicate a particular input sample is smaller than x_{th}. The multiplier turn _off_ logic (from fig.6) can be used to turn off the multiplier if the amplitude of both the input data and coefficients are smaller than x_{th} and c_{th}.
Multiplier_turn_off_logic =~(in_{ct}*Coef f_{ct})

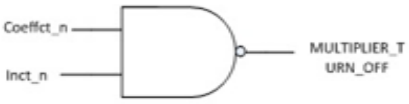

Figure 6 Multiplier_turn_off_logic

Where Coef f_{ct} = 1;if Coeff<c_{th}
Coef f_{ct}= 0; Otherwise

C. Pipelining latches:

Pipelining is done by introducing pipelining latches in the feed forward paths of FIR filter. Pipelining is done to reduce the critical path caused by additional hardware and to increase the speed of operation. Finally the overall area overhead of the modified reconfigurable FIR filter when compared with ordinary filter is a single AD logic, counter and nand gates.

D. Mathematical Analysis:

- P (tap) = (total power/#taps) * (16/#bits coeff) * (16/#bits sample) * (2.5/Vdd) 2 * (0.25/tech) * (100/clkfreq). Where P (tap)=Power/multiplier [1].

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

➢ $P_{saving}=1-(P_{reconfig}/P_{conventional})$.

IV. EXPERIMENTAL RESULTS

The data aware reconfigurable FIR is synthesized using cadence RTL compiler in 45nm CMOS process. The date aware reconfigurable FIR is implemented with following specifications:

45 nm TECHNOLOGY:
Filter specifications:
Order=9
MDW size=4
Input data=8-bit
Output data=16-bit
Data threshold =10
Filter coefficients=8-bit
Coefficient threshold=20.

A. COMPARISON TABLE FOR ORDINARY AND RECONFIGURABLE FIR FILTERS

Parameter	Ordinary FIR filter	Data Aware Reconfig FIR filter
Area(μm^2)	416	539
Power(nW)	280516.413	243140.485

Table 1

Powersavings = (0.28-0.24)/0.28=14.5%
Area overhead= 22%.

From Table 1, the data aware reconfigurable FIR filter achieved a power savings of 15% at the cost of 22% area overhead to that of the ordinary FIR filter. If we want to achieve higher power savings, the MDW (from fig 3) size has to be increased accordingly. This clearly shows a trade-off between amount of power saving and performance degradation.

B. COMPARISION BETWEEN RECONFIGURABLE FIR AND RECONFIGURABLE FIR WITH PIPELINING IN 45nm TECH.

45nm	Data Aware Reconfig FIR	Pipelined Reconfig FIR
No.of.cells	539	757
cell area	1738	2542.09
Leakage power (nW)	73.592	112.36
Dynamic power (nW)	243066.533	634548.08
Total power (nW)	243140.85	634660.44

Table 2

C. COMPARISON OF POWER REDUCTION OF OUR PROPOSED 25-TAP RECONFIGURABLE FIR WITH PREVIOUS WORKS

Ref	Filter de-scrip-tion	Tech	Total power	P(tap)	1-p_r
3	8taps 10x10	0.5	240mW at 10MHz	-	39%
4	48tap 16x12	0.25	0.28mW at 2.5v,44.1KHz	23.4	29%
5	Equirip 2.88 8x8	0.35	16.5mW at 2.5v,86MHz	19.03	-
Our work	25taps 16x16	0.045	5.9mW at 0.8V,209MHz	0.045	33%

Table 3

- Technology inμm
- P (tap) in μW

From Table 3, the result shows that the proposed FIR filter has improved power efficiency when compared to references [3],[4],[5].With the architecture discussed above power efficiencies up to 33% can be achieved.

V. CONCLUSION

In this paper we modified the reconfigurable FIR filter by adding pipelining latches to trade off the filter performance such as speed, power etc. In the presented architecture the input samples are continuously monitor and the multipliers are turn off if the amplitudes of both the data input and filter coefficients are small. Pipelining is done either to achieve high speed or to achieve power savings at the same clock speed. By carefully choosing MDW size, filter coefficients we can get power savings up to 5 to 25%.

REFERENCE

1. Seok-Jae Jee ,Li-Woong Choi, Seon Wook Kim, and Jongsun park,"Reconfigurable FIR Filter Architecture To Trade Off Filter Performance For Dynamic Power Consumption," IEEE Trans. Very Large Scale Intergr. Syst.,vol.19, NO. 12, pp.2221-2228, Dec.2011.
2. JohnG.Proakis,DimitrisG.Manolakis,"Digital Signal Processing: Principles, Alogrithms, and Applica- tions, 4thedition, published by Pearson Educa- tion,Inc.,"
3. Z. Yu, M.-L. Yu, K. Azadet, and A. N. Wilson, Jr, "A low power FIR filter design technique using dynamic reduced signal representation," in Proc. Int. Symp. VLSI Tech., Syst., Appl.,2001,pp.113–116.
4. S. Hwang, G. Han, S. Kang, and J. Kim, "New distributed arithmetic algorithm for low-power FIR filter implementation," IEEE Signal Process. Lett., vol. 11, no. 5, pp. 463–466, May2004.
5. K.-H. Chen and T.-D. Chiueh, "A low-power digit- based reconfig- urable FIR filter," IEEE Trans. Circiuts Syst. II, Exp. Briefs , vol. 53, no. 8,pp.617-621,Dec.2006.
6. Alan V. Oppenheim, Ronald W. Schafer,"Digital Signal Processing,"l'1975 by Prentice- Hall, Inc., Englewood Cliffs, N.J., U.S.A.

AUTHOR PROFILE

M.Bharath Reddy: Pursuing M.Tech in VIT University, vellore,India. Published paper on Digital PLL in international journal. Currently working as intern in intel corporation.

M.Sai Sarath Kumar: Pursuing M.Tech in VIT University,Vellore,India. Published paper on Digital PLL in international journal. Interested in analog circuits.

B. Suresh Kumar: Pursuing M.Tech in VIT University,Vellore,India. Published paper on Digital PLL in international journal.Interested in digital circuits.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)