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The Comparative Study of FPGA based FIR Filter Design Using Optimized Convolution Method and Overlap Save Method

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Abstract: ***This paper describes a comparative study of designing digital filter of long duration sequences. Here we have adopted the approach of block filtering scheme "overlap save method" and compare with the optimized linear convolution scheme for designing digital filter. We have implemented both methods in FPGA Spartan 3A starter kit, XC3S700A device.***

Implementing both algorithms in FPGA hardware platform reveals that there is a 67% area reduction and 70.6% increase in operating frequency in overlap save method compare to optimize convolution method. In addition the power utilization summary reveals that there is a 24.24% increased in the power utilization of overlap save method. Thus the experimental results shows that to design an area optimized , high speed digital filter we should used overlap save method where as for a power efficient digital filter we should used optimized linear convolution method.

Index Terms: FIR,MATLAB, Linear convolution.

I.INTRODUCTION

Digital signal processing has a broad application in the field of real time signal processing operation such as speech processing, Audio Compression, Digital Image Processing, radar signal processing and different media applications[1]. These computation intensive real time applications requires digital filter to perform the signal processing operation. A digital filter is an important class of linear time invariant system (LTI) that performs on a sample discrete time signal to reduce or enhanced certain aspect of that signal[2]. In this paper we focus on designing low pass FIR filter using the overlap save method technique. The general form of digital filter difference equation is given below in equation (1)[2].

$$y(n) = -\sum_{k-1}^{N} a_k\, y(n-k) + \sum_{k=0}^{M-1} b_k\, X(n-k) \qquad (1)$$

Where Y(n) is the current filter outputs, the Y(n-k)'s are current or previous filter inputs, the aK's are the filter's feed forward co-efficient corresponding to the zeros of the filter, the bK's are the filter's feedback co-efficient corresponding to the pole of the filter, and N is the filter's order.

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Depending upon the filter co-efficient there are two type of digital filter, frequency selective and adaptive digital filter.

We have designed low pass FIR filter using MATLAB FDA tool. Here we have developed overlap save method structure and optimized linear convolution method of designing digital filter and synthesized this structure using Xilinx ISE 13.4 synthesis tool and implemented in Spartan 3A. In our paper we have proposed that the long input sequences can be processed using optimized overlap save method technique of designing digital filter. This technique leads to reduction in the critical path, power consumption and at the same time it increases the clock frequency in comparison to optimized linear convolution method of designing digital filter. The rest of the paper is MATLAB FDA tool is shown in section 2.The FPGA implementation of overlap save method structure is given in section 3. The FPGA implementation of linear convolution structure is shown in section 4.section 5 contains the comparative study and calculation of noise variance. Section 6 contains the conclusion.

II.DESIGN OF FIR FILTER USING MATLAB FDA

For signal processing operation finite impulse response (FIR) filter plays an important role, these are the digital filter that computes the output response as the weighted, finite term-sum of past, present and future values of the filter input as given in equation (2)[3].

$$Y(n) = \sum_{k=M_1}^{M_2} b_k x(n-k) \qquad (2)$$

Where M1, M2 are finite. In this paper we will design a causal FIR (finite impulse response) filter; the difference equation is given as below in equation (3) .

$$Y(n) = \sum_{k}^{M} b_k x(n-k) \qquad (3)$$

Where M is finite. To design this low pass digital filter, we will use MATLAB FDA as the synthesis tool; the specification of the filter is shown in the table I. Depending upon the specification, we will have the transfer function co-efficient as shown in the table II. The difference equation of the FIR filter is given in equation (4)

$$y(n) = h(0)x(n) + h(1)x(n-1) + h(2)x(n-2) \qquad (4)$$

The magnitude and phase plot of this filter is shown in the figure (1).

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We have adapted the rectangular window method to design the filter in MATLAB FDA tool[4]. The truncated impulse response of the filter after passing through the rectangular window is given in equation (5)

$$h(n) = h_d(n)w_r(n) \quad (5)$$

Where $w_r = \begin{cases} 1 & 0 \le n \le M \\ 0 & otherwise \end{cases}$

processing the long duration data is to break into blocks and process by circular convolution[4] . In the last stage these blocks of circular convoluted data are to be processed and $h_d(n)$ is the impulse response of the causal FIR filter. by two methods- overlap save method and overlap add method .In this two method while computing the data the circuit diagram of overlap add method requires more hardware components in comparison to overlap save method.

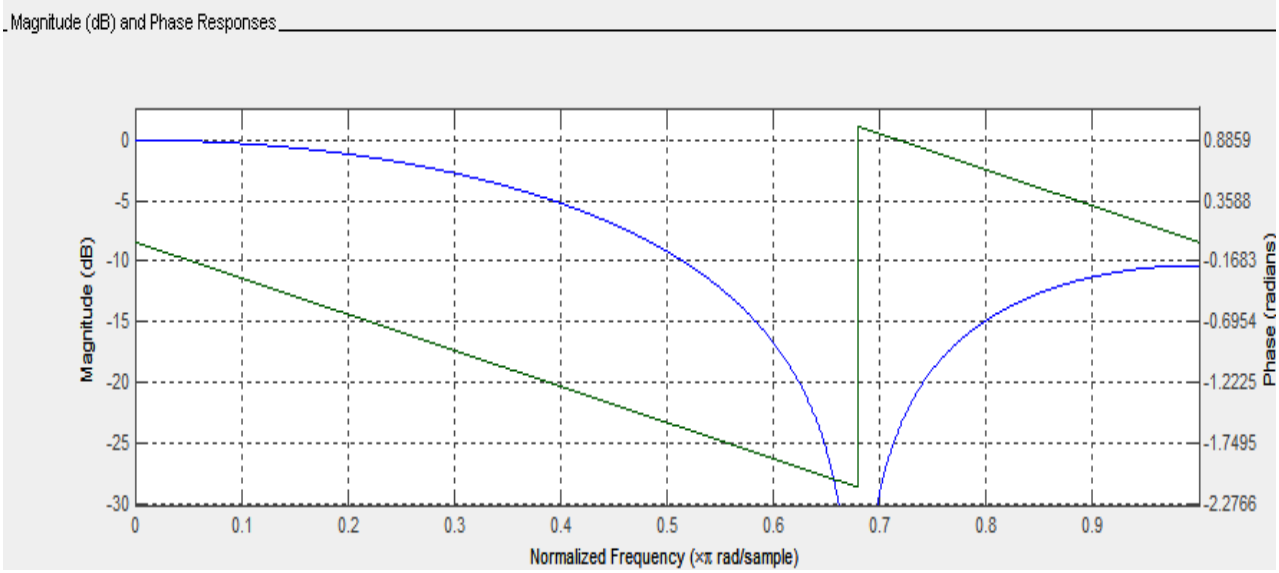

Fig.1. Magnitude and Phase plot of the FIR filter

In frequency domain, we can represent this truncated impulse response is shown in the equation (6).

$$H_d(e^{jw}) = \frac{1}{2\pi}\int_{-\pi}^{\pi} H_d(e^{jw})\, w(e^{j(w-\theta)})d\theta \quad (6)$$

Table I

Properties	Specification
response	low pass
order	2nd
table	Yes
window	rectangular window
cut-off frequency (wc)	0.198
attenuation at cut-off frequency	6 db

Table II

Transfer function	Co-efficient
h(0)	0.325996
h(1)	0.3480081
h(2)	0.325996

III. IMPLEMENTATION OF FIR FILTER USING OVELAP SAVE METHOD

In order to generate the output response y (n) of a digital filter, we have to perform the linear convolution between the input sequence & the impulse response. If a long duration input sequence is to be processed then the convolution results more hardware utilization as well as higher computation time delay ,therefore an effective way of

Thus in this paper we will design over FIR digital filter using an optimized, computation effective algorithm of overlap-save method.

In this method we consider the input data having the length L & the impulse response having the length M. the block length of the input data should have the size N=L+M-1[6,7] . Thus the block of data sequences is given by,

$$x_1(n) = \left\{ \underbrace{0,0,0,..,0}_{(M-1)zeros}, x(0), x(n) \dots x(L-1) \right\} \quad (7)$$

$$X_2(\mathrm{n}) = \left\{ \underbrace{\mathrm{x(L-M+1),\dots,x(L-1)}}_{\text{Last (M−1) data points from } x_1(\mathrm{n})}, \underbrace{\mathrm{x(L)\dots,x(2L-1)}}_{\text{L new data points}} \right\} \quad (8)$$

$$X_3(n) = \left\{ \underbrace{x(2L-M+1),..,x(2L-1)}_{Last\ (M-1) data\ points\ from\ x_2(n)}, \underbrace{x(2L)..,x(3L-1)}_{L\ mew\ data\ points} \right\} \quad (9)$$

The response of the FIR filter is now computed by the circular convolution method [8]:

$$Y_i(n) = X_i(n) \textcircled{N} h(n) \quad (10)$$

By putting the value of i we obtain the equation given bellow:

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$$Y_1(n)=\left\{\underbrace{y_1(0),y_1(1)}_{\text{discard}},y_1(2),y_1(3),y_1(4)..\right\} \quad (11)$$

$$Y_2(n)=\left\{\underbrace{y_2(0),y_2(1)}_{discard},y_2(2),y_2(3),y_2(4)..\right\} \quad (12)$$

The final output response,

$$y(n)=\{y_1(2),y_1(3),y_1(4),y_2(2),y_2(3),y_2(4)\} \quad (13)$$

A. FPGA based design of the overlap save method algorithm

In order to design the architechere of overlap save method we will divide over structure into two parts – controller and data path.we have used the approach of finite state machine for the design of controller part, the input of the controller part is the input data sequence and the output is the blocks of data sequences. Thus the FSM controller will divide the long duration input sequence into a fixed block size given by the equation (7), eqation (8) and eqation (10). The output of the controller is attached with data path as shown in the diagram figure(2). The data path is again divided into two sub blocks. The first subblocks is nothing but a ring counter that produce a impulse response as required during the computation of the circular convolution as shown in the diagram figure(2).The second subblock consists of multipliers and adders that requires during computation of the circular convolution.we have used 8 bit array multiplier and 8 bit ripple carry adder to perform the fast computation of the input sequence .The output of these second subblocks is connected to a shift register as shown in the diagram figure(2).These serial shift register is used to implement the overlap save method.From the five output response of each serial shifted data we will discard the left most output response as given in the equation(14).

$$Y_1(n)= X_1(n) \textcircled{N} h(n)$$

$$=\left\{\underbrace{y_1(0),y_1(1)}_{\text{discard}},y_1(2),y_1(3),y_1(4)..\right\} \quad (14)$$

Thus the final output block will starts from the output 3

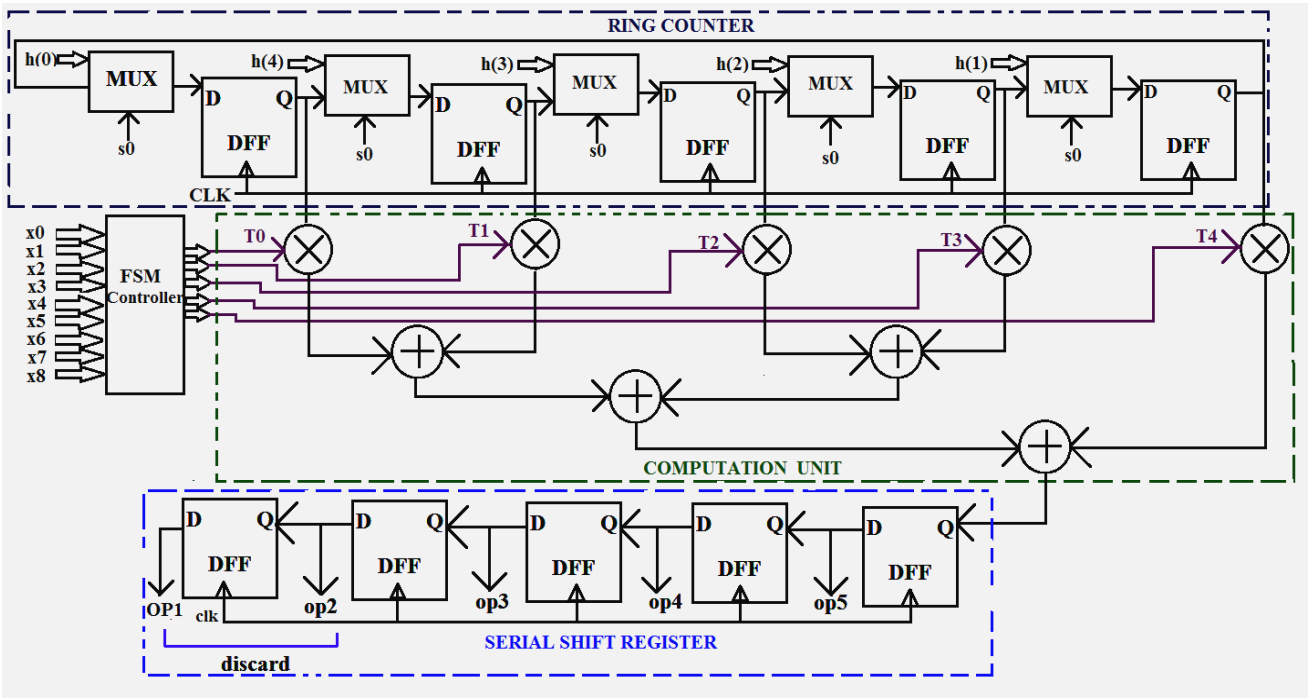

Fig. 2. Circuit diagram of the overlap save structure

A. Simulation results

We have design our structure using VHDL language and implemented in spartan 3A, starter kit,device XC3S700A.The simulation results of the overlap save method with different blocks of the input is shown in the figure(4a) and figure(4b).The table III shows the simulated output results exact valuer,its approaxmiate values and error generated due to approaximation.The figure (3) shows the plot of the input samples vs error in order to calculate the variance of output noise.From the error vs sample plot we find that as the number of sample increases with each iteration, error also increases linearly.

Variance output noise [2] $\partial_e^2 = \frac{N2^{-b}}{12} = 0.001953$ (15)

B. Device utilization

We have implemented the structure in spartam-3A starter kit in the device XC3S700A.The device utilization summary , the maximum computation path delay & the power utilization of this structure is given in the table below (IV)

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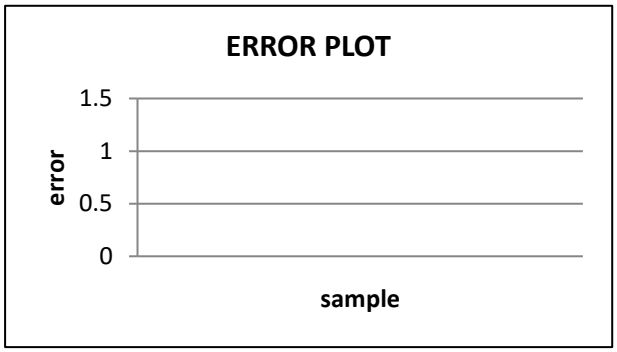

Fig.3. Sample versus Error plot

Table III

Input sequence	Actual value of output sequence(y)	Approximate value of output sequence (x)	Deviation(y-x)	Binary equivalent value of output
1.0	0.325996	0.3203125	0.0056835	000000000.0101001
2.0	1.0000001	0.984375	0.0156251	000000000.1111110
3.0	2.0000002	1.96875	0.03125	000000001.1111100
4.0	3.0000003	2.953125	0.0468753	000000010.1111010
5.0	4.0000004	3.9375	0.0625004	000000011.1111000
6.0	5.0000005	4.921875	0.0781255	000000100.1110110
7.0	6.0000006	5.90625	0.0937506	000000101.1110100
8.0	7.0000007	6.890625	0.1093757	000000110.1110010
9.0	8.0000008	7.875	0.1250008	000000111.1110000
0	5.7400409	5.65625	0.0837909	000000010.1010100
0	2.933964	2.8828125	0.0511515	000000010.1110001

Table IV

Logic device utilization summary		Path delay and frequency required to implement the circuit		Power utilization (w)	
Total Number of slices register	180	Minimum period	27.100ns	Total power	0.041
Number of slice flip flops	140	Maximum Frequency	36.900MHz	Dynamic power	0.009
Number of 4 input LUTs	1167	Minimum input arrival time before clock	5.815ns	Quiescent power	0.032
Number of used latches	40	Maximum output required time after clock	5.668ns	-	-

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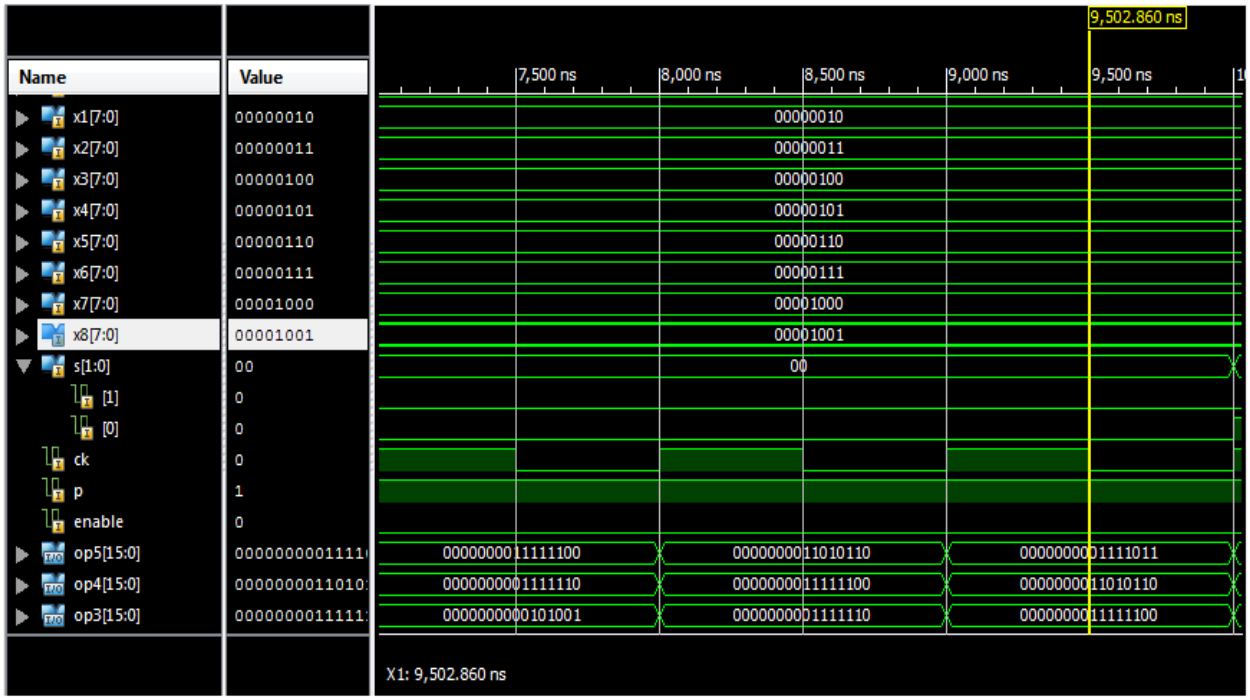

Fig. 4a. Simulation waveform of overlap save structure when select line (s =’00’)

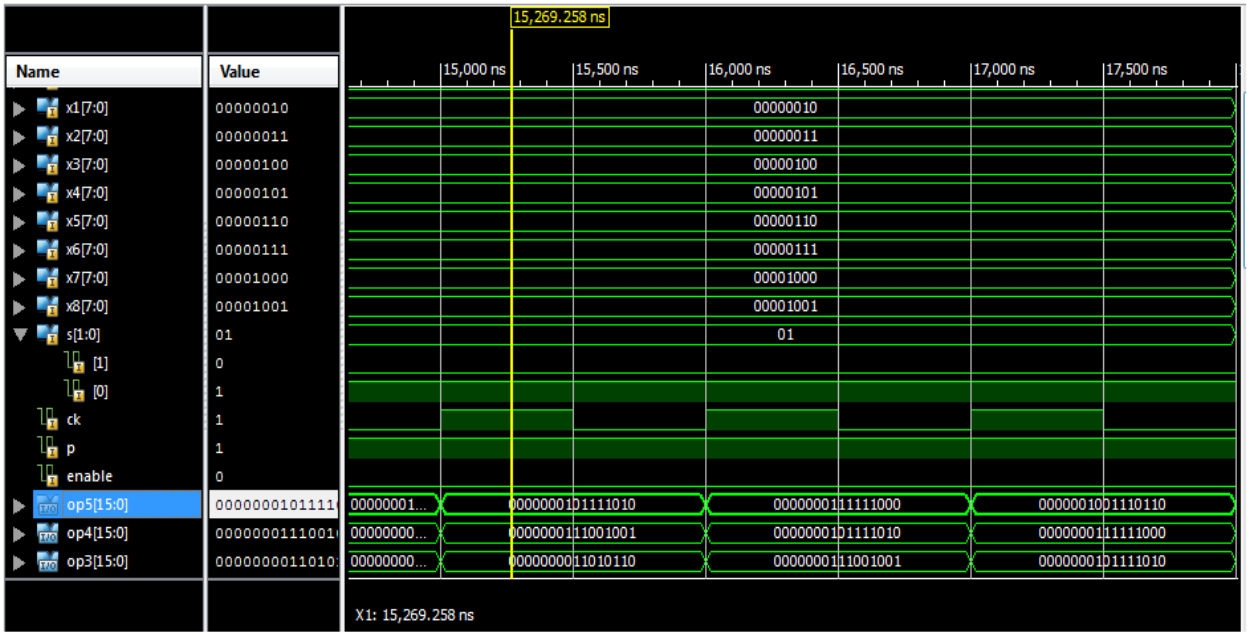

Fig. 4b. Simulation waveform of overlap save structure when select lines (s=’01’)

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IVOPTIMIZED LINEAR CONVOLUTION METHOD

To perform the signal processing operation, we have to study the impulse response of a system. In DSP system convolution is a mathematical tool for the study of the output response of a system. Thus we can find the output response of a linear time invariant system by using the technique of convolution[9].

$$Y(n) = \sum_{k=-\infty}^{\infty} x(k)h(k) \qquad (16)$$

This equation (16) is denoted by,

$$Y(n) = x(n) * h(n) \qquad (17)$$

Here x(n) is the input sequences, h(n) is the impulse response & y(n) is the output sequences. In this paper we have designed a low pass FIR filter using overlap-save method, now we will verify the output response of the system using the optimized convolution circuit.

In this circuit we have used an only one array multiplier and a ripple carry adder with array of multiplexer as a switching element to generate the output respons of the FIR low pass filter.

The proposed architecture is divided into two blocks**:** one for input sequences analysis and another for the generation for the output sequences. In this paper input circuit depending upon the control signal the input sequences multiplied with the impluse response in order to generate the intermidiate sequences. In the output circuit,the intermidiate signals are added as shown in the figure(5b) to produced the final output results. According to the table V generarion of output response for the various combination of control lines are shown below.

A. Simulation result

We have design our structure using VHDL language and implemented in spartan 3A starter kit,device.

The simulation results of the linear convolution with different inputs are shown in the figure(6a) and the output response is shown in the figure(6b).

B. Device utilization

We have implemented the structure in Spartan 3A starter kit in the device XC3S700A.The device utilization summary the maximum computation path delay & the power utilization of this structure is given in the table below (VI)

Table V

p_0 p_1	s_0 s_1 s_2 s_3	t_0 t_1 t_2 t_3 t_4	u_0 u_1 u_2 u3	Final output
0 0	0 0 0 0	0 0 0 0 0	-	Y0
0 1	0 0 0 0	0 0 0 1 0	0 0 0 0	Y1
1 0	0 0 0 0	0 0 1 0 1	0 0 1 0	Y2
1 0	0 0 0 1	0 1 0 0 0	0 1 0 0	Y3
1 0	0 0 1 0	0 1 0 1 1	0 1 1 0	Y4
1 0	0 0 1 1	1 0 0 0 1	1 0 0 0	Y5
1 0	0 1 0 0	0 0 1 0 0	1 0 1 0	Y6
1 0	0 1 0 1	1 0 1 1 1	1 1 0 0	Y7
1 0	0 1 1 0	1 1 0 1 0	1 1 1 0	Y8
1 0	0 1 1 1	1 1 1 0 0	1 1 1 1	Y9
1 0	1 0 0 0	1 1 1 0 1	-	Y10

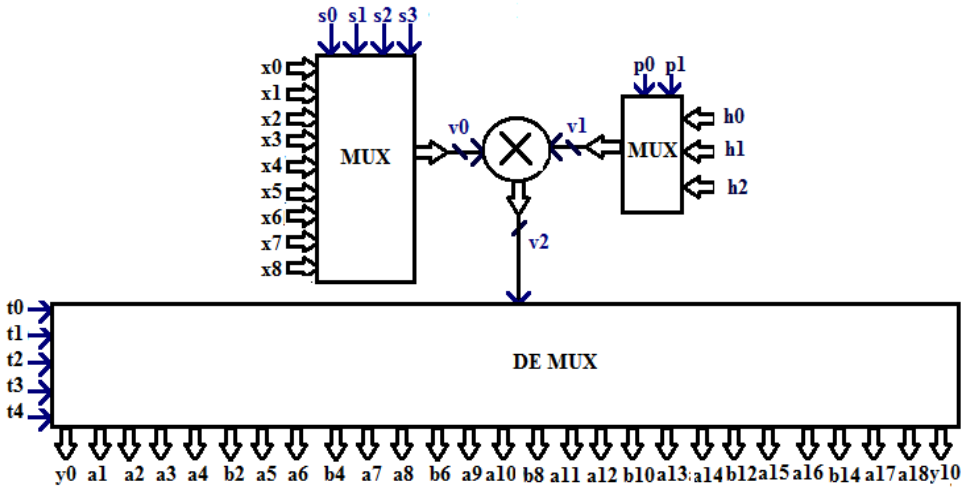

Fig.5a. input circuit diagram of linear the convolution structure

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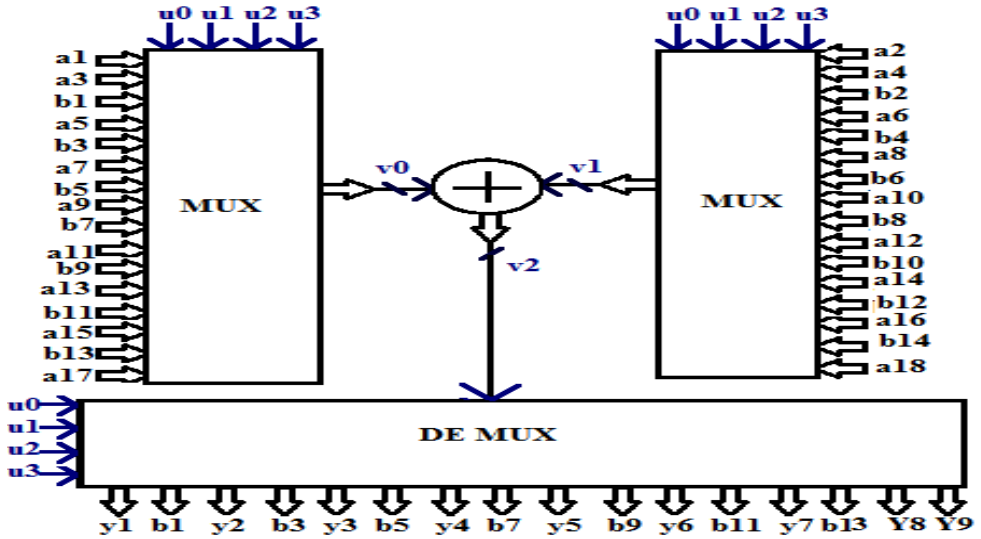

Fig.5b. output circuit diagram of linear the convolution structure

Table VI

Logic device utilization summary		Path delay and frequency required to implement the circuit		Power utilization (w)	
Total Number of slices register	543	Minimum period	7.959ns	Total power	0.033
Number of slice flip flops	27	Maximum Frequency	125.644MHz	Dynamic power	0.002
Number of 4 input LUTs	623	Minimum input arrival time before clock	31.070ns	Quiescent power	0.032
Number of used latches	516	Maximum output required time after clock	5.668ns	-	-

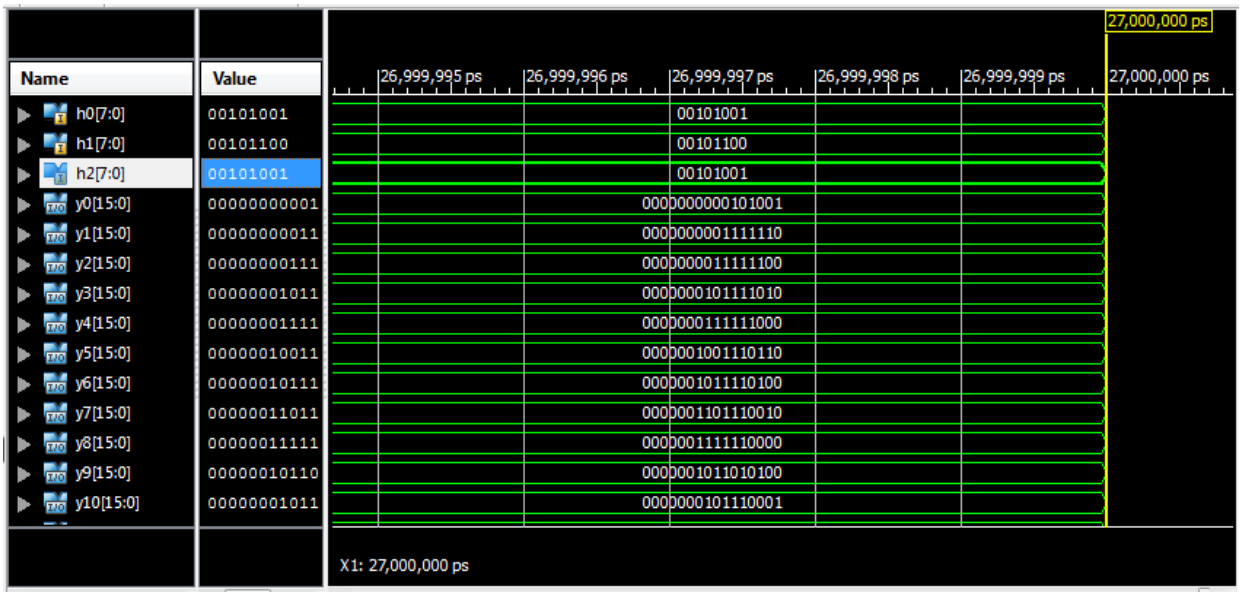

Fig.6b. Output waveform of the linear convolution structure

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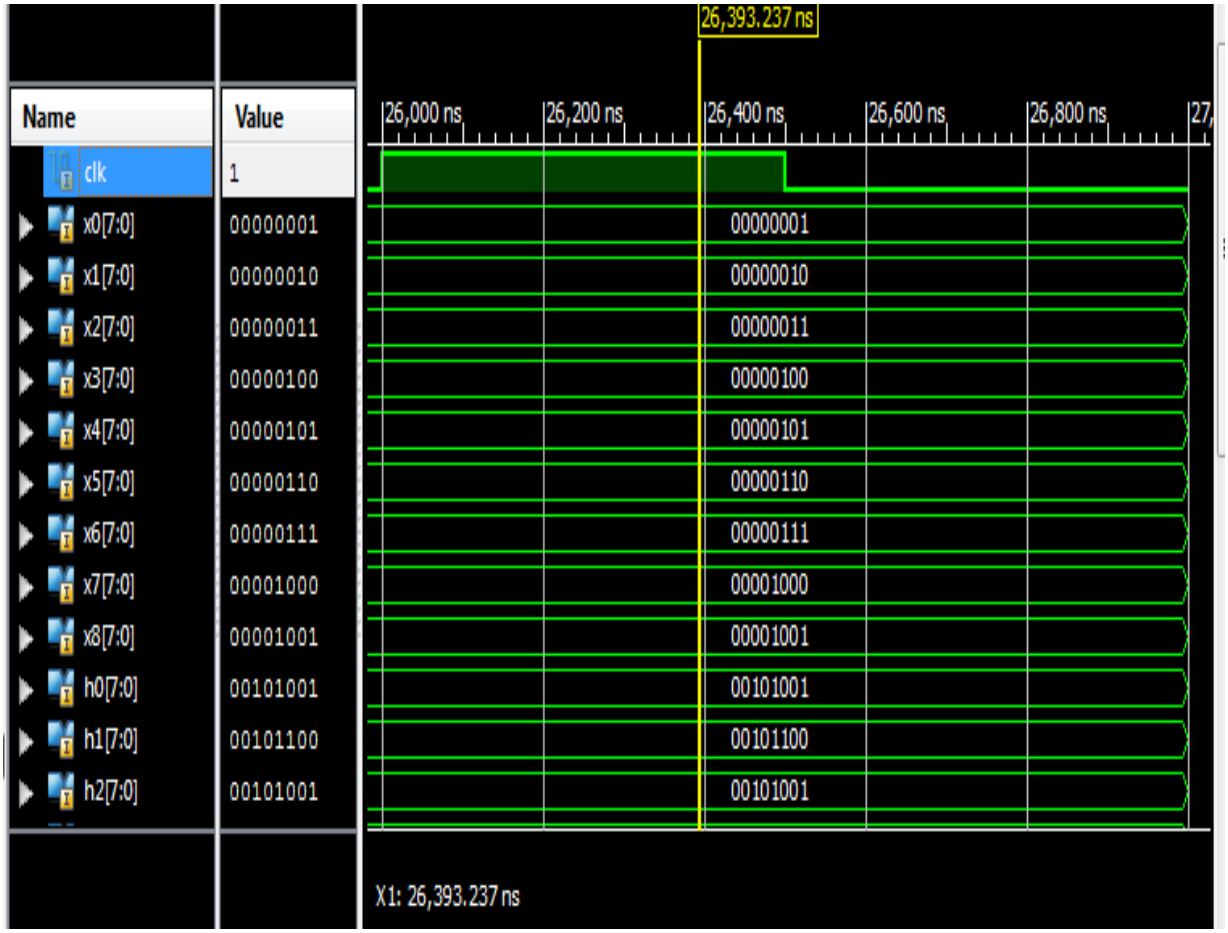

Fig.6a. Input waveform of the linear convolution structure

V. COMPARATIVE STUDY

The comparative study between the optimized convolution method and overlap save method shows that there is a 67% area reduction, 70.6% increase in operating frequency of overlap save method in comparison to linear convolution method .Thus for a area efficient high speed application we can prefer overlap save method but as the overlap save method structure used sequential logic for the operation thus the dynamic power consumption for this circuit is higher than optimized linear convolution method, thus to design a low power structure of a filter we will prefer optimized linear convolution structure.

VI. CONCLUSION

This paper has presented a comparative study of a designing FIR filter of long duration sequences using both optimized convolution method and overlap save method. The FPGA implementation results shows that for a area optimized, high speed FIR filter design application we can preferred overlap save method. But for a low power FIR filter design application we can preferred optimized linear convolution method

REFERENCES

1. Leila Ismail, Member, IEEE Computer Society, and Driss Guerchi,, "Performance Evaluation of Convolution on the Cell Broadband Engine Processor" IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, VOL. 22, NO. 2, FEBRUARY 2011.
2. S Poornachandra and B Sasikala,"signal and system Tata", McGraw Hill , 3rd edition , 2010.
3. Zdenka Babic, Danilo P. Mandic,"A Fast Algorithm for Linear Convolution of Discrete Time Signals",5th International Conference on telecommunicationin modern satellite, cable and broadcasting service 2001.
4. P.Ramesh Babu," Digital Signal Processing",Scitech publications,3rd edition Feb 2006.
5. Sumit Kumar Maity , Madhusudan Maiti, "A comparative study on FPGA based FIR filter using broadcast structure and overlap save method", International Journal of Advanced Research in Computer Science and Electronics Engineering (IJARCSEE) Volume 1, Issue 9, November 2012.
6. Pramod Kumar Meher,, "Parallel and Pipelined Architectures for Cyclic Convolution by Block Circulant Formulation Using Low-Complexity Short-Length Algorithms", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 18, NO. 10, OCTOBER 2008.
7. John W. Pierre," A Novel Method for Calculating the Convolution Sum of Two Finite Length Sequences", IEEE TRANSACTIONS ON EDUCATION, VOL. 39, NO. 1, FEBRUARY 1996.
8. Hideo Murukumi,,"GENERALIZATION OF THE CYCLIC CONVOLUTION SYSTEM AND ITS APPLICATIONS", IEEE International conference on acoustics ,speech and signal processing, 2000.
9. Khader Mohammad, Sos Agaian, "Efficient FPGA implementation of convolution", IEEE International Conferenceon Systems, Man, and Cybernetics San Antonio, TX, USA - October 2009.

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