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Investigation and Implementation of Step-Down Transformerless S S Single Switch AC/DC Converter

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Abstract: ***A transformerless single-stage single switch AC/DC converter with direct power transfer is presented in this paper. Unlike existing single-stage ac/dc converters with uncontrolled intermediate bus voltage, a new high step-down transformerless single-stage single switch ac/dc converter achieving intermediate bus voltage regulation and output voltage regulation is proposed. With the direct power transfer feature, the converter is able to achieve efficient power conversion, low voltage stress on intermediate bus (less than 120V) and low output voltage. The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. A detailed analysis of the proposed converter for regulated intermediate bus voltage and output voltage with simulation results are presented in this paper a prototype circuit is implemented to verify the performance.***

Keywords: AC/DC, (PFC).

I. INTRODUCTION

Efficient AC-DC power conversion has been of much interest in recent years with the wide increase in electronic devices which demand clean DC power supplies. The objectives for researcher and engineer in designing AC/DC converters are high efficiency, low cost, small size and high power factor. In order to meet the international regulations and standards [1] they require two stage architecture. Power factor correction (PFC) stage followed by a DC-DC stage. A two stage approach mostly uses a boost PFC circuit for the first stage. This is because of the good PFC capability and high efficiency provided by this circuit. The consequence of using it in the first stage is the high voltage output which requires a capacitor with high voltage rating resulting in increase in size and cost. This voltage can reach very high values at low load conditions as indicated in [2].

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In normal practice, two-stage approach refers to a wide input PFC converter, which is for tracking the line input current with the source voltage, cascaded with a DC/DC converter that is for achieving fast and tight output voltage regulation. However, this approach usually suffers from efficiency penalty, high cost, large size and complex control circuits resulted from two separated power stages compared with the single-stage counterpart. As for single-stage approach (SS), it is a very attractive solution in low power application as two power stages (PFC cell and DC-DC cell) are combined in sharing common switching devices, storage elements and control loop leading to reducing size and cost of converter, also enhancing conversion efficiency. Lately, there were numerous of single stage circuits reported [2-5],[7-9].

For the sake of circuit simplicity, most PFC cells in SS AC/DC converter are a boost cell for which the output voltage is always greater than the input voltage. At high line application, therefore, this output voltage usually exceeds 450V causing high voltage stress on bulk capacitor and switching devices. It has been reported that this intermediate bus voltage can easily exceed 1000V [3],[4],[7] leading to very limited and costly selections of switching devices and storage capacitor. A single stage approach combines the PFC stage and DC-DC converters to provide a less complex and compact solution. A single power stage circuit is formed by integrating a boost PFC converter with a two-switch clamped flyback isolated converter [5] The current stress of the main power switch is reduced due to separated conduction period of the two source currents flowing through the power switch. The current from two input sources (ac main and bus capacitor) can be separately controlled in the power circuit. As only one of the two currents passes the switches at a time within each switching period, Current stress on power switches is reduced [5]. However, transformer which couple the energy stored in the magnetizing inductance to output load at transistor turnoff period, increases the size and cost of the converter.

The recent transformerless AC/DC power converter architectures are compared [6] and provides an assessment of each. Therefore, a non-isolated (trfr.less) SS AC/DC is worth for reducing size and cost of converter, and keeping away from undesirable effect associated with the leakage inductance in the transformer i.e. voltage spike on power switch.[6] The converter shown in Fig. 1 is an Integrated Boost Buck-Boost single stage ac-dc converter [7],[9]. It uses the technique of direct power transfer to improve the efficiency and also keeps the voltage of the first stage at less than 400V in light load conditions.

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Its intermediate bus voltage can keep lower than 400V even in light load and universal line input conditions by using the concept of direct power transfer or reduced redundant power processing.

The voltage stress on the intermediate bus capacitor kept around 357.4V with double line frequency ripples under high line operation providing that the output voltage was 100V. Although the reported IBoBuBo converter [7],[9] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell.

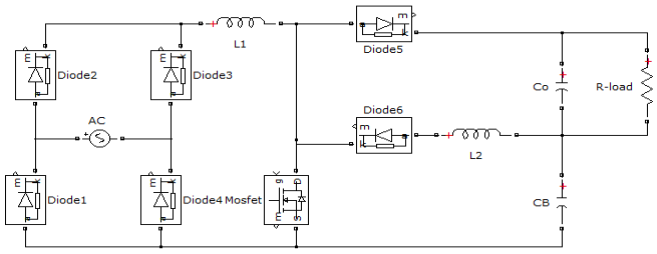

Fig. 1. Integrated Boost Buck-Boost single stage ac-dc converter [7],[9].

In this paper, a transformerless single-stage single-switch AC/DC converter is proposed by integrated buck PFC cell with a buck–boost DC/DC cell with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. An integrated buck–buck–boost (IBuBuBo) converter is proposed in this paper to achieve low intermediate bus and output voltages in the absence of transformer, simple control structure with a single-switch, high conversion efficiency due to part of input power is processed . The intermediate bus voltage and output voltage of the proposed buck–buck–boost (IBuBuBo) converter are compared with that of IBoBuBo converter [7],[9] by simulation . Further reduction of bus voltage and output voltage can be achieved with this proposed converter.

Therefore, a transformer is not needed to obtain the low output voltage. Section II gives a review of circuit operation briefly. The circuit design considerations will be given in section III. The simulation results and discussion are given in Section IVand V respectively. Experimental setup is shown in section VI verify the proposed circuit. Conclusion is stated in Section VII.

II. PROPOSED CIRCUIT AND ITS PRINCIPLE OF OPERATION

The schematic of the proposed IBuBuBo converter which is constituted by merging of buck PFC cell (L_1 S_1 D_6 C_o & C_B) & a Buck- Boost DC cell (L_s S_1 D_5 D_7 C_o & C_B)is illustrated In fig(2). Even though L_2 is the return path of the buck PFC cell, it will not contribute to cell. We operate both the cell in DCM mode so no currents in both inductor at the beginning of each switching cycle T_0.

Operating Mode1 (v in$(\Theta) \leq V_B$+Vo) : when the input voltage (v in(Θ)) is less than that of the V_T, where V_T is is the sum of bus voltage and output voltage. The operation of the circuit can be divide into three stages based on the current waveforms in Fig. 3Stage 1 (time period d1Ts): The inductor L2 current is charged linearly by the bus voltage VB when switch S1 is turned ON and diode D5 is forward biased . So the output capacitor sustains the load power

1. Stage 2 (time period d2Ts):The diode D7 becomes forward biased when the switch S1 is turned OFF. The energy stored in L2 is released to Co and to the load.
2. Stage 3 (time period d3Ts-d4Ts):The load current is only due to Co and the inductor current is totally discharged.

Operating Mode 2(v *in*$(\Theta) > V_T$): In this mode the input voltage is greater V_T, where V_T is the sum of output voltage and bus voltage. The operation the circuit can be divided into four stages based on the current waveforms in Fig 4

1. Stage 1 (time period d1TS): when the switch S1 is turned ON, inductors L2 & L1 charge linearly by the input minus the sum of output voltage and the bus voltage(v in –(Vo+VB))and diode D5 is conducting.
2. Stage 2 (time period d2Ts): The inductor current `iL1 decreases linearly when is turned OFF. Due to which the capacitor CB and Co charge through diode D6, as well as transferring part of input power directly to the load. The energy stored in L2 is discharged through Co and the current is supplied to the load through the diode D7. This continues till the inductor L2 is fully discharged.
3. Stage 3 (time period d3Ts): The inductor L1 delivers current to Co and the load continually till it reaches zero.
4. Stage 4 (time period d4Ts): Only capacitor Co deliver the output power.

III.DESIGN CONSIDERATION

Assumptions made to simply the circuit analysis

1) All components are ideal.
2) The switching frequency fs is much greater than line frequency so that the rectified line input voltage $|v$ in $(\Theta)|$ is constant within the switching period.
3) Pure sinusoidal input source is used i.e. v in (Θ) =Vpk sin(Θ) where Θ and Vpk are denoted as in phase angle and peak voltage respectively.
4) Both capacitors Co and CB are large enough such that they can be treated as constant DC without any ripple.

From fig (3) no input current is drawn from the source in Mode 1 therefore the phase angle can be expressed

$$V_{pk} \sin(\alpha) = V_T \qquad (1)$$

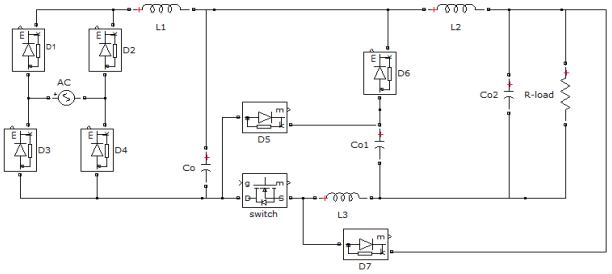

Fig.2. Proposed IBuBuBo

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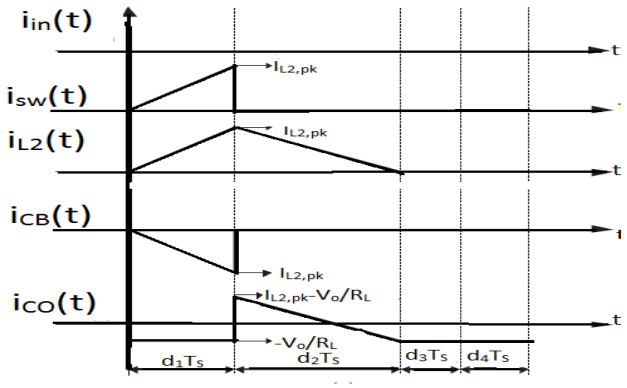

Fig.3. Current waveforms for mode 1 operration

$$\text{Sin}(\alpha)= \frac{VT}{Vpk} \qquad (2)$$

$$\alpha = \arcsin\left(\frac{VT}{Vpk}\right) \qquad (3)$$

$$\beta = \pi - \alpha = \pi - 2\arcsin\left(\frac{VT}{Vpk}\right) \qquad (4)$$

The conduction angle γ is given by

$$\gamma = \beta - \alpha = \pi - 2\arcsin\left(\frac{VT}{Vpk}\right) \qquad (5)$$

Where V_T is sum of output voltage and bus voltage.
In general the voltage across the inductor is

$$e_L = L\frac{di}{dt}$$

At the time d_1T_s

$$V\text{in} - V_T = L\frac{iL1_{pk}}{d1Ts}$$

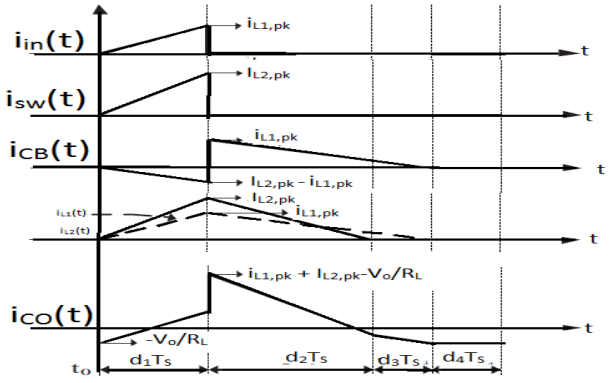

Fig.3. Current waveforms for mode 2 operation

$$\grave{i}_{L1\_pk} = \left\{ \begin{array}{ll} \frac{(v\,in(\theta)-VT)d1TS}{L} , & \alpha < \theta < \beta \\ 0 & otherwise \end{array} \right\} \qquad (6)$$

Where T_S is time period of switching period of the converter i.e. $T_S = 1/f$
From equation 6 we can see that is independent of the sine term and L_2 does not contribute in equation 3 even it on the current return path of the PFC cell.
By considering volt-second balance (total area) of L_1 and L_2, the duty ratio can be given as

$$d2+d3 = \left\{ \begin{array}{ll} \frac{(v\,in(\theta)-VT)d1}{VT} , & \alpha < \theta < \beta \\ 0 & otherwise \end{array} \right\} \qquad (7)$$

$$d2 = \frac{VB}{Vo} d1 \qquad (8)$$

By applying balance C_B for half line period ,bus voltage V_B can be determined, the average current of C_B over a switching and half period are as follows

$$\langle iCB \rangle_{SW} = \frac{1}{2}\left[\frac{(v\,in(\theta)-VT)v\,in(\theta)}{L1VT} - \frac{VB}{L2}\right] \qquad (9)$$

Components Stress
The currents i_{L2} and i_{L1} pass through the diode D1 at the time interval d_1T_S but in the opposite direction i.e. the current passing through diode D2 is difference of the current between i_{L2} and i_{L1}. the current in switch S1 is only i_{L2} but not the superposition of both currents of inductor s. the current of diode D1 and S1 switch at interval d_1T_s are

$$i_{D2} = i_{L2} - i_{L1} \qquad (10)$$
$$i_{s1} = i_{L2} \qquad (11)$$

Direct Power Transfer
The interaction of power processing between both PFC and dc/dc cell under high and low conditions is given by

$$p_o(\Theta) = p_{o\_PFC}(\Theta) + p_{o\_DC/DC}(\Theta) \qquad (12)$$

Where $p_o(\Theta)$, $p_{o\_DC/DC}(\Theta)$ and $p_{o\_PFC}(\Theta)$ are instantaneous output power of converter, output power of dc/dc cell, output power of PFC cell.

IV. STIMULATION RESULTS

The performance of the 100W proposed circuit was verified by simulation and prototype. The Performance of the basic converter[7],[9] shown in Fig 1 (Boost Buck Boost single stage AC/DC converter)was simulated for intermediate bus voltage (V_B) , output voltage (V_O) under universal line operating conditions. These stimulated results are used for comparison with our proposed converter.Table-1 depicts the parameters used for the stimulation.
Fig.5 depicts the relationship of bus voltage (V_B) ,rms value of the line voltage and the inductance ratio M. It is noted that the intermediate bus voltage (V_B) is kept well below 120V even at high –line operating conditions. Taking the performance of the converter on bus voltage and efficiency into account, the inductance M is selected. Fig. 6 (a) and (b) illustrates the stimulation of intermediate bus voltage (V_B) , output voltage (V_O) of the IBoBuBo converter shown in Fig. 1. It is observed that the intermediate bus voltage is around 360V at high line operations and output is 100V. Stimulation results of the proposed converter for, output voltage (V_O) and intermediate bus voltage (V_B) are given in Fig. 7(a) and 7(b) respectively for high line input condition (270 Volts). Fig. 8 (a) and (b) shows the output voltage (V_O), intermediate bus voltage).

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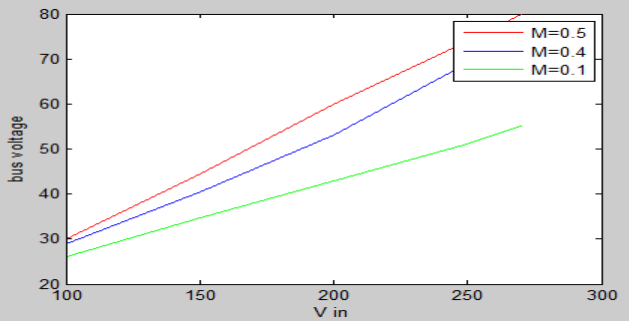

Fig. 5.Intermedite Bus Voltage at different inductance ratio

TABLE-I CIRCUIT PARAMATERS

Parameter	Value
Switching frequency (f_S)	20kHz
Line input voltage	90-270V/50Hz
Output voltage	19V
Output power	100W
Intermediate bus voltage (V_B)	<120
Inductance ratio M	0.432

Table-2 provides the intermediate bus voltage (V_B) and output voltage (V_o) for different load conditions (from full load to light load).It is observed that the output voltage is constant under different load conditions. The value of intermediate bus voltage (V_B) is varying depending on the load conditions. But is maintained well below 120V.

V. DISCUSSION

The proposed converter uses the technique of direct power transfer to improve the efficiency and also keeps the by using the concept of direct power transfer. Table-III depicts the comparative analysis of the basic converter [7],[9] and the proposed converter. The performance of both converters are tabulated in terms of intermediate bus voltage (V_B) , output
voltage (V_o), no of control switch, input voltage V_{rms}. Apart from the performance of reducing bus voltage the step down ratio and circuit complexity are less dependent on input and output 3conditions, and operating parameters. From the table.3 it can be seen that the proposed converter is able to achieve lowest bus voltage at high-line condition with low output voltage and simpler structure.

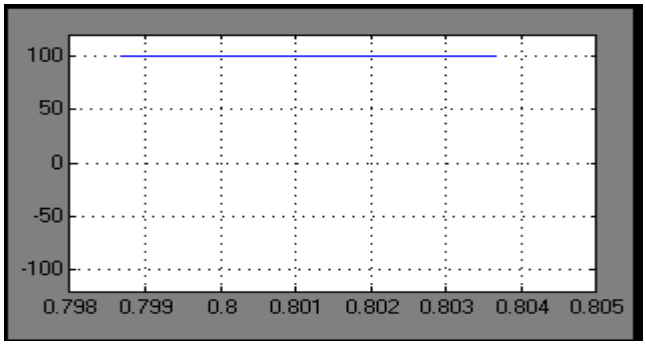

Fig. 6. (a) Stimulated Output Voltage for basic converter for input of 270 volts.

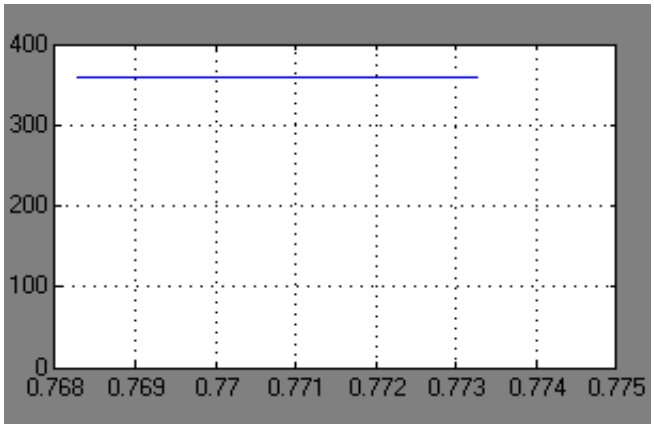

Fig. 6. (a) Stimulated bus Voltage for basic converter for input of 230 volts.

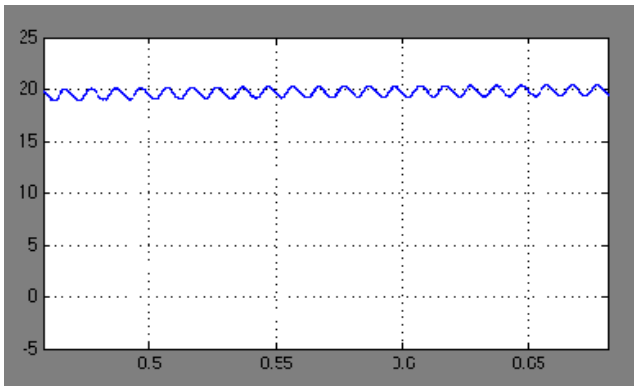

Fig. 7. (a) Stimulated Output Voltage 19 Vrms for input Of 270 Vrms for proposed converter

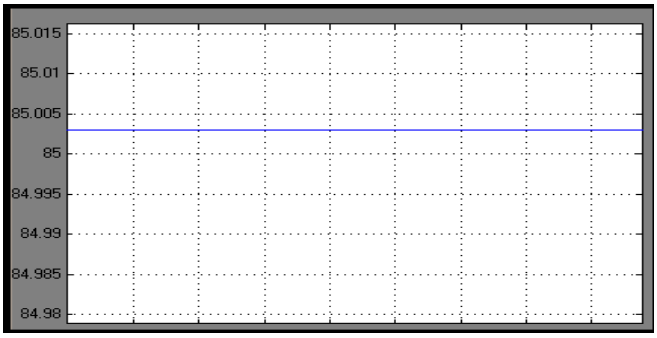

Fig. 7. (b) Stimulated Bus Voltage 85 V for input Of 270 Vrms

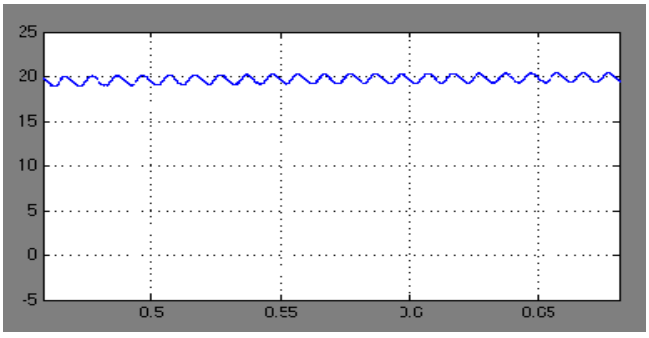

Fig. 8. (a) Stimulated Output Voltage 19 Vrms for input Of 90 Vrms for proposed converter

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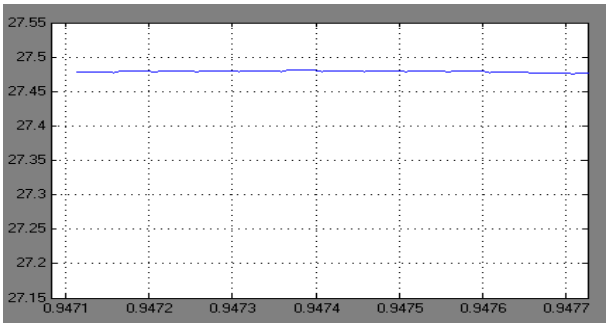

Fig. 8. (b) Stimulated Bus Voltage 27 V for input Of 90 Vrms for proposed converter

TABLE-II
VARIATION OF BUS VOLTAGE WITH OUTPUT POWER

Output Power	Bus Voltage	Output Voltage
20	45 V	19.5 V
40	57 V	19.5 V
60	65 V	19.5 V
80	77 V	19.5 V
100	84 V	19.5 V

TABLE III COMPARISON

	Input Voltage V_{rms}	Intermediate Bus Voltage (V_B)	Control Switch	Output Condition
Basic converter	90 ~270 V_{rms}	≤380	1	100V/100W
Proposed converter	90~270 V_{rms}	<120	1	19V/100W

Fig.9 Shows the experimental setup of the proposed converter

VI. EXPERIMENTAL RESULTS

To verify the theoretical analyses of the proposed converter a 100-W prototype is built in the laboratory for various applications as shown in Fig. 9. Under the conditions V_{in}=230V, V_o=19V, and P_o=100W, the experimental results are shown for the proposed converter. The results shows the voltage stresses on S_1 and intermediate bus voltage is reduced.

VII.CONCLUSION

The proposed integrated BuBuBo SS SS AC/DC Converter is verified by stimulation results and prototype. The intermediate bus voltage is kept well below 120V at all the input and output conditions is lower compared to other converters at both high and low conditions and also it is maintained for light load to full load conditions and is able to achieve efficiency about 89.7%.

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