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Design and Simulation of Energy-Efficient 8-Bit Input Buffer for NoC Router

Sanghapal D. Kamble, M.A.Gaikwad

Abstract- In NoC (Network on chip), the power consumption is major issue while designing. In NoC router, conventional input buffer consume more energy. The paper is focused on the energy-efficient design of 8-bit input buffers, which use the characteristic of transmission of data on NoC that has probability of transmitting a zero signal is more than that of transmitting a signal one. The design of energy efficient 8-bit input buffer reduces the power consumption by 48% and the chip area 29% with calculating the gates count as compared with conventional 8-bit input buffer by using 65 nm cmos technology in simulation.

Keywords: Network on chip, NoC Router, Input Buffer.

I. INTRODUCTION

In micro-processor design, the chip multi processing technology is mostly used for increasing the performance.[2] For on-chip communication, Network-on-chip is efficient solution. As increasing the number of processing cores, level two cache size and wire delay of chip, so a novel CMP architecture called as a tiled CMP is used to resolve these problems. In cores, the interconnection with high processing capability is more critical. For efficient interconnection between on chip processor cores, Network-on-Chip (NoC) is solution. As the process scaling down, more energy consumption by NoC will be more critical problem.[1] **N**oC architecture has two parts as a router and data link. The router is used to store and forward the data, and the data link transmits signals from one router to its neighbor. The router consist of three part: input buffer, arbiter, and crossbar. The delay of arbiter is not critical and its energy consumption is very small compared to input buffer, crossbar and data link, so it is ignored.[1] In NoC, most of the energy is consumed by input buffer and it has been found that input buffer consume about 79% power of NoC router[3]. The paper is focused on energy efficient 8-bit input buffer in NoC router which use the characteristic of transmission of data on NoC having the probability that transmitting the bit zero is more than transmitting the bit one. The design uses this characteristic because energy consumed by writing and reading zero is less than that of writing and reading the one. In simulation with 65 nm CMOS technology, the energy consumption of NoC is reduced more significantly and also it gives reduction in chip area by calculating the gates count and compare with conventional 8-bit input buffer.

II. RELATED WORK

2.1 NoC ROUTER

The important part of a tiled CMP is the NoC architecture has two parts: router and data link. The router can store and forward the data, and signals can be transmitted by the data link from one router to its neighbor.

There are three parts in router as input buffer, arbiter, and crossbar as shown in fig1. The input data is stored by input buffer temporarily and each direction hold one input buffer queue (In five directions as up, down, left, right, and home). It is easy to be decided the destination node of the request, so it can be decided the next hop when the input data enters input buffer. The input buffer gives the requests to arbiter and that allocates virtual channels to this requests and then generates grant signals to request initiators. The crossbar switches granted input requests which forwards the request data towards the data link, and then the request data is transmitted to the next hop router through data link. In NoC Router, input buffer consume one third of energy. As the conventional input buffer has extra energy consumption, which is a more critical problem. To reduce energy more efficiently, the design of energy efficient 8-bit input buffer for NoC router is proposed by using the eight 1-bit input buffer. The input buffer of 8-bit is most frequently used for NoC router as it gives the sufficient high speed with more efficiently reduction in energy consumption rather than more size of buffer. If the size of buffer is more, the energy consumption is more as memory is increased. The paper is focused on low power consumption, so energy efficient 8-bit input buffer is used which gives reduction in energy consumption more efficiently along with reduced chip area by calculating the gates count.

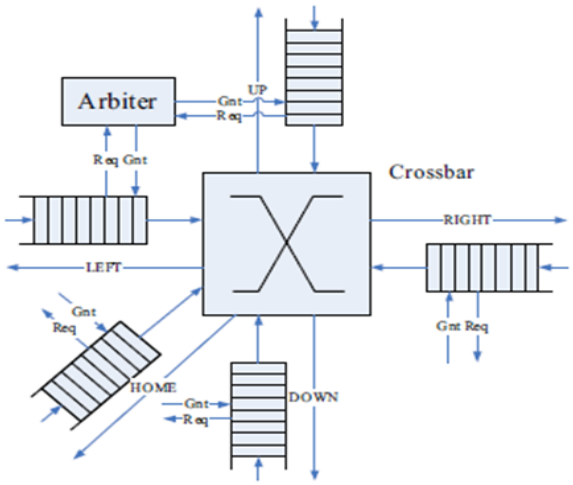

Fig.1 NoC router architecture

2.2 CHARACTERISTICS OF DATA ON NOC

The digital signals of requests and responses can have data, physical address, and control information like initiator ID and MSHR ID.

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* Correspondence Author
Sanghapal D. Kamble*, Student of M.Tech IV sem B.D. College of Engineering Wardha, India.
M.A.Gaikwad, Principal B.D. College of Engineering Wardha, India.

Some of them only contain physical address and control information, and some can have all three types of information. As the data is
of the biggest bit width, we can only consider the data information and which is much more than that of address information and control information. By analyzing these information, it can observe that the characteristics of these digital signals on NoC has the probability that the signals transmitted on NoC are zero is more than that of probability the signals are one. The energy consumption of input buffer reading and writing 0 is less than the energy consumption of input buffer reading and writing 1.[1]

2.3 INPUT BUFFER CIRCUIT

In conventional input buffer, differential bit line is used, which has extra energy consumption. In energy efficient input buffer, differential read bit line is reduced by single read bit line which reduces the energy consumption significantly. The conventional and energy efficient 1-bit input buffer circuit is as shown in fig. By using this 1-bit input buffer, we design 8-bit energy efficient input buffer. The energy consumption of transmitting 1-bit data from one node to the next will find in four parts: write data into the input buffer E_write; read data from the input buffer E_read. The write circuit of energy-efficient design is same as that of conventional. The read and write circuit for conventional and energy efficient is as shown in fig 2.

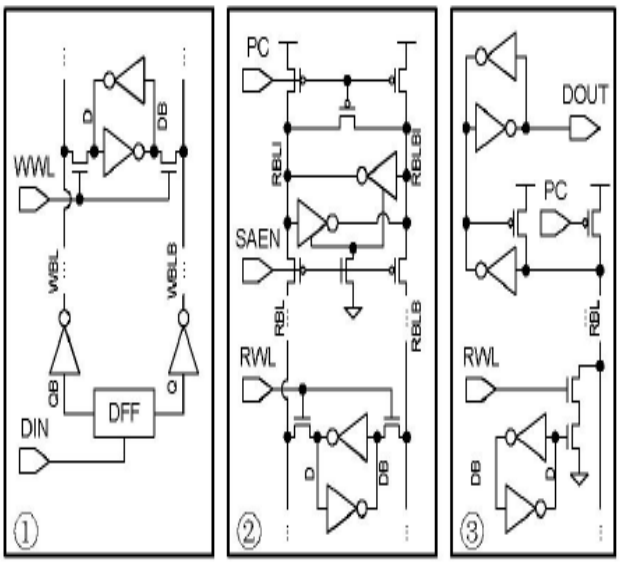

Fig.2 1. Write circuit input buffer 2. Read circuit of input buffer with Differential RBL 3. Read circuit of input buffer with Single- Ended RBL

2.4 WRITE INTO INPUT BUFFER

Static logic inverters drives the Differential write bit lines (WBL).The energy consumption of writing 1-bit data is

$$E_{write\_cv} = E_{write\_ze} = f\left(e_{w0}, e_{wl}, e_{wl}\right)$$

$$\text{Where } e_{w0} = \left(E_{wdec} + E_{wwl}\right)/W_{bit}\,; e_{wl} = E_{wbl} + E_{cc}\,.$$

And data width of the input buffer in bit is W_bit , the energy consumed by write address input flip flops and decoder is E_wdec; E_wwl is consumed during charging write word-line (WWL); by charging or discharging differential write-bit-lines energy consumed is E_wbl. (WBL); when the input data is different from the data stored in the bit cell, the energy consumed is E_cc. Because of the, The enabled input write address in one cycle will not be the same as its previous due to the characteristic of input buffer, so E_wdec and E_wwl will be counted for each write operation. E_cc is ignored as it is very small compared to the others.

2.5 READ FROM INPUT BUFFER

As in the conventional design, PC signal will pre-charge the differential RBL's at the rising edges of clock when the read function is enabled, and one of them will be discharged according to the stored data (D & DB) when read word-line (RWL) rises. After that, the voltage difference between RBL's is evaluated in the evaluation period and output data is generated. The energy consumption of reading 1-bit data is same due to differential RBL's, and no matter whatever the data transition is. The energy consumption of reading 1-bit data from conventional input buffer is as follows.

$$E_{read\_cv} = \left(E_{rdec} + E_{rwl\_cv} + E_{rpcg\_cv}\right)/W_{bit} + E_{rpc\_cv} + E_{rev}$$

Where E_rdec is the energy consumed by read address input flip-flops and decoder; E_rwl is the energy consumed by charging RWL; E_rpcg_cv is the energy consumed for generating pre-charge signal; E_pc_cv is consumed during the pre-charging of RBL's; E_rev is the energy consumed during evaluation is going on and generation of output data by the sense amplifier; The same reason for the write operation, E_rdec and E_rwl will be also counted for each read operation.

In Energy-efficient circuit, the differential read bit-lines (RBL) are reduced to single-bit. The pre-charged single-bit RBL will be discharged only when the stored data (D) is 1. So the energy consumption of reading 1-bit data from energy-efficient input buffer is

$$E_{read\_ze} = h\left(e_{r3}, E_{rdc}, E_{rpc}\right)$$

$$\text{Where } e_{r3} = \left(E_{rdec} + E_{rwl\_ze} + E_{rpcg\_ze}\right)/W_{bit}\,.$$

E_rwl_ze, E_rpcg_ze and E_rpc_ze all are have the same meaning as E_rwl_cv, E_rpcg_cv and E_rpc_cv, respectively as in write opration of input buffer, but the value are different. And E_dc is consumed during the discharging of RBL and generating the output data.

III.PROPOSED ENERGY EFFICIENT 8-BIT INPUT BUFFER

The proposed energy efficient 8-bit input buffer use data transmission characteristic of NoC having the probability of which the zero signals transmitted on NoC is bigger than the signals are one. The proposed energy efficient 8-bit input buffer for NoC router which consumes much less energy as compared to conventional 8-bit input buffer. The design of proposed energy efficient 8-Bit input buffer is as in fig3.

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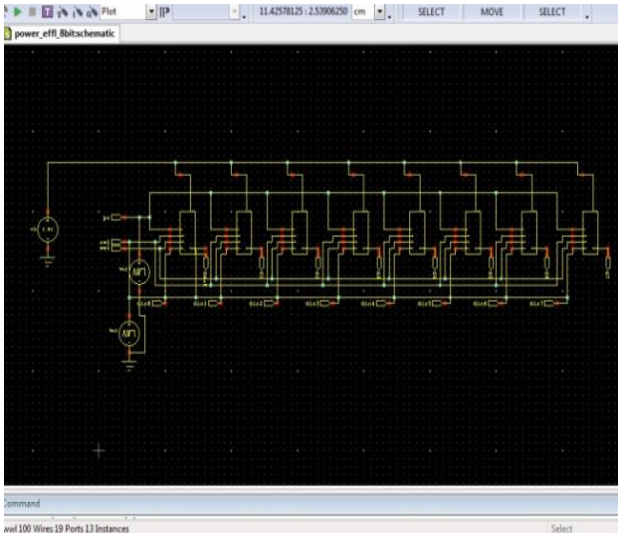

Fig.3 Circuit of energy efficient 8-bit input buffer

IV.SIMULATION AND SYNTHESIS

4.1 Simulation Result

Simulation refers to the verification of design, its fuction and performance. Fig. shows the simulation waveform of energy efficient 8-Bit input buffer. Simulation is performed on Tanner tool version 15.0 using 65 nm cmos process.

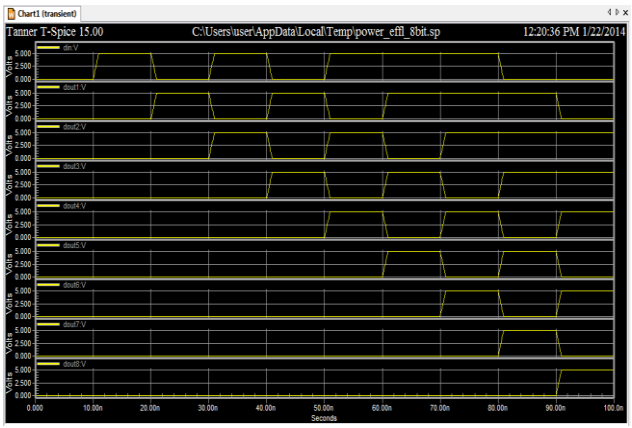

Fig.4 Simulation result of energy efficient 8-bit input buffer

4.2 Synthesis

4.2.1 Power Result

```
Measurement result summary
   avgpower      =    2.1004m
      From       =    0.000000
      To         =  100.0000n


Parsing                          0.03 seconds
Setup                            0.23 seconds
DC operating point               1.11 seconds
Transient Analysis               1.81 seconds
Overhead                         0.25 seconds
-----------------------------------------------
Total                            3.43 seconds
```

Fig.5 power result of energy efficient 8-bit input buffer

The power of energy efficient 8-bit input buffer is found as 2.1004 mW and for conventional 8-bit input buffer, it is 4.3875 mW using 65 nm Cmos technology in Tanner tool version 15.0. It gives near about 50 % of efficient reduction in power consumption. The comparison is as shown in fig.6.

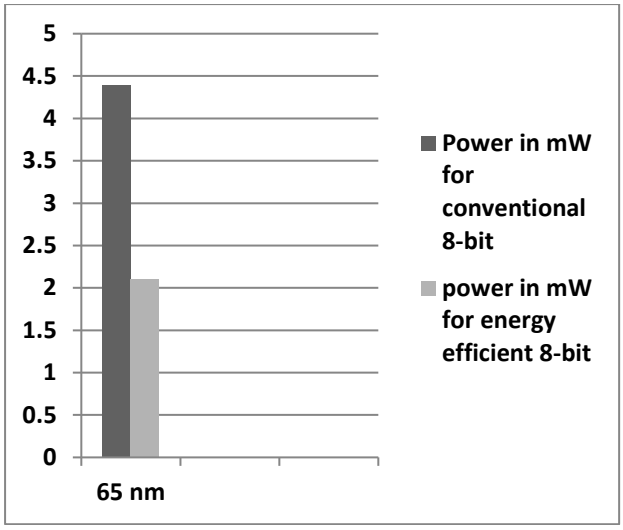

Fig.6 comparison of power in 8-bit input buffer

4.2.2 Gates Count

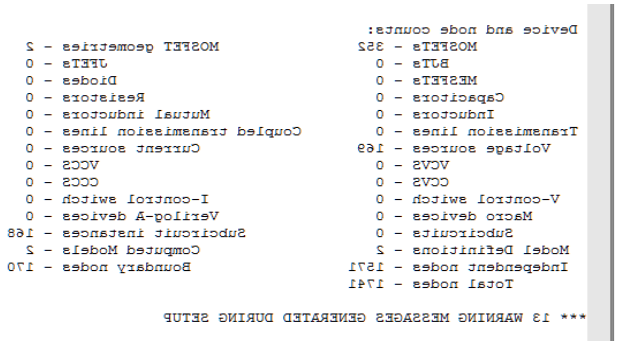

Fig.7 counting of gates in energy efficient 8-bit input buffer

The counting of gates for energy efficient 8-bit input buffer is 352 and for conventional 8-bit input buffer, it is 496 in 65 nm cmos technology. The counting of gates is used to find the chip area of 8-bit input buffer and 30 % of chip area is reduced efficiently. The comparison of 8-bit input buffer is as given in fig.8.

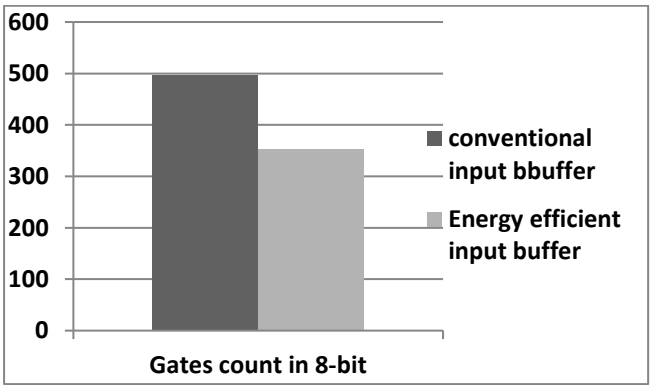

Fig.8 Comparison of gates count

V.CONCLUSION

In NoC Router, the energy consumption is major issue while designing. In NoC Router, one third of energy is consumed by the input buffer. In Conventional circuit of input buffer, energy is more consumed.

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So we have designed energy efficient 8-bit input buffer. It has been observed that the proposed design of energy efficient 8-bit input buffer reduces the energy consumption of NoC by 48% and also 29% of chip area with calculating the gates count by using 65 nm cmos technology as compared with conventional 8-bit input buffer.

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