International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-2 Issue-5, November 2013

Performance Evaluation of Logic Gates Based on Carbon Nanotube Field Effect Transistor

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Abstract- Carbon Nanotube Field Effect Transistors (CNFETs) are being widely studied as the possible alternatives to the conventional silicon-MOSFETs. In this paper we have successfully designed the CNFET-based digital logic gates and compared them with the existing CMOS technology based logic gates. The designs are modeled using 32-nm technology for both CNFET and CMOS technology, using Stanford University's MOSFET-like CNFET model [6] [7] and 32-nm BSIM PTM (Predictive Technology Model) respectively. For CNFET-based circuits, the compact SPICE model including non-idealities, which has been used for simulations, is the standard model that has been designed for unipolar MOSFET-like CNTFET devices, in which each transistor may have one or more Carbon Nanotubes (CNTs). HSPICE simulations have been performed on the logic gates designed using both these technologies and their output behaviors have been extensively studied at different supply voltages keeping the designs at room temperature. The performances are evaluated in terms of power, delay and PDP to show that it is possible to reduce the delay and the power consumption of the logic gates by replacing the CMOS transistors of the design with the emerging CNFETs.

Keywords- Carbon Nanotube (CNT), CNT Field Effect Transistor (CNFET), Logic gates. HSPICE

I.INTRODUCTION

According to Moore's law, the number of transistors of an integrated circuit increases exponentially by almost doubling every two years. Scaling of MOSFET technology has been carried continuously in order to meet the density and sustain the IC predicted by Moore's law. Since the year 2006, the gate length of a MOSFET device has entered the deep submicron/nano regime at 65-nm feature size. Today, 45-nm technology is a reality, and 32-nm has been predicted to be the feature size in the near future. As the physical gate length is reduced to below 65-nm, several device-level effects, such as large parametric variations and exponential increase in leakage current, have substantially affected the I-V characteristics of traditional MOSFETs. This results in major concerns for scaling down the feature size of these devices. To meet the challenges of nanoscale CMOS, a possible approach needs to be adopted which may consist of utilizing new circuit techniques together with alternative technologies to replace conventional silicon and the current MOSFET-based technology. The traditional MOSFETs can be replaced by either quantum-effect and single-electron solid-state devices or molecular electronic devices. Between these two categories, the most promising ones are the molecular electronic devices.

Revised Manuscript Received on 30 November 2013.
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Research work is going on in several such nanodevices, which include the Carbon Nanotube Field Effect Transistor (CNFET), the Resonant Tunneling Diode (RTD), the Single Electron Transistor (SET), and the Spin transistor (SPINFET). Carbon nanotube based technology develops the most promising devices among emerging technologies because it has most of the desired features. CNFETs are the novel devices that are expected to sustain the transistor scalability while increasing its performance. Recently, there have been tremendous advances in carbon nanotube (CNT) technology for nanoelectronics applications. CNFETs offer several advantages compared to silicon-based technology. Their principle of operation and structure both are almost similar to CMOS, and therefore the design infrastructure of this technology can be utilized, together with its fabrication process. The CNFET has been experimentally demonstrated to have excellent current capabilities, in literature. As one of the promising new transistors, CNFET avoids most of the fundamental limitations for silicon-based MOSFETs. With ultralong (~1 μm) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under low voltage bias to achieve the ultimate device performance. The quasi-1-D structure provides better electrostatic control over the channel region than 3-D devices (e.g., bulk CMOS) and 2-D devices (e.g., fully depleted SOI) structures. Efforts have been carried out in recent years on modeling semiconducting CNFET for digital logic applications, in order to evaluate the potential performance at the device level. In this paper, a performance assessment of CNFETs and their comparison against bulk nano CMOS are pursued at circuit level for delay and low power applications. The same gate length is utilized for the transistors made up of these two technologies. Different logic gates have been studied for different values of supply voltages at same temperature, to investigate the performance of this new technology. The circuit simulation uses a 32-nm CNFET HSPICE model that includes non-ideal effects for the CNFET and the 32-nm BSIM PTM (Predictive Technology Model) for the Si MOSFET. The Logic gates- Inverter, NAND, NOR, AND, OR, EX-OR and EX-NOR are investigated for performance under various operational conditions by considering power supply voltage and temperature.

II.CARBON NANOTUBE FIELD EFFECT TRANSISTORS

Carbon Nano Tubes (CNTs) are sheets of graphene rolled into tube. Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the single-walled carbon nanotubes can either be metallic or semiconducting.

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CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel. Therefore a semiconductor carbon nanotube seems to be appropriate to be used as the channel of field effect transistors. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel. By using appropriate diameter suitable threshold voltage for CNFET can be achieved. The threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT and can be expressed as:

$$V_{TH} = \frac{0.42}{D_{CNT}(nm)} \qquad (1)$$

For a CNT with *(n, m)* as chirality and *a* as lattice (that is carbon to carbon atom distance) the diameter is :

$$D_{CNT} = \frac{a\sqrt{n^2+mn+m^2}}{\pi} \quad (2)$$

As mentioned above, CNTs are used in CNFETs as channel and depending on the connections between source and drain with channel (CNTs) there are two main CNFETs. It works on the principle of direct tunnelling through a Schottky barrier at the source–channel junction; therefore, these transistors are called Schottky Barrier CNFET (SB-CNFET). SB-CNFET shows ambipolar behavior and constrain usage of these transistors in conventional CMOS-like logic families. Schottky barrier restricts the transconductance in the ON state, and thus I_{on}/I_{off} ratio becomes rather low. Second device is MOSFET-like CNFET which is doped in un-gated portions and has similar behaviour to CMOS transistors and it presents unipolar behaviour. The semiconductor-semiconductor junction will eliminate schottky barrier and therefore there is higher ON current unlike SB-CNFETs. Other advantages of MOSFET-like CNFETs are high on- off ratio and their scalability compared to their schottky barrier counterparts. In this paper we utilized MOSFET-like CNFETs for designing the logic gates.

III.SPICE COMPATIBLE MODEL OF CNFET

Fig. 1 is a theoretical illustration of a carbon nanotube FET structure. The structure resembles that of a MOSFET, but the nanotube is the channel for conduction in this case.

The study in this paper uses MOSFET-like CNFET model whose schematic diagram is shown in the above figure. The theoretical analysis of this model is described in brief, as follows. We assume near-ballistic transport and contacts in this work, i.e. $eV_{DS} \approx \mu_d - \mu_s$,so μ_s remains almost constant in the source-channel region and μ_d remains almost constant in the channel-drain region.

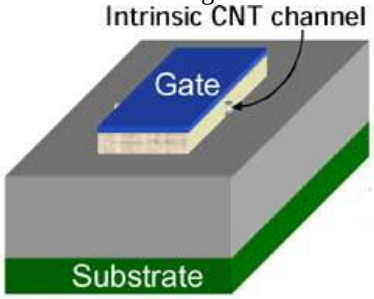

Fig. 1: MOSFET-like CNFET structure

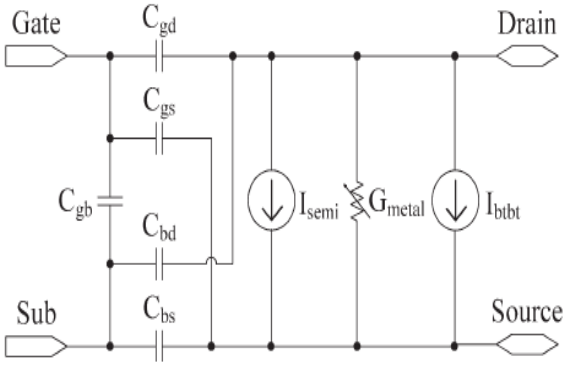

Fig.2: Equivalent structure of MOSFET-like CNFET

We consider three current sources in this CNTFET model: (1) the thermionic current contributed by the semiconducting sub-bands (I_{semi}) with the classical band theory, (2) the current contributed by the metallic sub-bands (I_{metal}), and (3) the leakage current (I_{btbt}) caused by the band to band tunneling mechanism through the semiconducting sub-bands.

A. Current and Capacitance Expressions

The thermionic current contributed by the semi conducting sub-bands is given by,

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = \frac{4e^2}{h}\sum_{\substack{k_m \\ m=1}}^{M} T_m \cdot \left[V_{ch,DS} + \frac{kT}{e} ln\left(\frac{1+e^{(E_{m,0}-\Delta\varphi_B)/kT}}{1+e^{(E_{m,0}-\Delta\varphi_B+eV_{ch,DS})/kT}}\right)\right] \quad \ldots(3)$$

$V_{ch,DS}$ and $V_{ch,GS}$ denote the Fermi potential differences near source side within the channel, e is the unit electronic charge, $\Delta\varphi_B$ is the channel surface potential change with gate/drain bias, T_m is the transmission probability, k is the Boltzmann constant and T is the temperature in Kelvin and $E_{m,0}$ is the half band gap of the m_{th} sub-band.

For metallic sub-bands of metallic nanotubes, the current I_{metal} includes both the electron current and the hole current,

$$I_{metal} = 2(1-m_0)T_{metal}\sum_{\substack{k_l \\ l=1}}^{L}\left[J_{ele\_0,1} + J_{hole\_0,1}\right] \quad \ldots(4)$$

$$J_{ele\_0,1} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\left(f_{FD}(E_{0,1}-\Delta\varphi_B) - f_{FD}(E_{0,1}+eV_{ch,DS}-\Delta\varphi_B)\right) \quad \ldots(5)$$

$$J_{hole\_0,1} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\left(f_{FD}(-E_{0,1}-\Delta\varphi_B) - f_{FD}(-E_{0,1}+eV_{ch,DS}-\Delta\varphi_B)\right) \quad \ldots(6)$$

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$f_{FD}(E)$ is the Fermi-Dirac distribution function $f_{FD}(E) = \frac{1}{1+e^{E/kT}}$ and the transmission probability T_{metal} is given by,

$$T_{metal} = \frac{\lambda_{ap}\lambda_{op}}{\lambda_{ap}\lambda_{op} + (\lambda_{ap}+\lambda_{op}).L_g} \quad \ldots(7)$$

where L_g is the channel length , λ_{op} (~ 15 nm) is the optical phonon scattering MFP and λ_{ap} (~ 500 nm) is the acoustic phonon scattering MFP.

In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling current from drain to source becomes significant. We include a voltage controlled current source I_{btbt} in the device model in order to evaluate the device sub-threshold behavior and the static power consumption.

$$I_{btbt} = \frac{4e}{h} kT \sum_{\substack{k_m \\ m=1}}^{M} T_{btbt} ln\left[\left(\frac{1+e^{(eV_{ch,DS}-E_{m,0}-E_f)/kT}}{1+e^{(E_{m,0}-E_f)/kT}}\right)\right] .\frac{max\left((eV_{ch,DS}-2E_{m,0}),0\right)}{eV_{ch,DS}-2E_{m,0}} \quad \ldots(8)$$

To model the intrinsic ac response of CNFET device, we use a controlled transcapacitance array among the four electrodes (G, S, D, B) with the Meyer capacitor model, thereby the equations for capacitance calculation are given as follows.

$$C_{bd} = C_{gd}\frac{C_{sub}}{C_{ox}} \quad \ldots(9)$$

$$C_{bs} = C_{gs}\frac{C_{sub}}{C_{ox}} \quad \ldots(10)$$

$$C_{gd} = \frac{L_g C_{ox}(C_{Qs}+\beta C_c)}{C_{tot}+C_{Qs}+C_{Qd}} \quad \ldots(11)$$

$$C_{gs} = \frac{L_g C_{ox}(C_{Qs}+(1-\beta C_c))}{C_{tot}+C_{Qs}+C_{Qd}} \quad \ldots(12)$$

$$C_{bg} = C_{gb} = \frac{L_g C_{sub} C_{ox}}{C_{tot}+C_{Qs}+C_{Qd}} \quad \ldots(13)$$

C_{tot} is the total electrostatic coupling capacitance per unit length between channel and other electrodes, C_{Qs} and C_{Qd} as the quantum capacitance due to the carriers from source (+k branch) and drain (−k branch), respectively.

IV.I-V CHARACTERISTICS OF CNFET

The circuit compatible model of MOSFET-like CNFET shown in fig 2 has been successfully implemented in HSPICE simulator. The p-type and n-type CNFETs are modeled and simulated in HSPICE. The series of I-V characteristics of both types of CNFETs are obtained for 1.5nm diameter CNT at room temperature (300K) and are shown in fig. 3 and fig. 4 respectively. In order to demonstrate the versatility of this model, we employed it to design basic logic gates. We see that CNFETs behavior is very similar to that of conventional MOSFET's.

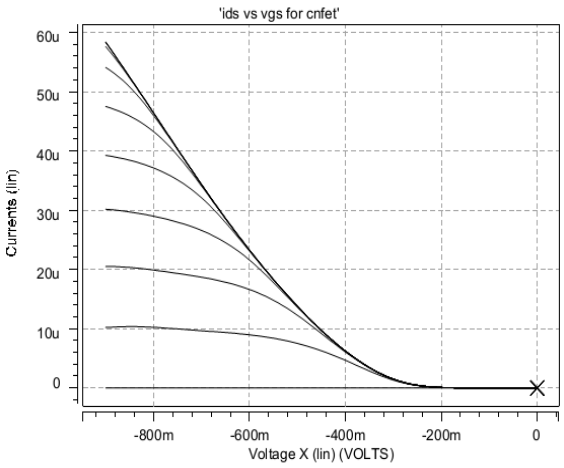

Fig. 3: PCNFET Characteristics

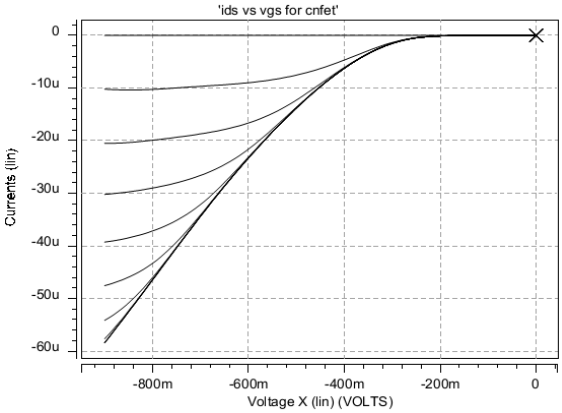

Fig. 4: NCNFET Characteristics

This model is designed for unipolar MOSFET like CNTFET devices, where each device may have one or more carbon nanotubes. 32nm technology with (19,0) semiconducting with 1.5nm diameter CNT is used . The supply given is 0.9V and gate and drain voltage can be varied up to supply voltage. Fig. 3 & 4 show current voltage characteristics of CNT model. Gate voltage starting from zero is varied upto supply voltage with a variation of 0.01 x supply. Different curves for various value of V_{dd} with a variation of 0.1 x supply are shown

V. SIMULATION RESULTS OF CNFET AND CMOS BASED LOGIC GATES

The inverter is the fundamental logic gate for digital circuit design. A CNFET-based inverter circuit is shown in Fig 5(a).. The pull-up network (PUN) is implemented using p-type CNFET and the pull-down network (PDN) is implemented using n-type CNFET. They are coupled together in series between a high supply voltage (V_{DD}) and ground, as shown in figure. The first CNFET which is biased to conduct holes, functions as a driver transistor with its gate providing an inverter input V_{IN}.

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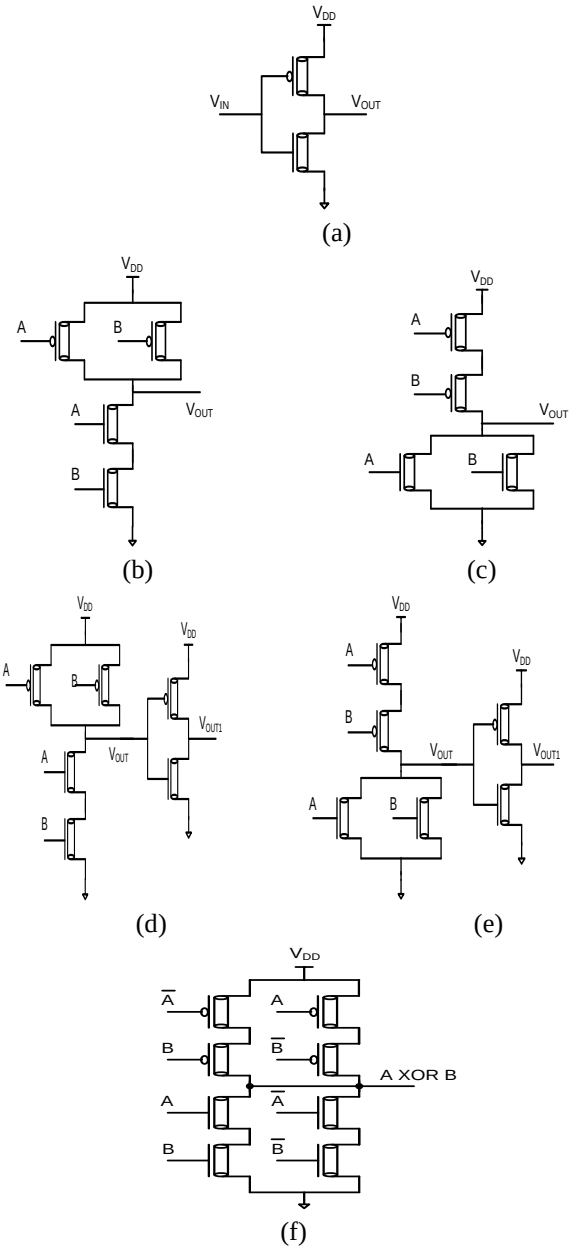
The second transistor which is biased to conduct electrons, functions to facilitate an active load with its gate coupled to a supply V_{GG} for appropriately biasing it, so that the output provides suitable low and high values, when V_{IN} is high and low respectively.

Fig. 5(b) and (c) show the implementation of two-input NAND and two-input NOR logic, respectively, comprising of CNFETs as discussed herein, in accordance with some embodiments. These comprise of driver CNFETs coupled together in parallel between a high supply reference (V_{DD}) and a series active load transistors, which is coupled to a low supply reference ground, as shown. The AND and OR gates can be designed by simply putting an inverter in front of NAND and NOR gates respectively. These are shown in fig 5(e) and (e) respectively



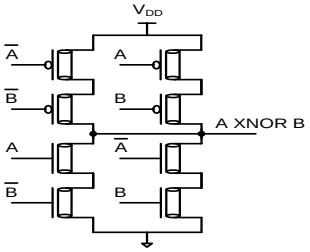


Fig. 6: (a) CNFET Inverter (b) NAND Gate (c) NOR Gate (d) AND Gate (e) OR Gate (f) EX-OR Gate (g) EX-NOR Gate

The Exclusive-OR (EX-OR) and Exclusive-NOR (EX-NOR) gates, designed using CNFET technology are shown in fig. The first part consists solely of complementary pull-up PCNFET network while the second part consists of pull-down NCNFET network. This technique is popular and produces results that are widely accepted one, and uses lesser number of CNFETs as compared to the EX-OR and EX-NOR gates produced using NAND gates.

To compare the performance of the MOSFET and CNFET, the P-transistor/ N-transistor ratio of the MOSFET and CNFET gates should be established. In general for Si CMOS, a PMOS/NMOS ratio of 2 or 3 is used because the NMOS mobility is about 2 or 3 times higher than for the PMOS transistor. A 3:1 (PMOS:NMOS) ratio is used in this simulation, especially for inverter, because at this value, the voltage transfer characteristic (VTC) of the MOSFET inverter shows a more symmetrical shape for the 32-nm technology. However for CNFETs, a PCNFET/NCNFET ratio of 1 is used because the NCNFET and PCNFET have the same current driving capabilities with same transistor geometry. In CMOS design, the width of the MOSFET is adjusted to change the PMOS/NMOS ratio. However in a CNFET, the number of tubes is the design parameter for changing the current and resistance. The designs are simulated in SPICE environment. The CNFETs with diameter of 1.5 nm, show very good results. The Voltage Transfer Characteristic (VTC) curves of the 32-nm MOSFET and 32-nm CNFET are shown in Fig. 6, for minimum size MOSFET and CNFET inverters' functionality. There is a stiff transition between two states with a threshold voltage equal to half the power supply, i.e., the curve is symmetric and the logic threshold voltage (V_{inv}) is in the center ($V_{inv}=V_{out}=V_{in}=V_{DD}/2$). Even though the amount of current of a CNFET is smaller than for the minimum sized MOSFET at 32nm, the CNFET can have a steeper curve in the transition region (due to the higher gain than the MOSFET).

The transient simulation results of the all the above mentioned CNFET gates at 0.9V supply are shown in Fig. 7(a)-(g) The waveforms indicate that there is no logic degradation in both the logic 0 and logic 1 states. The propagation delay through the gate, dynamic power dissipation, and the power delay product (PDP) are calculated for each of these gates

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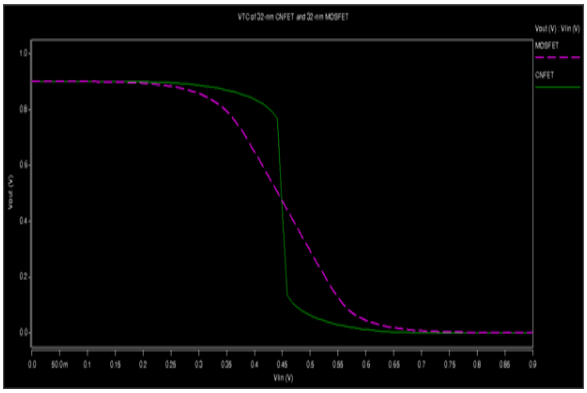
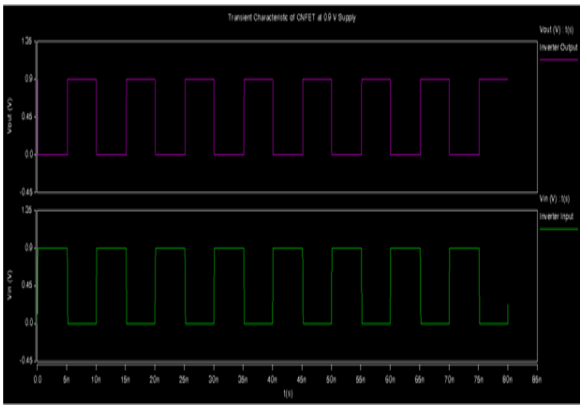
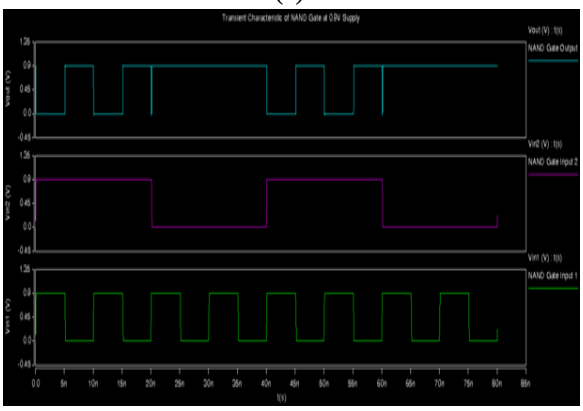


Fig. 6: VTC of CNFET and CMOS Inverter

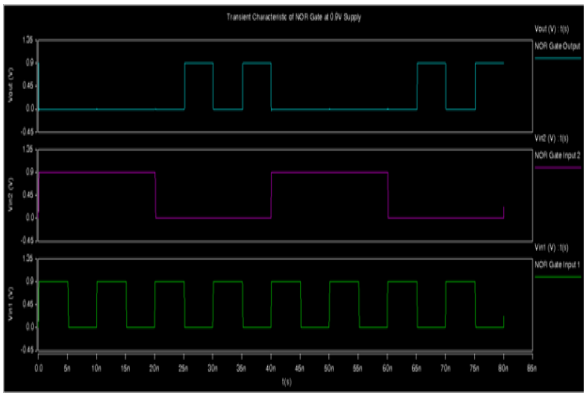
for different value of supply voltages 0.9V, 0.7V and 0.5V at room temperature. Table I, 2 and 3 show the performances of the gates designed using both of these technologies at 0.9V, 0.7V and 0.5V respectively. These tables clearly indicate that the performance parameters of CNFET-based logic gates are better than those of CMOS-based logic gates.



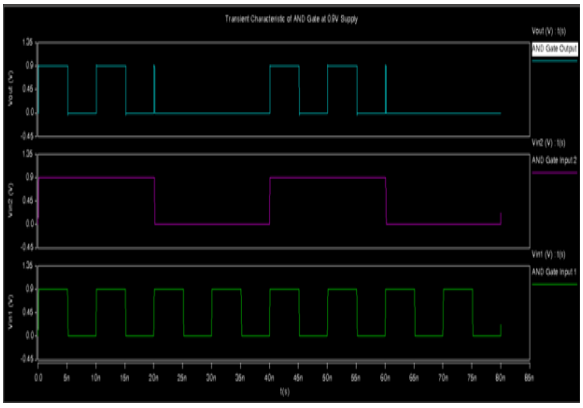
(a)



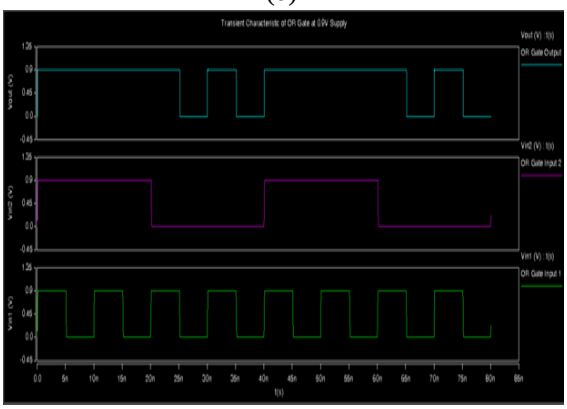
(b)



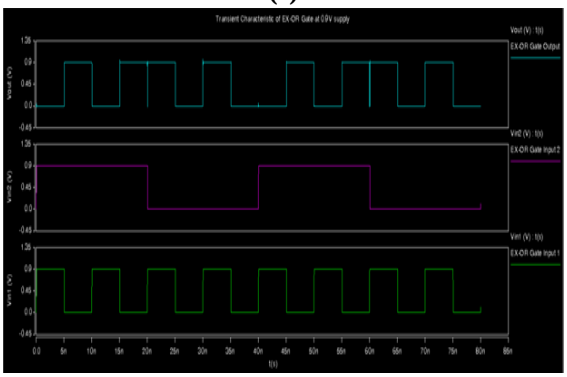
(c)



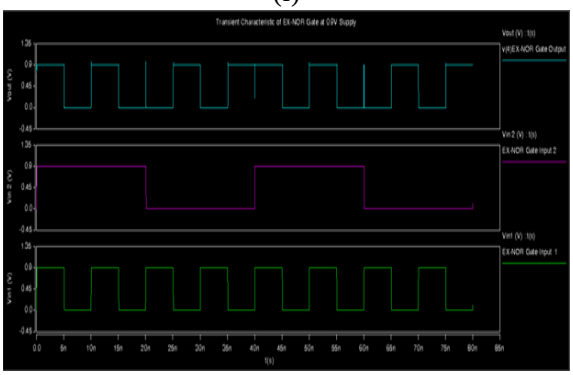
(d)



(e)



(f)



(g)

Fig. 7: Transient Characteristics of (a) Inverter (b) NAND Gate (c) NOR Gate (d) AND Gate (e) OR Gate (f) EX-OR Gate (g) EX-NOR Gate

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Table 1: Comparative performance of transient analysis of CNFET and CMOS logic gates at V_{DD}=0.9V

Logic Gates	P (W)	D (s)	PDP (J)	P (W)	D (s)	PDP (J)
	CNFET			CMOS		
Inverter	3.44E-08	2.46E-12	8.46E-20	7.37E-08	1.65E-12	1.22E-19
NAND Gate	1.13E-08	4.60E-12	5.20E-20	1.04E-07	1.57E-12	1.63E-19
NOR Gate	1.53E-08	2.98E-12	4.56E-20	1.69E-07	1.42E-12	2.40E-19
AND Gate	1.71E-08	1.67E-12	2.86E-20	2.41E-07	5.91E-12	1.42E-18
OR Gate	1.39E-08	3.12E-12	4.34E-20	1.41E-07	9.41E-12	1.33E-18
EX-OR Gate	6.32E-08	6.60E-12	4.17E-19	3.75E-07	1.78E-11	6.68E-18
EX-NOR Gate	6.40E-08	5.49E-12	3.51E-19	3.76E-07	1.77E-11	6.66E-18

Table 2: Comparative performance of transient analysis of CNFET and CMOS logic gates at V_{DD}=0.7V

Logic Gates	P (W)	D (s)	PDP (J)	P (W)	D (s)	PDP (J)
	CNFET			CMOS		
Inverter	7.98E-09	2.79E-12	2.23E-20	1.84E-08	9.55E-12	1.76E-19
NAND Gate	2.63E-09	1.80E-11	4.73E-20	3.88E-08	1.38E-11	5.35E-19
NOR Gate	3.90E-09	4.22E-12	1.65E-20	3.16E-08	8.82E-12	2.79E-19
AND Gate	5.89E-09	4.70E-12	2.77E-20	8.46E-08	2.13E-11	1.80E-18
OR Gate	5.89E-09	2.90E-12	1.71E-20	6.00E-08	2.66E-11	1.60E-18
EX-OR Gate	7.02E-08	3.10E-13	2.18E-20	1.41E-07	3.62E-11	5.10E-18
EX-NOR Gate	1.62E-08	8.60E-13	1.39E-20	1.51E-07	3.62E-11	5.47E-18

Table 3: Comparative performance of transient analysis of CNFET and CMOS logic gates at V_{DD}=0.5V

Logic Gates	P (W)	D (s)	PDP (J)	P (W)	D (s)	PDP (J)
	CNFET			CMOS		
Inverter	1.13E-09	4.82E-12	5.45E-21	8.75E-09	3.78E-11	3.31E-19
NAND Gate	5.20E-10	5.69E-12	2.96E-21	1.90E-08	4.44E-11	8.44E-19
NOR Gate	5.10E-10	7.44E-12	3.79E-21	1.63E-08	3.70E-11	6.03E-19
AND Gate	1.35E-09	9.24E-12	1.25E-20	3.21E-08	5.05E-11	1.62E-18
OR Gate	1.08E-09	5.85E-12	6.32E-21	2.82E-08	6.22E-11	1.75E-18
EX-OR Gate	3.17E-09	8.24E-12	2.61E-20	6.22E-08	9.25E-11	5.75E-18
EX-NOR Gate	3.27E-09	8.13E-12	2.66E-20	6.21E-08	9.61E-11	5.97E-18

VI. CONCLUSION

In this paper we have compared the CNFET-based logic gates with the CMOS-based logic gates, both simulated in 32-nm technology in HSPICE software using Stanford University's CNFET HSPICE Model and BSIM PTM Model respectively. The simulations are carried out at room temperature for different values of supply voltages i.e. 0.9V, 0.7V and 0.5V, and performances are studied in terms of power, delay and PDP. The CNFET-based logic gates show far better results as compared to those of CMOS-based logic gates

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