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Simulation and Optimization of a Partial Gate All Around Cylindrical Tunnel FET

Kanjalochan Jena, Brinda Bhowmick, Srimanta Baishya

Abstract*: This paper represents a partial gate all around cylindrical tunnel FET. In this device gate is applied over half of the channel and the entire source and hetero-gate dielectric is used. A compact electrostatic model for potential of the proposed device is formulated using central difference technique considering 16x16 matrix. Optimization has been done for various gate materials since electrical parameters like OFF current, ON current, threshold voltage, vertical electric field are strong function of gate work function. Furthermore, the proposed device is also compared with cuboidal partially gate-all-around 3D structure for gate oxide scaling. The results of the potential model show good agreement with the simulated data obtained from TCAD simulation.

Index Terms*: Band-to-band tunneling, partial gate all around, work function.

I. INTRODUCTION

Nowadays, CMOS technology is currently the driving technology of the whole microelectronics industry [1]-[2]. In 1994 the Semiconductor Industry Association (SIA) organized a workshop in Boulder, Colorado that resulted the National Technology Roadmap for Semiconductors (NTRS) [3]. This roadmap was updated once again in 1997 and 1999 through a series of meetings with relevant industries[4]. Due to scaling the CMOS devices, various short channel effects are coming into picture [5]. The tunnel FET ON current is limited by interband quantum mechanical tunneling [6]-[7]. One of the major disadvantages of Tunnel FET is its on current limitation. To overcome such major problems it is much appropriate to use Group III–V materials [8] so that tunneling current can be increased upto NTRS requirements. Various materials like GaAs, Si-Ge, InAs etc are the replacements for Silicon [9]-[10]. InAs is one of the promising candidates. The electron mobility in InAs is much higher than Si due to lower electron effective mass ($0.023m_0$). At the instance, high electric field is applied, light electrons experience "Ballistic Transport" in InAs. Thus, their instantaneous velocity can be higher than that in Si [11]. At the same time, quantum confinement effects can no longer be neglected [12]. Tunnel FETs are most promising candidates for overcoming the short channel effects [13]-[14]. Moreover, sub KT/Q subthreshold swing is possible in Tunnel FET where, as in case of CMOS, it is dependent on room temperature [15]. Tunnel FETs are band-to-band tunneling devices. The main disadvantage of tunnel FET is its low ON current.

In this paper, we propose a partial gate all around cylindrical structure, in contrast to gate all around cuboidal structure [16], where the gate is placed over the entire source and half of the channel. In As is applied over the whole source and channel. Gate oxide thickness scaling effect on the proposed device and cuboidal structure is compared. In case of cuboidal structure, the corner components of current reflect a lower threshold voltage and higher off current. Furthermore, the effect of gate work function on the electrical parameters like OFF current, threshold voltage (V_t), vertical electric field, and subthreshold swing (SS) is also observed.

II. DEVICE STRUCTURE

The proposed device is a 3D partial gate all around (PGAA) cylindrical TFET as shown in Fig. 1. Hetero gate oxide is used. On the source side high-K gate oxide HFO_2 and on the drain side low-K gate oxide SiO_2 is applied. The Gate covers the entire source and the half of the channel length, i.e., the device is a partial gate all around TFET where InAs channel and source is used. Band-to-band tunneling model is used. Also, band gap narrowing is activated. The doping concentrations in the source, channel, and drain regions are 10^{21}, 10^{16}, 10^{18} cm^{-3}, respectively.

III. MODEL FOR POTENTIAL DISTRIBUTION

Due to azimuthal symmetry, Poisson's equation is restricted to two dimensions only and the Poisson's equation is [17]

$$\frac{\partial^2 V}{\partial r^2}+\frac{1}{r}\frac{\partial^2 V}{\partial r^2}+\frac{\partial^2 V}{\partial z^2}=-\frac{\rho}{\varepsilon} \qquad (1)$$

where ρ is the charge density.

This above equation can be solved with a finite difference method, the most commonly used discretization scheme is the five point centered difference formula [18].

Considering the second order central differences for both the derivatives,

$$\frac{V_{i+1,j}-2V_{i,j}+V_{i-1,j}}{\nabla r^2}+\frac{V_{i,j+1}-2V_{i,j}+V_{i,j-1}}{\nabla z^2}+\frac{1}{r_i}\frac{V_{i+1,j}-V_{i-1,j}}{2\nabla r}=-\frac{\rho(r_i,z_j)}{\varepsilon} \qquad (2)$$

where r_i =idr, i=0,1,.....m

Z_j =c+jdz, j=0,1,.....n

m and n are the grid spacing along r and z directions.

The corresponding boundary conditions are

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* Correspondence Author
K.Jena, Research scholar in ECE Dept., NIT Silchar, Silchar, India.
Asst. Prof. B.Bhowmick , ECE Dept., NIT Silchar, Silchar, India.
Prof. S. Baishya, ECE Dept., NIT Silchar, Silchar, India.

$$V(r,0) = -\frac{\phi_S}{q}$$

$$V(r,L) = V_{DS} - \frac{\phi_D}{q},$$

$$\frac{\partial V(0,z)}{\partial r} = 0$$

$$V(b,z) = \phi_G - \psi_S(z)$$

$$\psi_S(z) = \psi_S(b,z) \qquad (3)$$

ϕ_S , ϕ_D , and ϕ_G are source drain and gate work functions, respectively. Ψs (Z) is the surface potential, L is the channel length, b is the radius.

Here we have considered 16X16 matrix, the potential distribution can be determined with some known charge density and applying the Gauss-Seidel iteration technique [17].

In this system we can determine charge density considering Dirac delta function in cylindrical coordinate δ(.)/r, with assumed electron concentration n and it signifies that carriers were taken into account by means of a sheet charge distributed uniformly over the surface.

$$\rho = \frac{qn}{2\pi}\frac{\delta(r-b)}{b} \qquad (4)$$

IV. RESULT AND DISCUSSION

Simulation is carried out using TCAD tools [19]. The proposed partial gate all around cylindrical TFET is shown in Fig. 1. The interface property of high-k oxide is better with metal gate [20]. Also, various metals such as silver, gold, cobalt, nickel, platinum, tantalum, and titanium are used as gate materials. The threshold voltage is a strong function of metal gate work function. It is observed that for titanium and tantalum better on current and off current is obtained in Fig. 2. With the increase of work function OFF current and ON current decreases significantly and but threshold voltage (Vt) is higher [21]. Variation of vertical electric field along the channel of the device is observed for various metal gates, in the Fig.3. With the increasing work function the vertical electric field decreases. This shows that with increasing work function tunneling at the source tunnel junction will decrease and results in reduced on and off current. Moreover, a cuboidal 3D tunnel FET with gate full source and half channel is compared with proposed device. The presence of corner effect is dominant in Cuboidal structure by observing the output characteristics in Fig. 4. In the range 0.4V to 0.6V V_{GS}, the drain current in cuboidal structure is more than that of cylindrical TFET and it is the significance of reduced miller capacitance effect.

With the increase of gate oxide thickness the off current degrades, but on current remains almost same. Also, the subthreshold swing (SS) is improved in the scaled device because InAs in source and channel provides low band gap as well as reduced density of states [8]. From Fig. 4, we surmise that low charge density due to the non-negligible component of electric field could influence the drain current, but at high oxide thickness corner effects are suppressed. This is because Vt depends on tox [22]. A 'hump' like characteristics is observed in I_D-V_{GS} curve for cuboidal structure that causes serious technological problem. Electrostatic potential is plotted in Fig. 5, the source side has highest potential. The table I shows the SS values at various gate oxide thickness. Excellent agreement has been achieved for potential distribution at different oxide layer thickness as shown. The center potential of the device increases with the scaling of oxide thickness, therefore immunity towards short channel effect is reduced.

TABLE I. Comparison of PGAA Cylindrical and Cuboidal TFET

t_{ox} (nm)	SS (mV/dec)	
	PGAA Cylindrical	PGAA Cuboidal
1	42	56
2	52	57.6
3	55	59

TABLE II. Comparison of electrical parameters for various metal gates

Type of metal	SS(mV/dec)	OFF current	ON current	V_t (V)
Pt	42	10^{-18}	10^{-4}	0.2
Au	45.8	$9.2X10^{-17}$	$3X10^{-3}$	0.186
Ni	49.07	10^{-17}	$4X10^{-3}$	0.14
Co	50.84	$9.67X10^{-17}$	$6.2X10^{-3}$	0.13
Ag	51	10^{-16}	$7x10^{-3}$	0.09
Cu	55.45	$8.86X10^{-16}$	$7.9X10^{-3}$	-0.2
Ta	56	$8.1x10^{-16}$	$8.1X10^{-3}$	-0.25
Ti	55	$7.8X10^{-16}$	$8.7X10^{-3}$	-0.36

In case of 3D Tunnel FET the dominant component of C_{gg} is the Gate to source capacitance. During the off state V_{GS}=0, the capacitances are negligibly small. But with increasing V_{GS} the capacitive effect increases linearly upto near about 0.5 V, in Fig. 6. This is due to the fact that upto 0.5V V_{GS} the channel charge increases after that it saturates and to maintain the charge level almost constant C_{gg} slightly decreases with V_{GS}. The potential function along the channel length is plotted. The entire gate capacitance is supplied from the gate to source capacitance and drain to source capacitance is very less. The TFET operation in digital circuit mainly depends on miller capacitance and this capacitance is dependent on C_{gd}. But in this PGAA TFET the effect of C_{gd} is negligible. Hence better performance can be obtained.

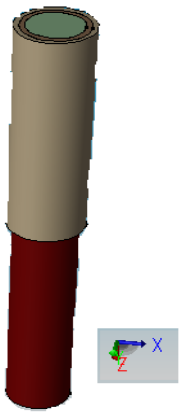

Fig. 1 Partially gate all around Tunnel FET

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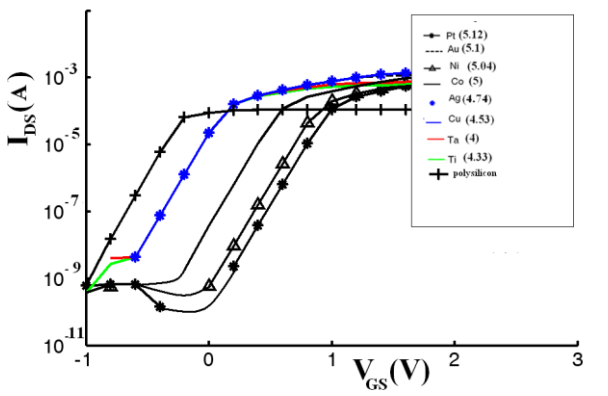

Fig. 2 I_D-V_{GS} characteristics of metal and polysilicon gate material in PGAA TFET

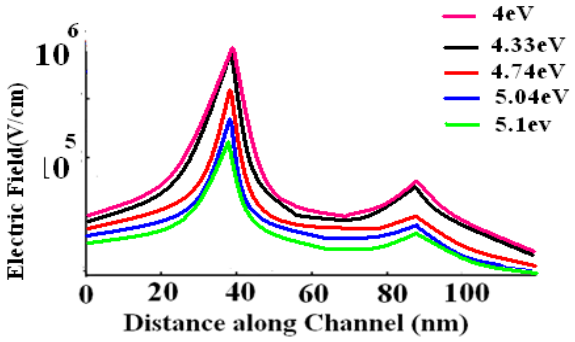

Fig. 3 Variation of electric field along channel length

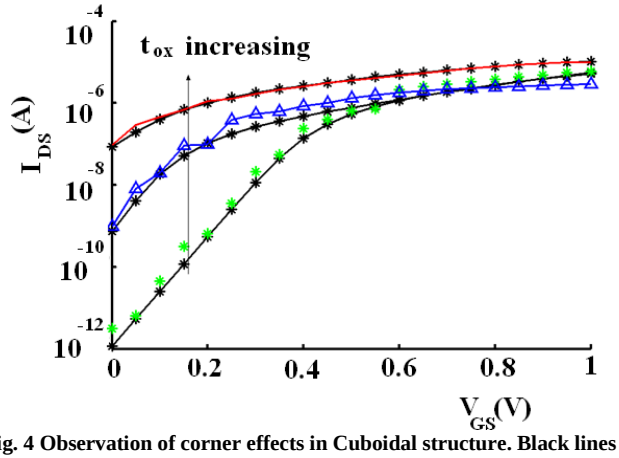

Fig. 4 Observation of corner effects in Cuboidal structure. Black lines indicate the cylindrical TFET and coloured figure indicate cuboidal structure for various oxide thickness.

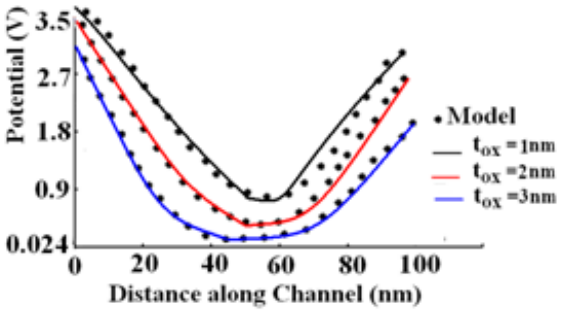

Fig. 5 Potential variation along the channel length for V_{GS}= 1V, at V_{DS}=0V.

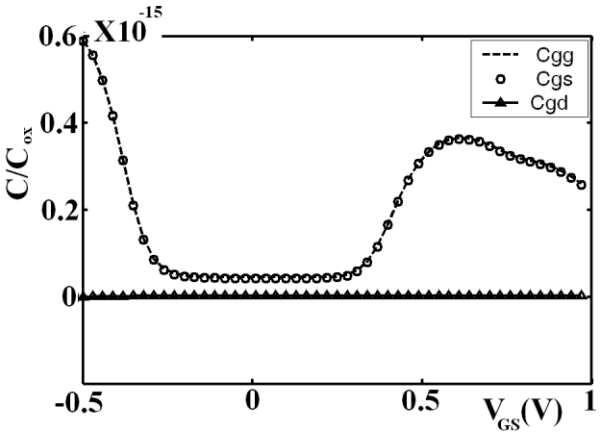

Fig. 6 At V_{DS}=0V, the C versus V_{GS} is plotted. Normalized magnitude of capacitance with respect to oxide capacitance is plotted for V_{DS}=0V.

V. CONCLUSION

In this paper PGAA cylindrical TFET is proposed with InAs in source and channel. Gate full source and half channel has OFF current 10^{-9} A and SS is 42mV/dec. The potential of the proposed device increases with scaling down of oxide thickness, and hence immunity toward short channel effect reduces. Optimization is carried out with various gate metals with different workfunction. With increasing work function the OFF current decreases, V_t changes and, also the vertical electric field decreases. Moreover, better performance can be obtained by decreasing the gate to drain capacitance. Hence, the proposed device is suitable for low power analog and digital applications.

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