Image Denoising using FPGA Based 2D-DWT Architecture

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Abstract*— *In this work, a simple design is implemented for removing noise from gray scale images, that depends on Two Dimensional Discrete Wavelet Transform (2D-DWT) and a threshold stage. The proposed design is used to remove two types of noise (the Salt and pepper noise, and the Gaussian noise) from the corrupted images. The proposed architecture is based on lifting scheme approach using the (5/3) wavelet filter. This architecture consists of a control unit, a processor unit, two on-chip internal memories to speed up system operations, and an on-board off-chip external memory (Intel strata parallel NOR flash PROM). The proposed architecture is designed and synthesized with the VHDL language and then implemented on the FPGA Spartan 3E starter kit (XC3S500E) to check validation of the results and performance of the design.

***Keywords*:—** *Two Dimensional Discrete Wavelet Transform (2D- DWT), image denoising, lifting scheme, (5/3) wavelet filter, and FPGA applications.*

I. INTRODUCTION

The discrete wavelet transform (DWT) has become one of the most used techniques for signal analysis and image processing applications. During the last decade, with the progress of wavelet theory, DWT plays a significant role in many fields such as image compression, speech processing, noise removal, pattern recognition and so on [1]. Since the DWT is implemented by using convolution method which is based on filter bank structures, it requires large number of arithmetic computations and large storage area, features that are not desirable for either high speed or low power hardware applications [2]. The lifting scheme was introduced by Win Swelden in 1995 [3] to eliminate the need for multiple addition and multiplication processes necessary for convolving any filter with the image.

Image manipulation, includes a wide range of operations like copying, transmitting, displaying…etc. Unfortunately, such manipulations generally degrade the image quality by spanning many types of noise. Hence, to enhance these images, the undesired noise needs to be removed. In image processing, noise removal is achieved through the usage of filtering-based denoising techniques. However, the filtering techniques lead in some cases to baneful effects when applied indiscriminately to an image. In fact, if it is not the whole image that is blurred, some of its important features (e.g. edges) are. A solution to overcome this problem has been introduced by Denoho and Johnstone [4]. Their technique consists of using the DWT followed by a thresholding operation. This method exploits the energy compaction ability of the wavelet transform to separate the image from the added noise.

The role of the threshold is to eliminate the noise present in the image. Finally, the enhanced"denoised" image is recovered by applying the inverse DWT. This method is also known as the wavelet shrinkage denoising [5].

Many recent DWT architectures have been developed and implemented for image denoising. The following applications represent some previous works, which are related with the image denoising by wavelet transform on FPGA technology:

In 2002, Yousef M. *et al*. [6] proposed an effective of both soft and hard thresholding for desired detail levels. Pipelining of the proposed algorithm allows it to be used for real-time processing. Implementation of the proposed denoising algorithm is performed by using Xilinx Virtex -II FPGA device.

In 2006, Jonathan J. *et al*. [7] proposed a reconfigurable system for denoising images based on the statistical modeling of wavelet coefficients. The architecture has regular data flow and is adaptable to arbitrary image sizes. The wavelet used is the Daubechies' (9/7) wavelet, The implementation is achieved on a Xilinx Virtex-II FPGA device. The modules were written in VHDL behavioral description.

In 2008, Mohamed I. *et al*. [8] developed a denoising method based on wavelet packet shrinkage. The principle of wavelet packet shrinkage for denoising and the selection of thresholds and threshold functions were analyzed. The design is implemented on the Altera FPGA device using six-levels of Daubechies wavelet with soft thresholding.

This paper focuses on the hardware implementation of the lifting scheme as applied for (2D-DWT) using the (5/3) lifting filter, and image denoising algorithm. The proposed architecture is designed by using VHDL language and implemented on FPFA Spartan 3E starter kit. The input image size is (512×512) pixel that cannot be possible to be stored in the internal block RAM. Because of the limited FPGA internal memory size in the Spartan 3E, so an external memory is used to store the original image. There is an on board 128Mbit Intel strata flash (parallel NOR flash PROM) which is used for image storing and all decomposition subbands. For result testing, the Xilinx chip scope tool is used as a validation tool.

II. THE LIFTING SCHEME

The Lifting scheme (LS) is a method to simplify performing the wavelet transform in an efficient way. The (LS) has some advantages when compared with classical filter banks method, such as the fewer and simpler arithmetic computations required, the simple and fast hardware implementation, the ease of inverse implementation, occupying less memory storage, in addition, the (LS) is more appropriate for high speed and low power applications such as the image/video processing applications.

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The disadvantages of lifting scheme is that the multiplier and adder delays are longer than convolution ones (has longer critical paths) [9]. The (LS) can be performed by three steps: the split stage, the predict stage, and the update stage. In the split stage the input signal or image is separated into even and odd indexed samples. The predict stage computes the high pass filter coefficients representing the details subband. The update stage gives low pass filter coefficients which stands for the approximation subband of the DWT process. For (5/3) wavelet filter the predict and update stages are represented in following equations [4]:

$$d(n)=X(2n+1)-0.5[X(2n)+X(2n+2)] \quad (1)$$

$$a(n)=X(2n)+0.25[d(n)+d(n-1)] \quad (2)$$

Where:

X(n): Is the input signal.

d(n): The details coefficients.

a(n): The approximations coefficients.

The advantage of lifting scheme is that, the inverse DWT can be obtained from the same architecture that is used for the forward DWT, but with inversing the sequence of the stages, changing the sign of the stages, and replacing the split stage with merge stage [10]. The data is first updated, then predicted and finally merged.

For (5/3) wavelet filter the update and predict stages for inverse lifting scheme are represented in following equations [4]:

$$X(2n)=a(n)-0.25[d(n)+d(n-1)] \quad (3)$$

$$X(2n+1)=d(n)+0.5[X(2n)+X(2n+2)] \quad (4)$$

From lifting scheme wavelet transform equations, it is noticed that hardware design requires only adders and shifters instead of multipliers. Fig. (1) shows the lifting scheme DWT block diagram for the analysis and the synthesis stages.

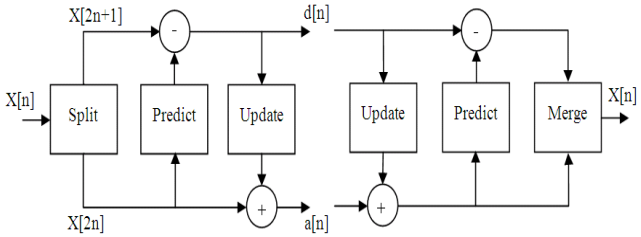

Fig. (1) Analysis and synthesis stages of lifting scheme [5].

III. WAVELET DENOISING

For the applications of interest, noise is primarily high frequency, while the signal to be denoised is primarily low frequency. Because the wavelet transform decomposes the signal neatly into approximations (low frequency) and details (high frequency) subbands, the details coefficients will contain much of the noise. This suggests a method for denoising the signal: simply reduce the size of the detail coefficients before using them to reconstruct the signal. This approach is called thresholding the detail coefficients. Of course, we cannot throw away the detail coefficients entirely; they still contain some important features of the original signal. Various kinds of thresholding have been proposed, and also the kind of thresholding is best depending on the application. The two different approaches which are usually applied for denoising: hard thresholding or soft thresholding [8]. Fig. (2) shows the hard and the soft thresholding approaches with denoising threshold (δ) [11].

Hard thresholding can be described as the usual process of setting to zero the elements whose absolute values are lower than the threshold. Soft thresholding is an extension of hard thresholding, first setting to zero the elements whose absolute values are lower than the threshold, and then shrinking the nonzero coefficients toward zero [11].

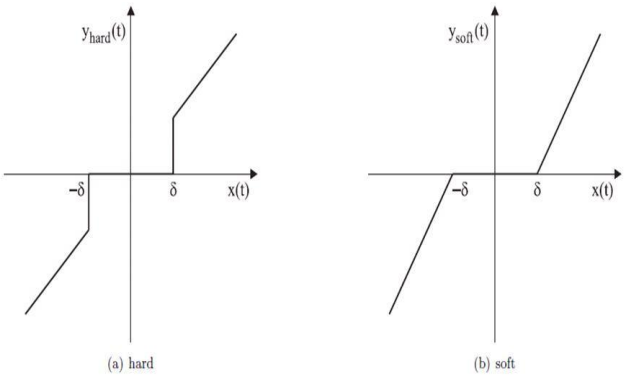

Fig. (2) Threshold types; (a) Hard, (b) Soft [12].

$$y_{hard} = \begin{cases} x(t), & |x(t)| > \delta \\ 0, & |x(t)| \le \delta \end{cases}$$

$$y_{soft} = \begin{cases} sign\,(x(t))\,(|x(t)| - \delta)\,, & |x(t)| > \delta \\ 0, & |x(t)| \le \delta \end{cases}$$

The hard and the soft thresholding are described analytically as: [12].

The general de-noising procedure involves three steps. The basic version of the procedure follows these steps [11]:

1. Decompose: Choose a wavelet, choose a decomposition level *N*. Compute the wavelet decomposition of the image at level *N*.
2. Threshold detail coefficients: For each level from 1 to *N*, select a threshold and apply the required thresholding to the details coefficients.
3. Reconstruct: Reconstruct the image using the original approximations coefficients of level *N* and the modified details coefficients of levels from 1 to *N*.

When thresholding is applied, no perfect reconstruction of the original signal is possible [12]. However, it is generally impossible to remove all the noise without corrupting the signal [11]. Only the large coefficients are used for the reconstruction of the image. The denoising is not limited to a special kind of noise, different kinds of disturbances can be filtered out of the images [12].

IV. PROPOSED ARCHITECTURE FOR 2D-DWT

This section presents and explains the overall design of a 2D-DWT module for image denoising, hardware and software tools that are used for design simulation, implementation, and the output results verification. The following sections explain the main design steps, starting with word length of the DWT coefficients, calculating the threshold value for denoising operation, simulation and testing the results with MATLAB program. After that, the VHDL design used for DWT processor unit, arranging the on-chip internal memory units, and control unit are given. The chip scope program is used as a verification tool for checking and testing the application results.

A. Word Length and Threshold Value:

At first, before designing the 2-D DWT processor, DWT coefficients word length must be taken into consideration.

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The word length means the number of bits per pixel. The original image data word length is 8-bits per pixel, this amount of bits is not enough for wavelet transform coefficients. It is observed that the retrieved image in inverse discrete wavelet transform has distortion, because of overflow condition. The overflow occurs when the addition operation result may be larger than can be held in the word length being used. In DWT the word length of wavelet coefficients will grow gradually in FDWT in each DWT level, and as the DWT levels are more. To select the appropriate word length, the MATLAB program is used for writing appropriate code to simulate the (5/3) wavelet filter in (FDWT) and (IDWT). With (FDWT) MATLAB program the Lena test image of size (512×512×8) is used as the original input image, it is analyzed for two levels of decomposition by using different word lengths, then the (IDWT) is used to reconstruct the retrieved image.

The mean square error (MSE) and peak signal to noise ratio (PSNR) are used to determine the retrieved image accuracy. Table (1) shows word length effects on the PSNR values, this table is calculated by using MATLAB environment.

$$PSNR = 10\log\frac{(255)^2}{MSE} \quad (6)$$

$$MSE = \frac{1}{n}\sum_{i=1}^{n}(Pi - Qi)^2 \quad (5)$$

Where, n: number of image pixels, Pi: original image pixel, and Qi : retrieved image pixel.

From table (1), it is noticed that the (10 bit) data length makes the (PSNR=Infinity) for two levels, the wavelet coefficients should be large enough to prevent the overflow, so the filter coefficients and the 2D- DWT coefficients are represented by 10 bit.

Images	PSNR				
	8bit	9bit	10bit	11bit	12bit
Cameraman	18.04	53.52	∞	∞	∞
Lena	17.88	72.03	∞	∞	∞
Peppers	13.98	38.94	∞	∞	∞
Goldhill	18.25	54.98	∞	∞	∞

Table (1). PSNR values for the images with two levels of decomposition.

The effective decomposition level must be determined because it is one of the most important factor in the wavelet denoising. If the higher decomposition level is used, the thresholding can eliminate some coefficients of the original image, therefore, to increase the decomposition level too high will decrease the PSNR after an optimal level and also increase the complexity of the decomposition. For this purpose, a noise added image will be used to obtain how the performance is changing with respect to the decomposition level. A Gaussian noise and salt and pepper noise are added to Lena test image, that made the PSNR between the original image and the noisy image almost (16 dB) for both noise types. Table (2), illustrates the PSNR values after denoising process for various decomposition levels. The best PSNR value is obtained at the decomposition level of two.

Table (2), PSNR values with respect to the decomposition levels after DWT denoising.

levels	PSNR for Gaussian noise	PSNR for salt and pepper noise
1	21.6468 dB	20.9337 dB
2	25.1337 dB	24.4707 dB
3	24.3734 dB	24.0790 dB
4	22.0639 dB	21.8936 dB

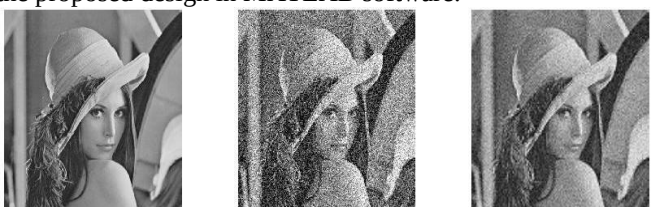
Regarding the type of denoise thresholding, the hard thresholding function is used, because it is the simpler method for hardware implementation and it gives acceptable results with the image denoising. The thresholding value is computed depending on the MATLAB program results in order to get the best image quality after image denoising operation. The denoising algorithm is applied on the noised Lena image (512x512) with two types of noise (salt and pepper, and Gaussian). In the FDWT, two levels of decomposition is used with thresholding. The thresholding value is based on the universal thresholding method, which was proposed by donoho in (1993), the universal thresholding function is given as [13]:

$$\delta = \sigma\sqrt{2\log(n)} \quad (7)$$

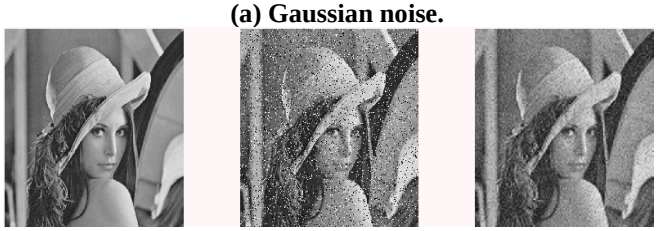
Where, (n) is the number of pixels of the processed image, (σ) denotes the standard deviation of the noise.

For Lena test image, the PSNR between the original image and the noisy image (having Gaussian noise with σ =40) is (16.1003dB), after performing the denoising algorithm on the noisy image, the PSNR between the original image and the retrieved image becomes (25.286 dB).

Regarding with the salt and pepper noise, the PSNR between the original image and the noisy image (having noise density =0.15) is raised from (13.698 dB) to (23.102 dB) after denoising. The thresholding value and the results are obtained by using MATLAB software. Fig. (3) shows the original image, the noised image, and the filtered image using the proposed design in MATLAB software.



(a) Gaussian noise.



(b) Salt and pepper noise.

Fig. (3): denoising Lena test image, for (a) Gaussian noise, (b) salt and pepper noise.

B. 2D-DWT Architecture Design:

The 2D-DWT is designed depending on the lifting scheme structure. The (5/3) wavelet filter is used to implement the DWT processor design. The proposed design consists of two separate architectures. The first architecture performs the 2D-FDWT (Two Dimensional Forward Discrete Wavelet Transform) on the stored image with two-levels of decomposition and applies the thresholding method for denoising, and stores the DWT coefficients in the external strata flash memory. The second architecture performs the 2D-IDWT (Two Dimensional Inverse Discrete Wavelet Transform) on the stored DWT coefficients in order to retrieve the decomposed image.

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Both the 2D-FDWT system and the 2D-IDWT system have the same architecture and components, but the difference between these two systems, is in the internal functions and arithmetic operations for the DWT processor unit, therefore both the two systems have the same block diagram, see Fig. (4). The proposed architecture consists of four different components, these components are discussed in the following sections:

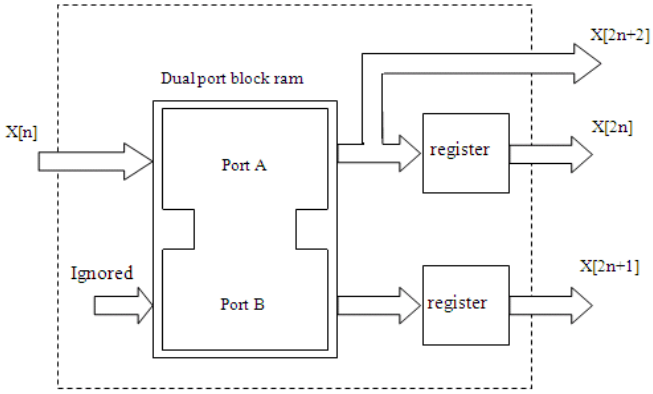

Fig. (4): Block diagram of the proposed architecture for 2D-DWT.

B.1. Internal Memory Units:

There are two internal on-chip memory units in the system design, each one has size (2N) for (N×N) image, these memory units are used to speed up the DWT system assignments because the internal memory is faster than external memory. Each of these internal memory units is a single dual port Block RAM. Therefore only one clock cycle is needed for reading or writing two words of data in two random memory locations.

The first memory unit works as a split stage for the lifting scheme wavelet transform, this unit works on separating the even indexed pixels from the odd indexed pixels. The separation process can be done by putting out even memory locations from (port A) output port, and odd memory locations from (port B) output port. This unit consists of a dual port block ram with two registers connected to the block ram output ports as shown in the Fig. (5). This arrangement delivers three outputs (X[2n], X[2n+1], and X[2n+2]) form the memory unit at each clock cycle to the DWT processor unit. Since, the DWT processor has two outputs for each clock cycle the (LPF, and HPF) coefficients, a second memory unit is necessary. This memory unit is also a dual port Block RAM used as dual input ports and single output port. This unit brings out the wavelet coefficients toward the strata flash memory.

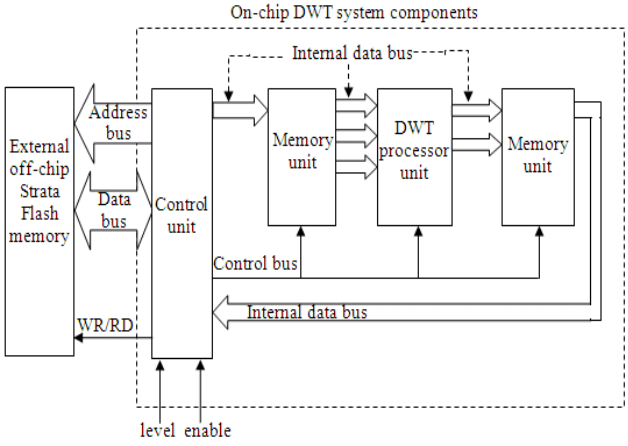

Fig. (5): Organization of the first memory unit.

B.2. DWT Processor Unit:

This unit represents the hardware design of the (5/3) lifting scheme filter, it contains predict stage and update stage. The same unit is used for row operations and then for column operations. This unit has three input ports connected to the three output ports of the first memory unit, and has two output ports connected to the input ports of the second memory unit as shown in the Fig. (4). In the FDWT system this unit is designed to perform the lifting scheme analysis equations (1, and 2), and the hard thresholding function on the incoming noisy image data. The proposed approach is generally simple and effective. In this approach, the discrete wavelet transform (DWT) of an incoming noisy image data is calculated and the resultant details wavelet coefficients are passed through a threshold testing. In this case, the coefficients that are smaller than a certain value are removed. Then the resultant coefficients are used to reconstruct the image after denoising, with this method it is possible to remove noise with little loss of details. In the IDWT system, this unit is designed to perform the lifting scheme synthesis equations (3, and 4) on the wavelet subbands for each reconstruction level in order to get the denoised image.

B.3. Control Unit:

There are two duties for the control unit. The first, it controls the on-chip DWT system components, see Fig. (4), by providing control signals (read, write, status, and enable), also it gives the appropriate addresses for memories units, and controls the data flow in the proposed design. The second, it provides complete interface signals and buses with external memory (read, write, enable, address bus, and data bus).

There are two input signals that are connected to the switches of the FPGA kit, these control signals must be asserted by the user before starting the system operations. First one is the DWT level signal, used to select the wanted DWT levels. The Second is the enable signal, used to enable the system components to perform DWT operations. After setting the (enable and level) signals, the control unit is responsible for all system operations starting with reading data from external memory, enable DWT processor unit operations, and writing DWT subbands to the external memory.

B.4. External Memory (Strata Flash):

The external memory is the on board 128Mbit Intel strata flash (parallel NOR flash PROM). It is used for storing the original image and later the DWT coefficients. This memory is configured as (8 Mword) (128Mbit), each memory location is of (16 bit) word size, the strata flash memory has (23 bit) memory address bus width, 16 bit data bus width, and three important control signals that must be taken in to consideration (chip select, output enable, and write enable).

The strata flash memory controller is designed by using the VHDL language to be appropriate for the proposed design. This controller is included in the proposed DWT control unit, already mentioned. The original image data is converted to hexadecimal format before storing it in the memory, the conversion operation is achieved by using a MATLAB program. In order to store the original image in the on board memory, the strata flash controller is used for writing image data file, in the addressed memory locations.

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The DWT proposed architecture for image denoising is downloaded on the FPGA chip to process noisy image and store the wavelet coefficients in the strata flash memory. Then the IDWT architecture is implemented on the FPGA in order to get the denoised image, which is stored also in the strata flash memory.

V. APPLICATION RESULTS

A. FPGA Synthesize and Implementation:

The proposed architecture designed with VHDL is then synthesized, placed, and routed by using Xilinx ISE 10.1 software. The proposed design is implemented on the Xilinx (XC3S500E) chip using Spartan 3E FPGA starter kit. The grayscale Lena test image with size (512×512) is stored as an original image in the on board strata flash memory. After implementing the proposed design on the FPGA device the resources utilization are shown in table (3), and the maximum operation frequency is 52.84MHz.

Table (3). The Device Utilization Summary.

Logic utilization	Used	Available	Utilization
Number of slices	1,464	4,656	31%
Number of slices flip flops	818	9,312	8%
Number of 4 input LUTs	2,321	9,312	24%
Number of BRAMs	2	20	10%
Maximum frequency	52.84MHz		

B. Results Verification and Checking:

The results are checked by using chipscope program, the chip scope is a xilinx product that inserts a software logic analyzer onto the FPGA chip, it is used for verification of the FPGAs designs. The chipscope product can be integrated in the ISE project as a component, it can be connected to inputs, outputs, and intermediate signals of the design that are implemented on the FPGA device. In this research, after implementing the proposed design on the FPGA device for computing the DWT coefficients, the Xilinx chipscope program was used as a validation tool once the system was running in a Spartan 3E starter kit. Fig. (6) shows the signals of the proposed design.

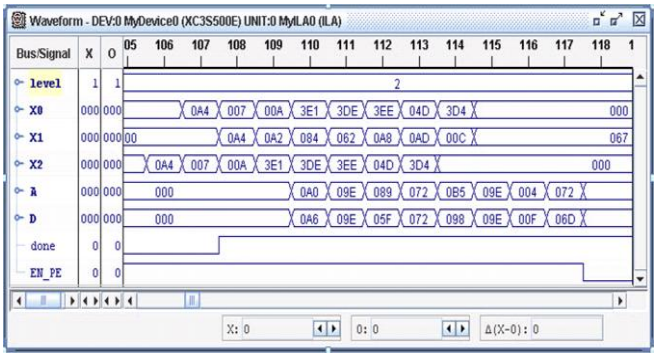

Fig. (6): The chipscope program shows proposed design signals.

C. Reading The External Memory:

After completing the DWT operation, all the DWT subbands are stored in the external on board Strata Flash memory. An UART (Universal Asynchronous Receiver Transmitter) design is used for reading strata flash memory contents, this design is loaded on the FPGA chip to provide serial data communication between the Spartan 3E kit and the personal computer through RS-232 serial link. The Hyper Terminal program is adequate for managing this communication. Once the UART design is loaded into the Spartan 3E, a new hyper terminal session can be started. This session needs to configure the serial port setting (baud rate, data bits, parity, stop bits, and flow control) before connection with the UART design. When a correct connection is established between Spartan 3E (UART) and the personal computer (Hyper Terminal), the contents of the strata flash memory will be appeared on the hyper terminal program as hexadecimal data and stored into a text file with hexadecimal format.

The MATLAB program is used for some duties, such as reading the image text file contents according to the DWT subbands and displaying these subbands, also it is used to read and display the retrieved image after denoising operation, and to compute the PSNR. Fig. (7) shows the original image, the noisy image (with Gaussian noise σ =60), and the filtered image using the proposed design for standard (512×512) Lena image.

Fig. (7): Image denoising by using FPGA hardware design.

Tables (4) and (5), illustrate the PSNR values before and after the denoising operations for various noisy test images (having Gaussian noise with different noise variance values as in table (4), and having salt and pepper noise with different noise density values as in table (5).

Table (4). Gaussian noise:

Image	Noise σ=40		Noise σ=60		Noise σ=80	
	PSNR (dB) before denoising	PSNR (dB) after denoising	PSNR (dB) before denoising	PSNR (dB) after denoising	PSNR (dB) before denoising	PSNR (dB) after denoising
Cameraman	16.083	24.588	12.569	22.384	10.094	20.481
Lena	16.100	25.286	12.567	22.907	10.071	20.950
Goldhill	16.102	24.813	12.581	22.647	10.065	20.633
Baboon	16.083	20.287	12.553	19.343	10.075	18.330

Table (5). Salt & pepper noise:

Image	Noise density=0.15		Noise density=0.2		Noise density=0.25	
	PSNR (dB) before denoising	PSNR (dB) after denoising	PSNR (dB) before denoising	PSNR (dB) after denoising	PSNR (dB) before denoising	PSNR (dB) after denoising
Cameraman	13.276	21.459	12.091	20.312	11.104	19.306
Lena	13.698	23.102	12.427	21.832	11.456	20.924
Goldhill	13.574	22.584	12.354	21.573	11.401	20.520
Baboon	13.798	19.570	12.563	19.084	11.601	18.600

VI. CONCLUSIONS

The wavelet denoising techniques offer better quality and some flexibility for noise problems of signals and images. In this work, the proposed 2D-DWT architecture for image denoising is based on the lifting scheme approach, which proves fast and easy hardware implementation, few and simple arithmetic computations,

and occupies less memory storage, therefore it is appropriate for FPGA solutions.

A simple hard threshold method is introduced based on the universal threshold function in order to remove two types of noise (gaussian noise, and salt and pepper noise) from various noisy test images. Subjecting the noisy images to FDWT with appropriate thresholding value, and IDWT for both types of noise gave image enhancement (reaching to about 10 dB). The best decomposition level for FDWT proved to be two levels, which gives highest PSNR between the original image (noise free) and the denoised image.

The image is saved in the strata flash prior to arrange for DWT, and the FDWT subbands coefficients and the retrieved image (denoised image) are then stored as they result during the hardware application also in the same chip. The strata flash was used because it is easier to be reached and implemented. The 2D-DWT hardware application was tested using chip scope software, while the data verification was tested using MATLAB software, by computing the PSNR values between the original image and the denoised image.

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