

DDS Based Multi Channel Radar Waveform Generator

B.Suresh, M.V.Srikanth

Abstract- A radar waveform generator is designed and it is implemented by using directly digital modulation method based on DDS. It can generate arbitrary signals whose amplitude, frequency or phases are controlled by the description words given from an external computer. Accurate waveforms can be generated. We can generate waveforms digitally by using Direct digital synthesis technique. DDS principles of the technique are simple and widely applicable. Direct Digital Synthesizer (DDS) is a frequency synthesizer which can generate arbitrary waveforms from a single, fixed-frequency reference clock. DDS Applications include: function generators, modulators. Here in order to implement radar waveform generator along with DDS we need FPGA and microcontroller. In order to generate the waveform using DDS we need to store the hexadecimal data into the internal registers of DDS chip along with that we need some control signals which will be generated using FPGA. First from PC we need to send the hexadecimal data through serial port for that we need design a Graphical User Interface (GUI). In GUI we will enter the amplitude, phase and frequency of the waveform to be generated and then it has to convert it into particular hexadecimal data based on the formulas mentioned in the datasheet, then it has to send the data through serial port. Now, microcontroller has to receive the data from PC and then it has to send the data to the FPGA. FPGA has to receive that data, along with that it has to generate some control signals based on the control signals, received data will be send to the internal registers of DDS chip.

Keywords: Direct Digital Synthesizer (DDS), FPGA microcontroller

I. INTRODUCTION

Generally in any equipment, it is important to readily control and produce accurate waveforms of different frequencies. . Examples include agile frequency sources with less phase noise and low spurious signal content for communications, which will be used for biomedical and industrial applications. For such applications, we should be able to generate an adjustable waveform conveniently and cost effectively is a key design consideration. Various approaches are available to generate the signal but direct digital synthesis (DDS) is most flexible one. AD9910 DDS chip will generate an analog signal —usually a sine wave, but we can generate other signals also by generating a time varying signal in digital form and then by using D/A converter we generate an analog signal. DDS devices will offer faster switching between output frequencies and fine resolution in frequencies.

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As the technology advances in design and technology ,DDS devices consume less power and very compact .Here we are using AD9910 DDS chip it will generate signal with frequencies ranging from 1Hz to 400 MHz (based on a 1-GHz clock), with time resolution of 64 bits. Devices with low cost and using new process technologies are combined with DDS's which can produce waveforms and can be program them digitally—make DDS as attractive approach compared to other solutions. Multichannel waveform generator can be designed using multiple AD9910 DDS chips and microcontroller along with FPGA to control those DDS chips. Here we are designing 4 channel waveform generator using 4 DDS chips, which produces four identical waveforms whose phase, amplitude and frequency can be varied digitally. Our objective here is to design and develop a multi channel radar waveform generator . First we need to design a GUI where we will enter the information of the waveform to be generated such as amplitude, phase and frequency. GUI will convert the information entered into hexadecimal data and send it to the microcontroller using RS232 cable. We can also control the DDS chip in GUI. Microcontroller will receive the data and send it to the FPGA through SPI. FPGA will generate clock and control signals to DDS chips based on the control signals FPGA will transfer the received data to the internal registers of DDS through SPI. Now DDS will generate the signal based on the data present in the registers.

II. DDS TECHNOLOGY

Direct digital synthesis (DDS) is a method of generating an analog waveform such as sine wave by using time varying signal in digital form and then by using digital to analog converter we can generate an analog signal. It has an ability to control and generate an accurate signal that's why it has been used by most of the industries. DDS technique is mostly used for solving signal generation requirements for both industrial applications and communications because single chip is able to generate an accurate analog signal with low cost and power consumption.

DDS principle of operation can be easily understood with the Fig.1. Phase accumulator will take the Frequency tuning word as input and converts into angular phase and then it is converted into the sine wave amplitudes by Amplitude/Sine Conv. Algorithm and then it is converted to analog sine wave output by D/A converter.

Generally DDS is used to produce a sine wave at a given frequency. The output frequency mainly depends on the reference-clock frequency and tuning word. The frequency tuning word is the main input to the phase accumulator. Phase accumulator is used to compute the phase (angle) address for the look up table if sine look-up table is used, which gives the digital value of amplitude — corresponding to that phase angle to the DAC.



The DAC will convert that digital value into corresponding analog current or voltage. To generate sine wave of fixed frequency a constant value is added to phase accumulator. If tuning word is large, the phase accumulator will step through the look up table quickly. If it is small the phase accumulator will take more steps thus generating a slower waveform.

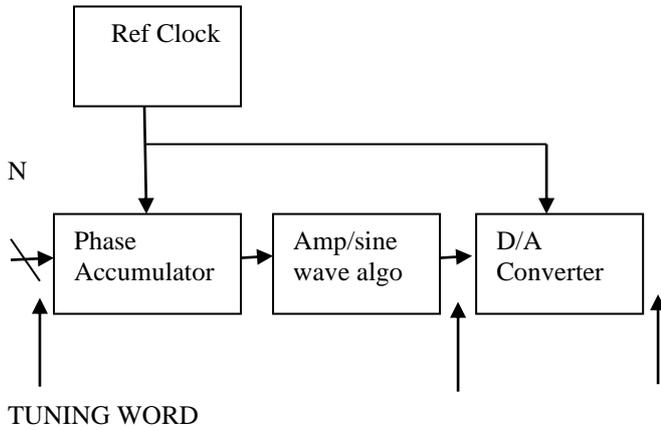


Fig.1. DDS architecture

Where N denotes the number of bits used to represent the tuning word. Generally for AD9910 Frequency Tuning Word (FTW) is of 32 bit.

$$f_o = \frac{M \times f_c}{2^N}$$

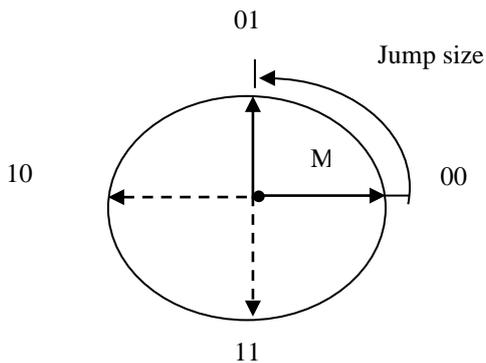
Where:

f_o = output frequency of DDS

M = frequency tuning word

f_c = internal clock frequency

N = length of the phase accumulator in bits



N	NUMBER OF POINTS
8	255
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

Fig.2. DIGITAL PHASE WHEEL

For understanding the basic function consider sine wave oscillations as a vector rotating around a phase circle. The number of discrete points can be determined by the resolution of phase accumulator. Each point on the phase circle corresponds to equivalent point on cycle of sine waveform.

As the vector rotates along the wheel, corresponding output sine wave will be generated. As vector completes one revolution at a constant speed around the phase wheel it completes one cycle of output sine wave. The phase accumulator will provide the equivalent of the vector's linear rotation around the phase wheel. Each content of the phase accumulator represent the corresponding point on the cycle of the output sine wave. The number of phase points on the wheel are determined by the resolution N of phase accumulator. As the output of the phase accumulator is linear we cannot directly generate any wave expect ramp. So, we use phase-to-amplitude lookup table to convert output value of phase accumulator to sine wave amplitude information and then it is applied to D/A converter. The output frequency and length of the accumulator are related by the equation.

Here we are using AD9910 DDS chip which can generate waveforms ranging from 1Hz to 400 MHz, whose clock frequency is 1 GHz with 14 bit DAC.

III.SYSTEM ARCHITECTURE

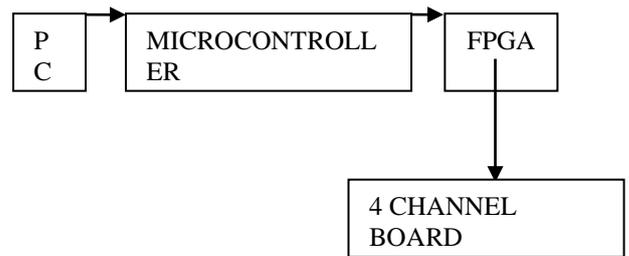


Fig.3. Block diagram

GUI: In order to generate the radar signals we need to store the corresponding hexadecimal data into the internal registers of DDS. so we need GUI to convert the corresponding amplitude, frequency and phase description into corresponding hexadecimal data using the formulas specified in the AD9910 datasheet and it has to send the hexadecimal data through serial port from the pc.

PIC: As we are sending data from pc using GUI through serial port. we have to receive the data send by the pc so we are using PIC microcontroller. PIC micro controller has to receive the data from the serial port and it has to send the data to the FPGA .Here we are using DSPIC33F. By using USART functions of DSPIC33F we can receive and store the data available at the serial port.

FPGA: We have to send the data to the DDS based on some control signals and we have to provide some clock signals to the DDS so we are using FPGA. PIC will send the data received from the pc to the FPGA using SPI. FPGA will provide clock signal to the DDS and it has to receive the data from PIC and based on the control signals it has to send the data to the DDS

4 CHANNEL BOARD: Our requirement is to generate a identical signals whose phase , amplitude, frequency should be in our control. so in order to generate identical signals first we need to synchronize DDS chips. for synchronization one of the DDS chip has to generate SYNC_CLK and ADCLK846 will distribute that SYNC_CLK to all the DDS chips. one which

Generate the SYNC_CLK behaves like master remaining as slaves, thus the DDS chips are synchronized and they will operate on the same internal clock so they will produce identical signals. SYNC_CLK will be generated from the internal clock only by using frequency divider. AD9520 will distribute the clock signal generated by the FPGA to all the DDS chips. From FPGA we will provide the 10 MHz signal, but AD9910 clock frequency is 1 GHz so, we will multiply the 10Mhz signal to get desired 1 GHz frequency using the internal multiplier of the AD9520.

By using these devices the RADAR waveform generator is designed. Now in the GUI we need to enter the amplitude, phase and frequency and we need set the mode in which the AD9910 DDS chip has to operate generally we will operate the DDS chip in single tone mode in which DDS will generate the signal based on the information provided from the serial port. After setting all the controls we will send the data to be stored in the registers through serial por. Now DSPIC33F will receive the data and send it to the FPGA through SPI. FPGA will receive the data and then it will send the data to the DDS chips based on some control signals along with that it need to provide clock signals to DDS devices.

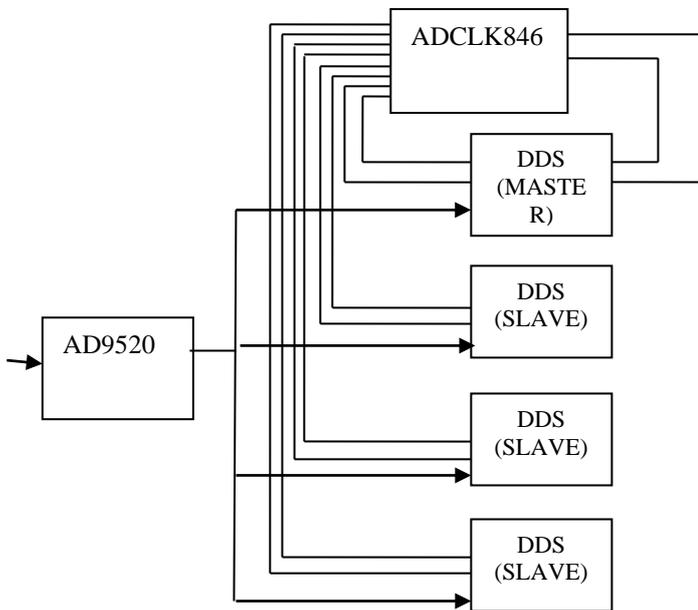


Fig.4 .BOARD DIAGRAM

IV. RESULTS

The below figure shows single frequency output spectrum in which mark1 denotes the frequency of 35 Mhz with an amplitude of 14.21 dbm.

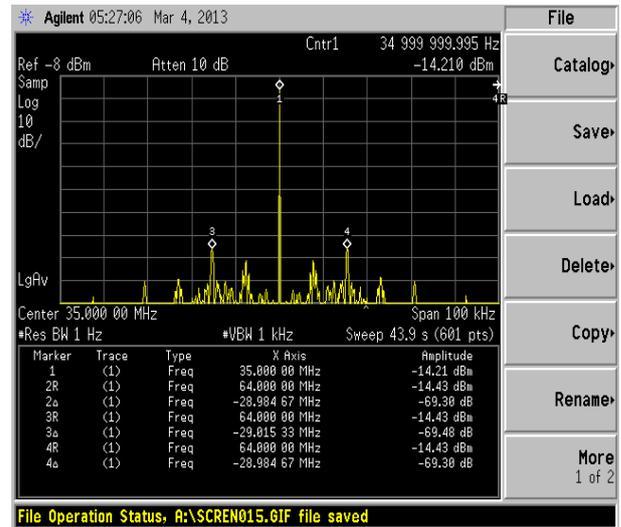


Fig.5. Single frequency output spectrum

Below figure shows dds output which directed into spectrum analyzer zoomed in.

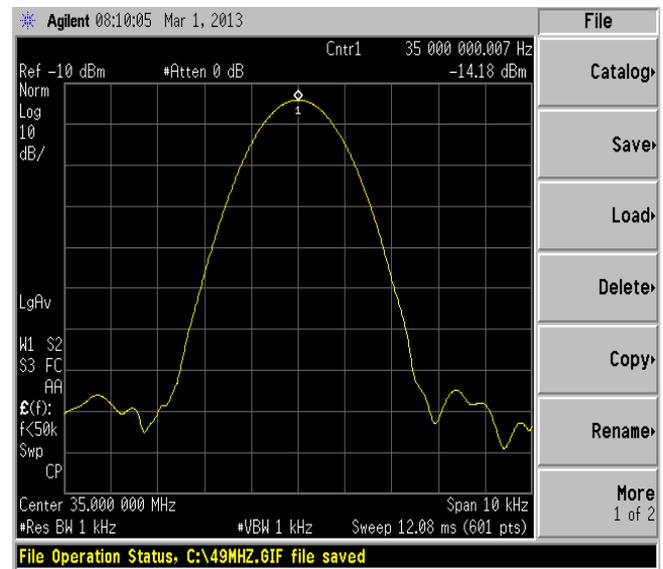


Fig.6. DDS output direct into spectrum analyzer

V. CONCLUSIONS

In this paper, the multichannel waveform generator is designed using multiple AD9910 DDS chips. This design shows the multichannel radar waveform generator architecture which is designed using AD9910 DDS chips, PIC microcontroller and FPGA.

REFERENCES

1. "Development of an Eight Channel Waveform Generator for Beam-forming Applications", john ledford.
2. "FPGA-Based Design, Implementation, and Evaluation of Digital Sinusoidal Generators", 2008 IEEE.
3. Analog Devices, A technical tutorial on digital signal synthesis, 1999.
4. Microchip, MPLAB_User_Guide_51519c
5. Digital frequency synthesis demystified / Bar- Giora Goldberg, 1999.
6. Digital modulation techniques / Fuqin Xiong,2000.
7. Xilinx Spartan-3E Evaluation Kit User Guide
8. Analog Devices, AD9910 Data Sheet.

9. Analog Devices, ADCLK846 Data Sheet
10. Analog Devices, AD9520 Data Sheet.
11. Analog Devices, CN0121 Circuit Note.
12. Spartan3E_FPGA_User Guide
13. Cadence Layout_Tutorial
14. Microchip, dsPIC33F Product Overview

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