International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-2 Issue-3, July 2013

Optimization of CMOS 8-bit Counter using SLA and Clock Gating Technique

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Abstract*—The development of digital integrated circuits is challenged by higher power consumption. Scaling helps to improves transistor density, increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Power consumption has a static component coming from the leakage of inactive devices and a dynamic component coming from the switching of active devices. It has been proved that clock signal consumes a high dynamic power as the clock net has one of the highest switching densities. The clock signal keeps changing its state in certain time points according to its frequency even if the logic output doesn't change "hold mode". Switching power dissipation may eventually dominate total power consumption in sub micron technology. Glitches or unwanted transitions consume about 20%-70% of Dynamic Power and needs to be eliminated. Therefore, the main aim of this thesis work is to reduce power consumption due to both glitches and Clock switching. In this thesis work, the novel approaches are proposed for reducing dynamic power with minimum possible power consumption and delay trade off. A novel approach for reducing dynamic power i.e. SLA (State Look Ahead) and Clock Gating has been proposed. Proposed parallel counter shows 66.04% power improvement as compared to Kakarountas counter and 54.3% power reduction as compared to Alioto's counter. Abdel's counter with proposed parallel counter shows 29.9% power reduction. Maximum operating frequency is also improved in proposed parallel counter. By using pass transistors drawback of large area in Abdel's counter is optimized in proposed circuit. So the proposed parallel 8-bit counter is optimized in terms of speed, power and area as compared to previous counter designs. Use of Pass Transistor is helpful in reducing or eliminating the glitches from circuit. Clock Switching power reduction designs are also proposed which are more power efficient and have less delay as compared to existing techniques.

***Index Terms*—Dynamic power, Integrated clock gating, Pass transistor, State look ahead logic, Switching activity.**

I. INTRODUCTION

Counters are among the basic blocks in every digital system. Fast and constant time counters are important in high- speed VLSI design as well as in many applications in communication and measuring systems. Circuits such as high-speed counters, frequency synthesizers, and frequency dividers implemented by counters are among the basic building blocks of the above systems. Also, fast and constant time counters with features such as up down counting, radix-2 binary output representation, and value loading are required. A counter is a circuit that produces a set of unique output combinations corresponding to the number of applied input pulses. The number of unique outputs of a counter is known as its mod number or modulus. High-frequency operations require that all the FFs of a synchronous counter be triggered at the same time to prevent errors. The synchronous counter is similar to a ripple counter with two exceptions: The clock pulses are applied to each FF, and additional gates are added to ensure that the FFs toggle in the proper sequence. The advantage of synchronous counter over asynchronous counter is that, Since all inputs are synchronized with a common clock, no interrupts can occur in the middle of a state transition in synchronous counters, all flip-flops change simultaneously and in asynchronous counters, the propagation delay of the flip-flops add up to produce the overall delay. Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift, where power dissipation has become as important a consideration as performance and area. Reducing power consumption in very large scale integrated circuits (VLSI) design has become an interesting research area. Most of the portable devices available in the market are battery driven. These devices impose tight constraint on the power dissipation. Reducing power consumption in such devices improves battery life significantly. Due to lesser advancement in battery technology, low power design has become more challenging research area. Power consumed in a digital circuit is of two types. (1) Static power and (2) Dynamic power. Static power consists of power dissipated due to leakage currents whereas dynamic power consists of capacitive switching power and short circuit power. CMOS has been the dominant technology for very large scale integration (VLSI) implementations. As VLSI circuits continue to grow and technologies evolve, the level of integration is increased and higher clock speeds are achieved. Higher clock speeds, increased levels of integration and technology scaling are causing unabated increases in power consumption. Flip-flops are the critical timing elements which has a large impact on the circuit speed and power dissipation of the system. Clock related power consumption is 60% of the total chip power i.e. this much power is dissipated by the clock distribution circuit out of total chip power. From this clock distribution power 90% is consumed by last part of the clock distribution network. There are basically four sources of power dissipation digital CMOS circuits which is the switching power, short circuit power, leakage power and the static power [31].

Revised Manuscript Received on 30 July 2013.
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In the digital circuits, the power dissipation on the signal switching (dynamic) is dominant.

II. RELATED WORK

Early design methodologies [7] improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance(containing higher significant bits) were enabled when all bits in all modules of lower significance (containing lower significant bits) saturate. Initializations and propagation delays such as register load time, AND logic chain decoding, and the half incrementer component delays in half adders dictated operating frequency. Subsequent methodologies [22], [35] improved counter operating frequency using half adders in the parallel counting modules that enabled carry signals generated at counting modules of lower significance to serve as the count enable for counting modules of higher significance, essentially implementing a carry chain from modules of lower significance to modules of higher significance. The carry chain cascaded synchronously through intermediate D-type flip-flops (DFFs). The maximum operating frequency was limited by the half adder module delay, DFF access time, and the detector logic delay. Since the module outputs did not directly represent count state, the detector logic further decoded the module outputs to the outputted count state value. Further enhancements improved operating frequency using multiple parallel counting modules separated by DFFs in a pipelined structure. The counting modules were composed of an incrementer that was based on a carry-ripple adder with one input hardcoded to "1" [35]. In this design, counting modules of higher significance contained more cascaded carry-ripple adders than counting modules of lower significance. Each counting module's count enable signal was the logical AND of the carry signals from all the previous counting modules (all counting modules of lower significance), thus prescaling clocked modules of higher significance using a low frequency signal derived from modules of lower significance. Due to this prescaling architecture, the maximum operating frequency was limited by the incrementer, DFF access time, and the AND gate delay. The AND gate delay could potentially be large for large sized counters due to large fan-in and fan-out parasitic components. Design modifications enhanced AND gate delay, and subsequently operating frequency, by redistributing the AND gates to a smaller fan-in and fan-out layout separated by latches. However, the drawback of this redistribution was increased count latency (number of clock cycles required before the output of the first count value).

Hoppe *et al.* [13] improved counter operating frequency by incorporating a 2-bit Johnson counter [18] into the initial counting module (least significant) in a partitioned counter architecture. However, the increase in operating frequency was offset by reduced counting capability. In Hoppe's design, counting modules of higher significance were constructed of standard synchronous counters triggered by the Johnson counter and additional synchronization logic. However, the synchronization circuit and initial module still limited the operating frequency and resulted in reduced applicability.

Swatzlander E.E et al. [2] proposed an (n, m) parallel counter circuit which provides an m-bit count of the number of the n-inputs that are logic ONES. A counter differs from a compressor in that compressors have carry inputs and carry outputs in addition to the "normal" inputs and outputs, while counters do not have carry inputs and outputs. The most widely used parallel counters are full adders which are (3, 2) counters and half adders which are (2, 2) counters. Larger parallel counters are especially useful in the implementation of widely used signal processing elements such as multipliers, convolvers, etc. M.R Stan et al. [3] systolic counters have a clock period independent of counter size. Previously proposed systolic counters need to be initialized to non-zero values in order to enter the desired repetitive sequence without a transient phase. This is due to the non-unique redundant representation of the zero-state for up-counters. We propose a systolic down-counter that enters a repetitive sequence directly after reset as it has a unique representation of the zero state. The uniqueness of the zero state is also convenient for modulo-p systolic counters.

M. Alioto et al. in [7] presents a methodology to design high speed power efficient MOS current-mode logic (MCML) static frequency divider. Analytical criteria to exploit the speed potential of MCML gates are first introduced. Then, an analytical strategy is formulated to progressively reduce the bias currents through the stages without affecting the divider operation speed, thereby reducing the overall power consumption. The proposed design approach is general and independent of the process adopted. Due to its simplicity, it can be used in a pencil-and-paper approach, avoiding a tedious and time-consuming trial-and-error approach based on simulations. As a design example, a 1:8 frequency divider is designed and simulated by using a 0.18-mum CMOS process. Ko-Chi Kuo in [8] presents a high-speed CMOS nine-stage programmable counter with lower power consumption. The pulse swallow counter is implemented in TSMC 0.18μm CMOS technology process. The supply voltage is 1.8V. The speed enhancement of proposed circuit is 53.26% faster than that of Chang's counterpart. The decrease of the power consumption per megahertz compared to Chang's counterpart is 21.6%. The average power consumption of pulse-swallow counter is 2.6 mW and 3.275 mW at 2.4-GHz and 5-GHz with 1.8V supply Voltage.

M. Dastjerdi-Mottaghi et al. purpose new and low power architecture for synchronous ring counters which can noticeably reduce the switching activity of the conventional ring counter. To achieve the goal we partition the ring counter into some blocks for each of which we use a special clock gator. The Hot block (the block in which the '1' exists) is the only block the flip-flops of which are clocked. The delay and area overhead of the proposed clock gator is independent of the block size; this enables designer to freely resize the blocks and compromise with area and power overheads. The latency increase in the proposed architecture is independent of the counter width and depends only on the technology. For 90 nm technology it increases the latency by 5%. The architecture noticeably (about 85%) reduces the total switching activity of the counter especially for wide counters. Ajane. Avinash in [27] presents LFSR Counter. Due to the complexity involved in designing systems-on-chip (SoCs), manufacturing costs, testing time, and the amount of test data have all increased.

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It is found that linear feedback shift registers (LFSRs) help alleviate these three issues. For example, [1] introduces a SoC testing scheme in which the input test data are compressed using an LFSR. In [2], an LFSR is used for built-in self-test in the implementation of a Universal asynchronous receiver/transmitter on a field programmable gate array. It is also shown that binary counters used for a SoC consume more test time compared to the LFSR, when the input data set is large. LFSRs are also widely used as event counters and efficient pseudo-random number generators. For example, pseudo-random number generators can be used in cryptography to generate a secret key. Binary counters generally use flip-flops, half adders, and a high-speed carry chain. The delay associated with a binary counter depends on the number of bits in the adder/carry chain circuit. In contrast, LFSR counters use only flip-flops and XOR gates. Their delay is independent of the number of bits in the counter. An on-chip event counter for a processor has a maximum allowable delay of one clock period or 10 ns in this case. In a 0.6-/lm process, the longest binary counter we expect to build with a maximum delay of 10ns is approximately 32 bits. In contrast, the maximum length of an LFSR counter we can build in the same process is much higher than 32 because the delay is independent of N. The major drawback of using LFSR counters is the need to convert the pseudo-random LSFR count to a known binary count. The conversion can be performed using a hardware or software algorithm. Several algorithms exist to do this task. We introduce an algorithm that makes efficient use of memory and time in decoding LFSR counts to a known binary count [20].

S. Vinod Kumar et al. in [29] presents an 8 bit synchronous counter using the improvised Clock Gated Conditional Capture Flip-Flop (CGCCFF). The Conditional Capture Flip-Flop (CCFF) outputs the data, only when the input differs from the output. But, it has redundant transitions due to continuous clock flow irrespective of the input and output logic levels. The clock gating allows the clock, only when there is a need for change in output due to a change in the input. Using, the improvised CGCCFF and hence, avoiding the redundant transitions, author observe a power saving of up to 75% compared to the conventional CCFF. Moreover, it achieves a 60% higher performance than the CCFF and a better negative setup time. Hence, author implemented an 8 bit synchronous counter using the CGCC flip flop. From the experimental results, author observed that, the 8 synchronous counter with CGCCFF saves 15% power than conventional CCFF counter.

Heung Jun Jeon, Yong-Bin Kim and Minsu Choi et al. in [21] has presented a novel low-power design technique is proposed to minimize the standby leakage power in nanoscale CMOS very large scale integration (VLSI) systems by generating the adaptive optimal reverse body-bias voltage. The adaptive optimal body-bias voltage is generated from the proposed leakage monitoring circuit, which compares the sub threshold current (ISUB) and the band-to-band tunnelling (BTBT) current (IBTBT). The proposed circuit was simulated in HSPICE using 32-nm bulk CMOS technology and evaluated using ISCAS85 benchmark circuits at different operating temperatures (ranging from 25 ◦C to 100 ◦C). Analysis of the results shows a maximum of 551 and 1491 times leakage power reduction at 25 ◦C and 100 ◦C, respectively, on a circuit with 546 gates. The proposed approach demonstrates that the optimal body bias reduces a considerable amount of standby leakage power dissipation in nanoscale CMOS integrated circuits. In this approach, the temperature and supply voltage variations are compensated by the proposed feedback loop.

Power consumption is now a major technical problem facing the CMOS circuits in deep submicron process. As process moves to finer technologies, leakage power significantly increases very rapidly due to the high transistor density, reduced voltage and oxide thickness. Jae Woong Chun and C. Y. Roger Chen et al. in [22] has proposed a family of circuit types for low-power design centered around inserting controlling transistors between pull-up and pull-down circuits as well as between pull-up circuits/pull-down circuits and power/ground. In addition, several variations of drain gating are discussed. In the end, an overall procedure for low-power circuit design is proposed by intelligently mixing various proposed circuit types for gates in the circuits based upon gate criticality analysis. Extensive SPICE simulation results were reported using 45nm, 32nm and 22nm process technologies. Significant power reduction is achieved with zero or little increase in the critical path delay of the overall circuits.

III. OPTIMIZED COUNTER

In this paper, we improve counter operating frequency using a novel parallel counting architecture in conjunction with a state look-ahead path and pipelining to eliminate the carry chain delay and reduce AND gate fan-in and fan-out. Clock gated pass transistor D flip-flops are used to optimize power consumption and area. Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. The state look-ahead path bridges the anticipated overflow states to the counting modules, which are exploited in the counting path. The counting modules are partitioned into smaller 2-bit counting modules separated by pipelined DFF latches. The state look-ahead path is partitioned using the same pipelined alignment paradigm as the counting path and thereby provides the correct anticipated overflow states for all counting stages. Subsequently, all counting states and all pipelined DFFs (in both paths) are triggered concurrently on the clock edge, enabling the count state in modules of higher significance to be anticipated by the count state in modules of lower significance. This cooperation between the counting path and state look-ahead paths enables every counting module (both low and high significance) to be triggered concurrently.

The most compact implementation of edge trigger latch is based on inverters and pass transistors as shown in schematic Figure 1. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when clock = 0. Other two chain inverters on the right hand acts in opposite way, and the reset function is obtained by direct ground connection of the master and slave memories, using NMOS devices.

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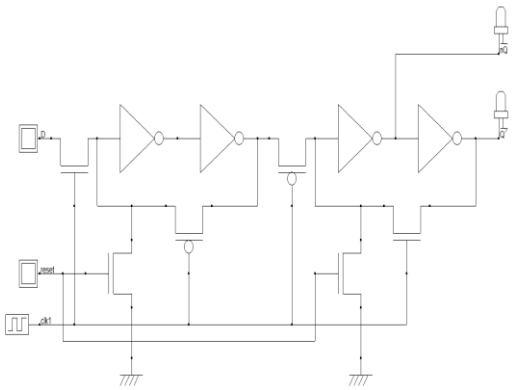

Fig 1: Schematic of D Flip Flop using pass transistors.

This proposed flip-flop is used to design optimized 8-bit parallel counter. Optimized counter consists of three modules. Module-1 is a standard parallel synchronous binary 2-bit counter, which is responsible for low-order bit counting and generating future states for all module-3's in the counting path by pipelining the enable for these future states through the state look-ahead path. Module-1 outputs Q1Q0 (the counter's two low-order bits) and QEN1= Q1 AND n Q0.Figure 2 shows the schematic of module-1 of proposed parallel counter.

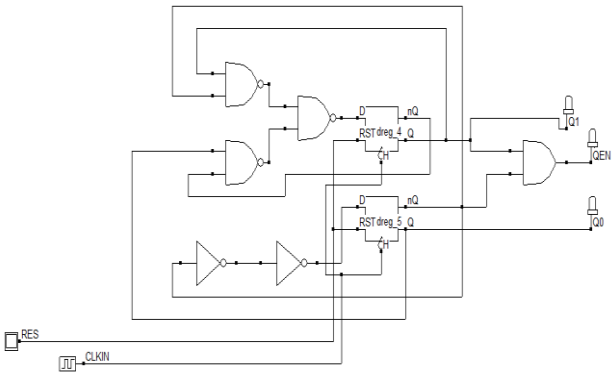

Fig 2: Schematic of Module-1 of Parallel Counter

Module 2s is a simple D latch. The placement of module-2s in the counting path is critical to the novelty of our counter structure. Module-2s in the counting path act as a pipeline between the module-1 and module-1 and between subsequent module-3s. Module-2 placement increases counter operating frequency by eliminating the lengthy AND-gate rippling and large AND gate fan-in and fan-out typically present in large width parallel counters. Module 3S is a parallel synchronous binary 2-bit counter whose count is enabled by INS. INS connects to the Q output of preceding module-2.schematic of module-3s is shown in figure 3.

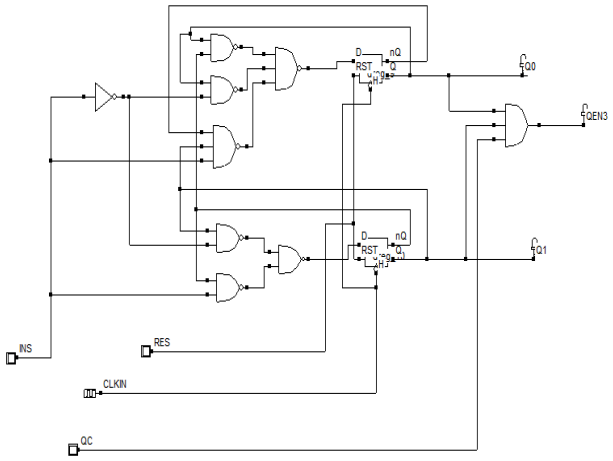

Fig 3:Schematic of Module-3S of Parallel counter

Figure 4 shows the optimized parallel counter with state look ahead mechanism and the flip-flops used in module-1 ,module-2S and module-3S are designed by using pass transistors it reduces area also (measured in number of transistor count). In this clock gating using AND gate technique is used. With clock gating clock is disabled during idle conditions in portion of circuit. This helps to reduce dynamic power consumption.

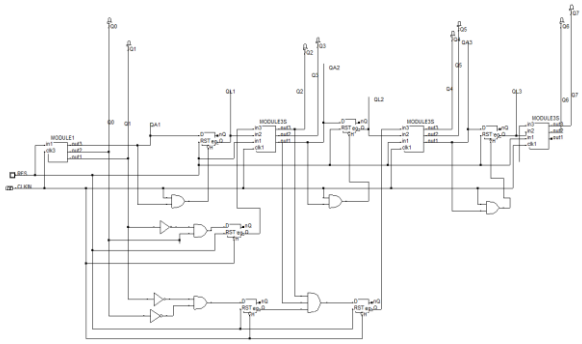

Fig 4: Schematic of Optimized 8-bit Parallel Counter

IV. TIMING AND LAYOUT SIMULATIONS

In this section, simulations of the proposed flip-flop and counter are shown. Simulations are obtained in Microwind Tool in 90nm technology at room temperature.Timing simulation of schematic shown is figure 1 is given below:

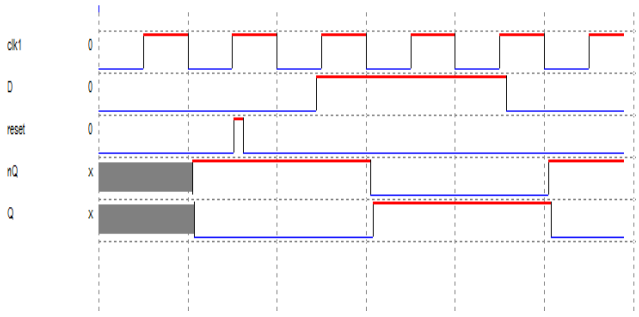

Fig 5: Timing simulation for D Flip Flop using Pass Transistors

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A pass transistor has been introduced at the place of NAND gates in D flip-flop to obtain the circuit shown in figure 2 .Layout design and simulation for the circuit is shown below in fig 6 and fig 7. There is considerable decrease in power consumption and area.

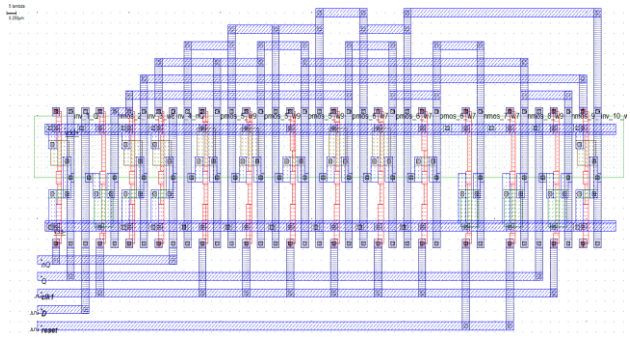

Fig 6: Layout Design for D Flip-flop using Pass Transistors

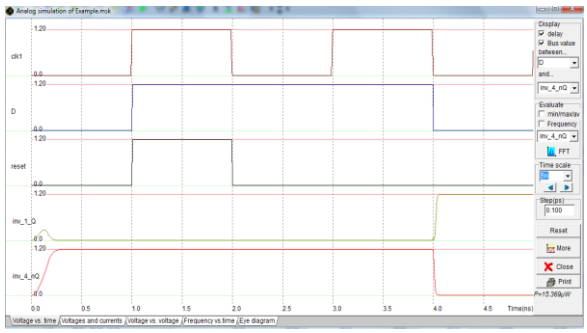

Fig 7: Simulations for D Flip-flop using Pass Transistor

Timing simulation of counter module1 is shown in fig 8 Layout of module-1 of proposed parallel counter is shown in fig 9.

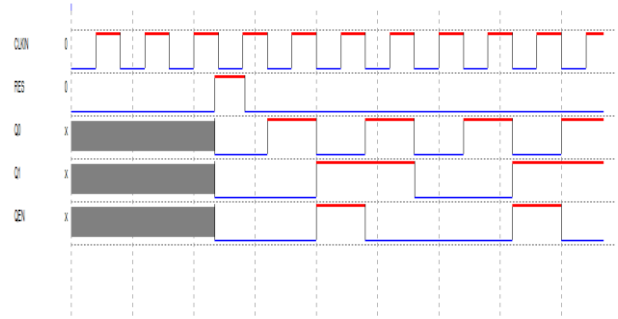

Fig 8: Timing simulation for Module-1 of proposed Parallel Counter

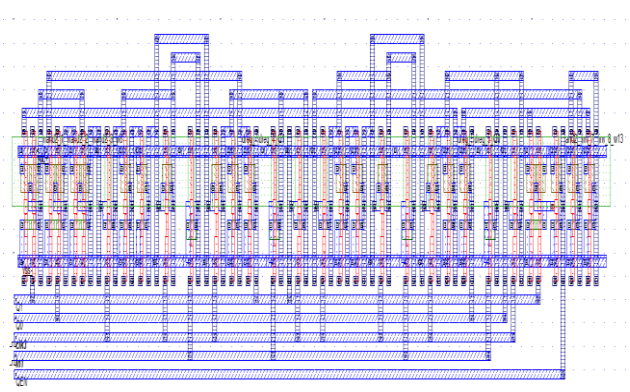

Fig 9: Layout Design for Module-1 of proposed Parallel Counter

Timing simulation of module 3s is shown in fig 10. After compiling the verilog file in Microwind3.1 layout generated is shown in fig 11.

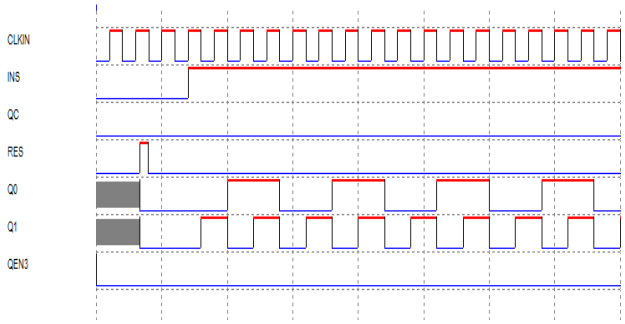

Fig 10: Timing simulation for Module-3S of proposed Parallel Counter

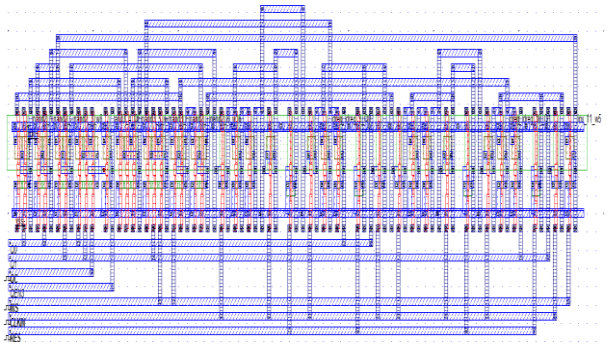

Fig 11: Layout Design for Module-3S of proposed Parallel Counter

Timing simulation and Layout design for the 8-bit optimized parallel counter is shown below in fig 12 and 13. Glitches are completely eliminated from the output. There is considerable decrease in power consumption and transistor count by using pass transistor D flip-flops in modules of counters instead of NAND gates. Layout simulation for the 8-bit Optimized parallel counter is shown below in fig 14. Clock gating technique is implemented in this to check the clock switching activity. Simulation for the circuit is obtained in 90nm technology at room temperature

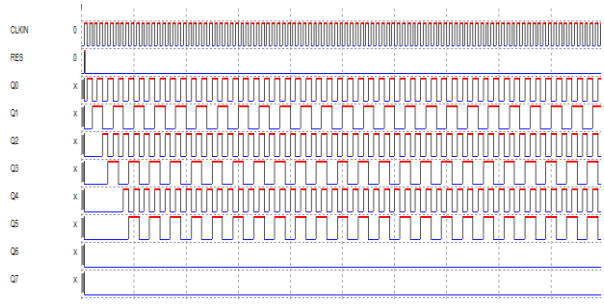

Fig 12: Timing simulation for of Optimized 8-bit Parallel Counter

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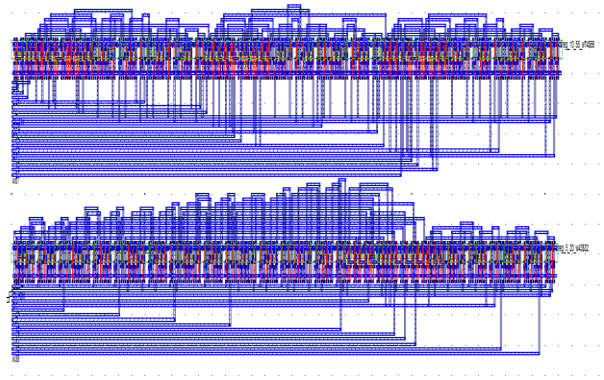

Fig 13: Layout Design for Optimized 8-bit Parallel Counter

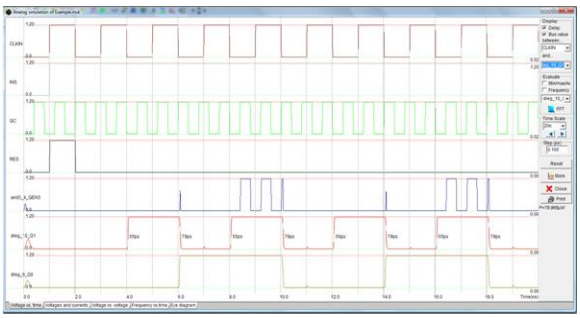

Fig 14: Simulations for Optimized 8-bit Parallel Counter

V. RESULTS AND COMPARISON

In this section, comparison among various D flip-flops has been shown in form of tables. Comparison between NAND Gate D flip-flop and optimized circuit with pass transistor (90 nm) for glitch elimination is given in Table 1. There is a reduction of about 59.4% in power in optimized circuit with pass transistor as compared to NAND gate circuit. This reduction in power has occurred because of the elimination of glitches, which consume dynamic power. Glitches are completely eliminated from the output of optimized circuit. Transistor count is also less.

Table 1 D Flip-flop in 90nm technology

Component	Area measured in terms of Transistor count	Power dissipation (µW)
NAND Gate	34	26.45 µW
Pass Transistor	14	10.72µW

Comparison of simulation results of proposed 8-bit parallel counter and previous counter designs are shown in table 5.2. Simulation for the circuit is obtained in 90nm technology at room temperature. Proposed parallel counter shows 66.04% power improvement as compared to Kakarountas counter and 54.3% power reduction as compared to Alioto's counter.Comparing Abdel's counter with proposed parallel counter shows 29.9% power reduction.Table 5.2 shows maximum operating frequency is also improved in proposed parallel counter.By using pass transistors drawback of large area in Abdel's counter is optimized in proposed circuit.So the proposed parallel 8-bit counter is optimized in terms of speed ,power and area as compared to previous counter designs.

Table 2 Comparison of Proposed Parallel Counter with previous work

	Power Consumption at Max Freq (mW)	Max. Freq. (GHz)	Area in no. of transistors
Kakarountas counter	28.64mW	0.5	286
Alioto's counter	21.3mW	0.46	160
Abdel's counter	13.89mW	2	510
Proposed parallel counter	9.726mW	2	388

VI. CONCLUSION

Dynamic power has become a serious concern in nanometre CMOS technologies. Dynamic and leakage power both are the main contributors to the total power consumption. With the continuous trend of technology scaling, dynamic power is becoming a main contributor to power consumption. In this paper, a technique named clock gating and SLA has been proposed which will reduce simultaneously both glitch and clock switching power. The results are simulated in Microwind3.1 in 90 nm technology at room temperature. the proposed parallel 8-bit counter is optimized in terms of speed, power and area as compared to previous counter designs.

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