International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-2 Issue-2, May 2013

2-Bit CMOS Comparator by Hybridizing PTL and Pseudo Logic

Vandana Choudhary, Rajesh Mehra

Abstract- In this paper an area and power efficient hybrid comparator is proposed by hybridizing PTL and Pseudo logic design. This hybrid comparator is proposed to improve area and power in 120 nm technology and compared with the previous work. To improve area and power minimum number of transistor logic is used in the proposed hybrid comparator. The proposed comparator has been designed and simulated using DSCH 3.1 and Microwind 3.1 on 120nm. Also the simulation of layout and parametric analysis has been done for the proposed comparator design. Power and current variation with respect to the supply voltage and temperature has been performed on BSIM-4 and LEVEL-3 on 120nm. Results show that area consumed by the proposed hybrid comparator is 40.99% on 120nm technology. At 1.2V input supply voltage the proposed adder has shown an improvement of 42.69% in power on BSIM-4 120nm technology

Keywords: Magnitude comparator; Binary Comparator; High speed; Low power; Hybrid PTL/PSEUDO NMOS logic

I. INTRODUCTION

In digital system the comparator is a very useful and basic arithmetic component of digital system. there are several approaches to designing CMOS comparator by flattering the logic function directly[1].This approach is only suitable for comparator with short input .For the comparator with longer inputs, circuit complexity increases drastically, and the operating speed is degraded accordingly. In the last few years, the design of high-speed, low power, and area-efficient binary comparators has received a great deal of attention, since, as is well known, comparison is a fundamental operation in almost all digital processors. Examples of efficient architectures of binary comparators are demonstrated in [2]–[6]. A magnitude comparator is a hardware electronic device that takes two number as input in binary form and determines whether one number is greater, less than or equal to the other number .An n bit magnitude comparator block is shown in fig.1. and compares two n bit binary numbers A and B and produces three outputs: GT (A>B), EQ (A=B) and LT (A<B).

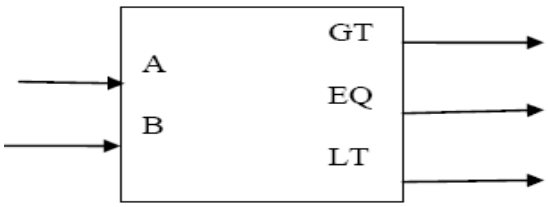

Fig.1 .A magnitude comparator

Revised Manuscript Received on 30 May 2013.
* Correspondence Author
Vandana Choudhary, M.E Student Department of ECE NITTTR, Chandigarh, India.
Rajesh Mehra, Associate Professor Department of ECE NITTTR, Chandigarh, India.

2-Bit Magnitude Comparator Compares two numbers each having two bits (A1, A0 & B1, and B0). For this arrangement truth table [7] has 4 inputs & 16 entries as in Table 1.

Table.1. Truth Table of 2-Bit Magnitude Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

II. COMPARATOR LOGIC STYLES

a. CMOS Logic Style b. Pseudo NMOS Logic
c. PTL Logic

A. *CMOS logic style*

Fig.2 (a) represents symbol of CMOS Inverter. It consists of one NMOS & one PMOS transistor. If input A=0 (logic low) then both gates are at zero potential & PMOS is ON & provide low impedance path from VDD to output (Y). Therefore output (Y) approaches to high level of VDD. If input A=1 (logic high) then both gates are at higher potential but NMOS is ON & provide low impedance path between ground & output (Y). Therefore, output (Y) approaches to low level of 0V. The substrate for the NMOS is always connected to ground, while the substrate for the PMOS is always connected to VDD, so it is ignored in the diagrams for simplicity

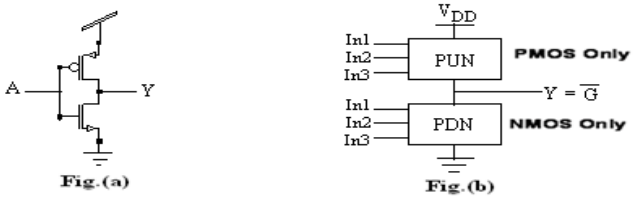

Fig.2. (a) Symbol of CMOS Inverter (b) Logic Network of CMOS Style

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

CMOS logic style is really extension of CMOS inverters to multiple inputs [8]. Logic network of CMOS style is shown in Fig.2 (b). The principle of CMOS logic design says that Pull up network has only PMOS circuitry & Pull down network has only NMOS circuitry. The function of PUN is to provide connection between output & VDD, similarly of PDN is to provide connection between output & GND. PUN and PDN networks are constructed in a fashion such that one & only one network is conducting at a time [9]. Number of transistors for N-input logic gate is 2N. Any logic function can be realized by NMOS pull-down and PMOS pull-up networks connected between the gate output and the power lines. Schematic of 2-bit magnitude comparator using CMOS logic style is given in Fig.4.

Design provides full output voltage swing between 0 and VDD. It provides high noise immunity because it has low sensitivity to noise. Provides high noise margin because VOH & VOL are nearly at VDD & GND, respectively. It is called Ratio less logic due to balanced device [10]. Design produces Large Power dissipation in comparison to remaining three logic styles. Design requires large number of transistors because for every input both (NMOS & PMOS) are used.

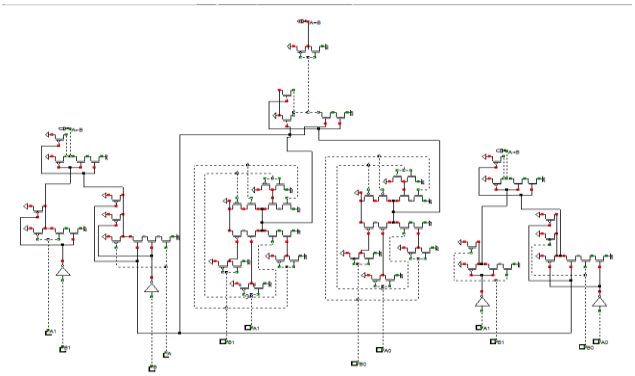

Fig.3.Schematic of 2-Bit Magnitude Comparator using CMOS Logic Style

In fig 4 the layout designs of the 2-bit comparator using CMOS logic style. layout is the general concept that describes the geo metric representation of the circuits by the means of layers and polygons. Different logical layers are used by the designer to generate the layout.

Fig.4. layout design of 2-bit Comparator using CMOS logic style

B. Pseudo NMOS logic style

In Pseudo NMOS logic style, single PMOS transistor is used in place of Pull-up network as a load with its gate terminal always connected to ground as in Fig.5. In this logic entire PUN is replaced with single load device that pulls up the output. Number of transistors for N-input logic gate is N+1. Pseudo NMOS logic style is used where majority of outputs are high, such as address decoder in memory & where speed is more important. Schematic of 2-bit magnitude comparator using pseudo NMOS logic style is given in Fig.7.

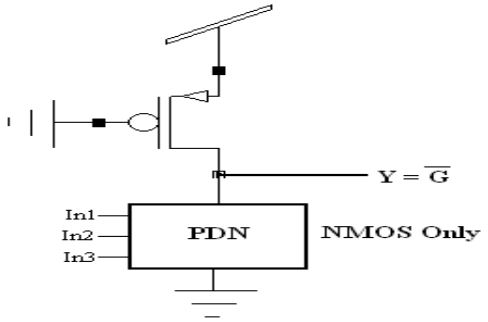

Fig.5. Logic Network of pseudo NMOS Style

Design requires less number of transistors than CMOS and TG styles. Speed is more because less number of transistors is used in design. Logic style reduces dynamic power by reducing capacitive loading.

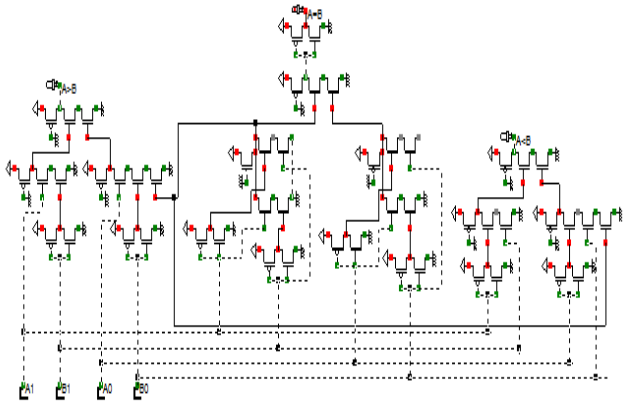

Fig.6. Schematic of 2-Bit Magnitude Comparator using Pseudo NMOS logic style

It does not provide full output voltage swing because PMOS is always ON by which output resistance is increased then always degraded output is obtained. Low noise margin. It produces non-zero static power dissipation due to always ON PMOS load device.

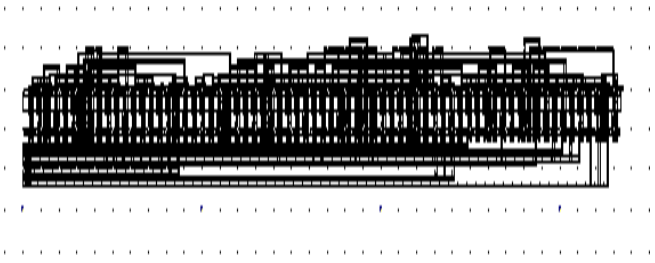

Fig.7. Layout Design of 2-Bit Magnitude Comparator using Pseudo NMOS logic style

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

C. PTL logic

Main idea behind PTL is to use purely NMOS Pass Transistors network for logic operation. The basic difference of pass-transistor logic style compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines as in Fig.8. In this design style, transistor acts as switch to pass logic levels from input to output [11]. Schematic of 2-bit magnitude comparator using pass transistor logic style is given in Fig 9

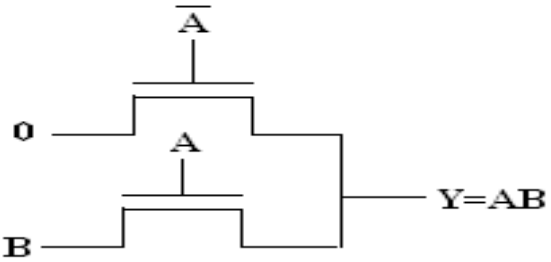

Fig.8. Symbol for AND Gate using Pass Transistor Logic

Design requires less number of transistors because one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation. Speed is increased because less number of transistors is used for design.
Less area is required for design because PMOS is not used.

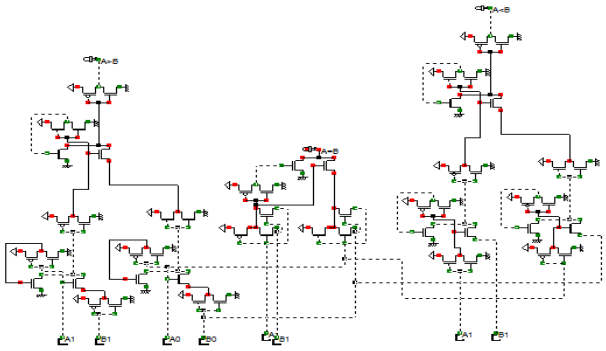

Fig.9. Schematic of 2-Bit Magnitude Comparator using Pass Transistor Logic Style

It does not provide full output voltage swing because PMOS is not used. Design produces threshold loss because it uses only NMOS transistors to pass both Low & High (0 & 1) inputs.

Figure.10. Layout Design of 2-bit magnitude Comparator using Pass Transistor Logic

III. HYBRID COMPARATOR SCHEMATIC

PTL has some advantage over static CMOS that it has the capability to implement a logic function with smaller number of transistor, smaller area and less power consumption. For full swing output level-restoring logics will slow down the PTL circuits and increase the power dissipation as well. Pseudo NMOS logic style is used where majority of output are high, such as where speed is more important. Schematic of 2-bit magnitude comparator using hybrid logic style is given in Fig.11.

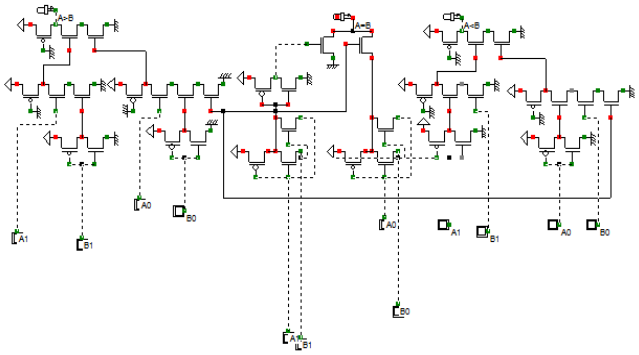

Fig.11. Schematic of proposed 2-Bit Magnitude Comparator using Hybrid logic style

It requires less number of transistors than other logic style. Speed is more because less number of transistor are used in this design. Less area is required for this design. Less power is consumed It does not provide full output voltage swing. Design produces threshold loss.

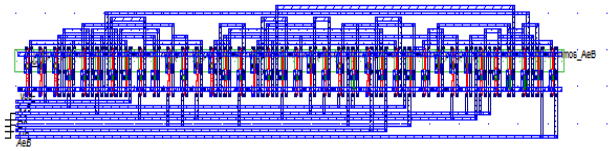

Fig.12.Layout Design of proposed hybrid comparator

In fig.14. The simulation waveform for the proposed circuit is shown. The waveform is produced voltage versus time.The voltage amplitude taken in this work is 1.2V.the simulated waveform of the proposed hybrid comparator is shown below.

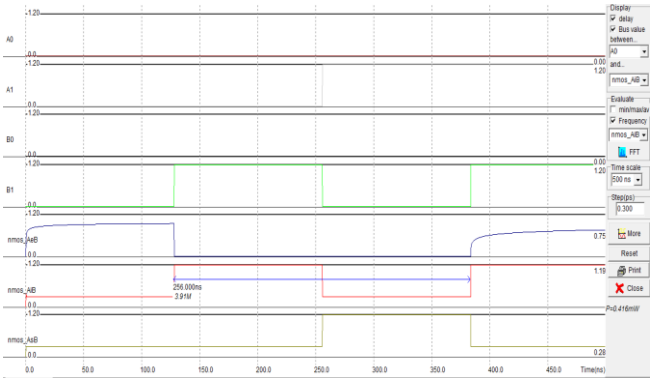

Fig.13. Simulation Waveform of Proposed Hybrid Comparator

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

IV. ANALYSIS AND ANALYSIS

In this section, simulations of the proposed methods Comparisons between hybrid and other logic circuit are shown in tabular form. Simulations are obtained in Microwind Tool. First step in obtaining the simulations is to compile the Verilog file in Microwind 3.1. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Microwind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Microwind. After that simulations are performed on the layout generated using Verilog files. The results are simulated at room temperature. Simulation and Measurement Results of hybrid comparator with different logic style is shown in Table 2.

Table 2 Simulation and Measurement Results of hybrid comparator with different logic style

	Pseudo-logic	CMOS Logic	PTL Logic	Hybrid Logic
NMOS Devices	66/2000	24/2000	35/2000	25/2000
PMOS Devices	34/2000	24/2000	19/2000	13/2000
Electrical Nodes	70/3000	30/3000	33/3000	30/3000
Compiled Cell	51/51	48/48	54/54	38/38
Routed Wires	104	134	98	63
Power(mw)	6.59	1.760	0.766	0.416
Area(μm²)	2253.7	1131.4	1021.2	602.6

V. CONCLUSION

After simulation of all four designs final results are obtained for Power Consumption & Area. PTL Logic Style provides low power design as compared to other Logic Style. Pseudo NMOS logic style provides less delay as compared to other logic style. PTL Logic Style provides less PDP as compared to other logic style. It has been found that transistor count is less in PTL style design than that of other logic style design. An important factor, output voltage swing is better in CMOS logic style design & Transmission Gate design. But Transmission Gate logic style requires transistor count more than CMOS design style. Pseudo NMOS logic style and PTL style do not provide full output voltage swing. A hybrid comparator has been presented in this brief. By using the proposed architecture the power is reduced up to 0.439mw and area is reduced up to 602.6 μm² than the other logic styles.

REFERENCES

1. M. M. Mano(1991), *Digital Design*. Englewood Cliffs, NJ: Prentice-Hall, ch. 5.
2. N. West and K. Eshraghian(1993), *Principles of CMOS VLSI Design*. Reading, MA: Addison-Wesley, ch. 8.
3. C.-C. Wang, C.-F. Wu and K.-C. Tsai(1998), "1-GHz 64-b high-speed comparator using ANT dynamic logic with two- phase clocking," *Proc. Inst.Elect. Eng. Comput. Digital Techn.*, vol. 145, no. 6, pp. 433–436.
4. R. X. Gu and M. I. Elmasry(1996), "All-N-Logic high-speed true-single-phasedynamic CMOS logic," *IEEE J. Solid- State Circuits*, vol. 31, pp.221–229, Feb.
5. S. Furber(1997), *ARM System Architecture*. Reading, MA: Addison-Wesley.
6. J.-S. Wang and C.-H. Huang(2000), "High-speed and low-power CMOS priorityencoders," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1511–1514.
7. S. Kang and Y. Leblebici(2003), "*CMOS Digital Integrated Circuit, Analysis and Design*" (Tata McGraw-Hill).
8. M.Morris Mano(2002) "*Digital Design*" (Pearson Education Asia. 3rd Ed).
9. A. Bellaouar and Mohamed I. Elmasry(1995), "*Low Power Digital VLSI Design: Circuits and Systems*" (Kluwer Academic Publishers, 2nd Ed).
10. Anantha P. Chandrakasan and Robert W. Brodersen(2009), "Minimizing Power Consumption in CMOS circuits". Department of EECS, University of California, pp.1-64.
11. S. Salivahanan and S. Arivazhagan (2004)"*Digital Circuits and Design*" (2nd Ed).
12. Dinesh Sharma, Microelectronics group(2010), EE Department IIT Bombay, "Logic Design",*pp.1-34*
13. N. Weste and K. Eshraghian(1993) "*Principles of CMOS VLSI Design: A system Perspective*" (Addison- Wesley, 2nd Ed).
14. John P. Uyemura(2002) "*Introduction to VLSI Circuit and Systems*" (John Wiley India, ISBN: 978-81-265-0915-7).
15. R. Zimmermann and W. Fichtner(1997), "Low Power Logic Styles: CMOS Versus Pass Transistor Logic" *IEEE Journal of Solid State Circuits, Vol.32, No.7, pp1079-1090*.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)