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Design and Analysis of 8-bit Low Power Parallel Prefix VLSI Adder

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Abstract*— The binary adder is the critical element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. As such, extensive research continues to be focused on improving the power delay performance of the adder. High speed and low power Arithmetic units are required for applications of digital signal processing like Fast Fourier Transform, Finite Impulse Response filters, convolution etc. The present work focused on designing of high performance low power 8-bit parallel prefix adder structure. For improving the speed and to reduce the power, we have reduced the static power and dynamic power. The design is simulated using Xilinx 13.2 ISE and implemented on Spartan 3 FPGA Board.

Index Terms*—Parallel Prefix Adder, Propagation signal, Power, Delay.

I. INTRODUCTION

The arithmetic operations of two binary numbers are one of the most interesting problems in modern digital VLSI systems consuming a major design effort of digital signal processors and general purpose microprocessors. The high-operation speed and the excessive activity of the adder circuits in modern microprocessors, not only lead to high power consumption, but also create thermal hotspots that can severely affect circuit reliability and increase cooling costs. The presence of multiple execution engines in current processors further aggravates the problem. Therefore, there is a strong need for designing power-efficient adders that would also satisfy the tight constraints of high-speed. The design of high-speed, low-power and area efficient binary adders always receives a great deal of attention. Among the hundreds adder architectures known in the literature, when high performances are mandatory, parallel prefix trees are generally preferable. [1]

There are three performance parameters on which a VLSI designer has to optimize their design i.e. Area, Speed and Power. The design of faster, smaller and more efficient adder architecture has been the focus of many research efforts.

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(i) Low power dissipation has become a major issue demanded by the high performance processor market in order to meet the high density requirements of advanced VLSI processors. The importance of low power is also evident in portable and aerospace applications, and is related to issues of reliability, packaging, cooling and cost [2]. Another important reason for low-power circuit design is its reliability. The present work comprises of designing low power high speed adder architectures. The paper is organized as follows: Section II discusses on the notion of Sources of Power Consumption in CMOS. Section III deals with the Parallel Prefix Problem. Section IV focuses on the design methodology of the parallel prefix adder structure that is typically used to speed up the addition process. Section V presents the simulation results of the parallel prefix adder.

II. SOURCES OF POWER CONSUMPTION IN CMOS

To measure the power consumption in CMOS circuits, the sources of power consumption should be known. Figure 1 represents the sources of power consumed in a CMOS circuit. It indicates, the major part of the power consumption is active and standby powers. The power consists of two components, capacitive or dynamic power and short circuit power [3] [6].

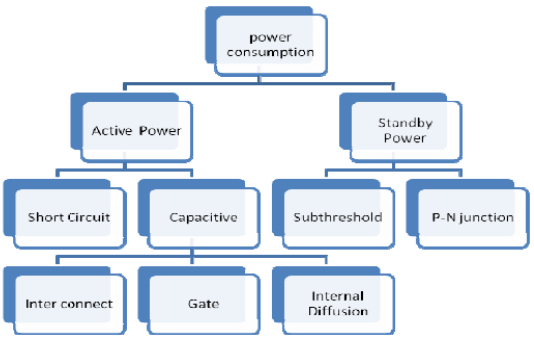

Fig. 1: Sources of Power Consumption in CMOS

This paper addresses the design and analysis of low power parallel prefix adders. Si Cadence tools are used to analyze CMOS circuits, simulators give average power alone.

III. THE PARALLEL PREFIX PROBLEM

The carry look ahead and the tree adder architectures can be represented by a parallel prefix adder structure consisting of three main parts: preprocessing, carry look ahead network and post processing.

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Let us consider two binary input vectors A and B, the preprocessing logic extract two special signals – propagate (P) and generate (G). The generate signal is high when a carry is generated at any stage. The propagate signal is high when there is a carry from a previous stage and the carry will be propagated into the next stage. The carry propagation problem can be expressed in terms of a prefix problem where for a set of binary inputs (xi: i=0, 1, 2,…., n) the outputs (yi: i=0, 1, 2, …., n) are defined by the help of an associative binary operator • as:

$y_0 = x_0$

$y_i = x_i \bullet y_{i-1}$

$y_i = x_i \bullet x_{i-1} \bullet x_{i-2} \bullet x_{i-3} \bullet \ldots\ldots\ldots\ldots \bullet x_0$ (1)

Since the • operator is associative, it can be grouped in any order and computed in a number of levels.

$$(G,P)_{i:i}^{0} = (g_i, p_i) \quad (2)$$

$$(G,P)_{i:j}^{k} = (G,P)_{i:q+=1}^{k-1}(G,P)_{q:j}^{k-1} \quad (3)$$

Where the desired

$Carry_i = G_{i:0}$

regardless of the number of levels necessary to cover the range i:0. Depending on the algorithm the carry propagation will have a different structure and shape. The maximum number of levels required to calculate the final Carry signal is referred to as the depth of the prefix graph is equal to the number of logic levels in the network. The depth of the carry propagate network is a function of the bit-width of the input. This number relates approximately to the delay of the network. The total numbers of binary associative operations within the network determine the active area required to compute the result. Secondary effects like the number of times a sub range is used in subsequent operations (fan out) and the distance between operators of an operation also contribute to the overall performance of the system [4].

IV. DESIGN METHODOLGY

In the parallel prefix addition, to carry out addition and to obtain the final summation and final carry following steps should be followed

1. Arrange the two operands in the array form.
2. In Pre-computation stage, Compute Propagation signal and Group Propagation signals for all the bits of operands using following relation.
   P[i] = a[i] ^ b[i]
3. In the look ahead stage, Generate the initial carry using multiplexer by choosing corresponding propagation signal as the selection, present operand bit and initial carry input as its stimulus for multiplexer.
4. Compute the next significant carry bits using the composite function of all present, previous propagation signals and the operands.
5. In the post computation stage, generate final summation bits using XOR operation of propagation signal and corresponding previous carry bit.

Figure 2 shows the methodology of the Parallel prefix adder.

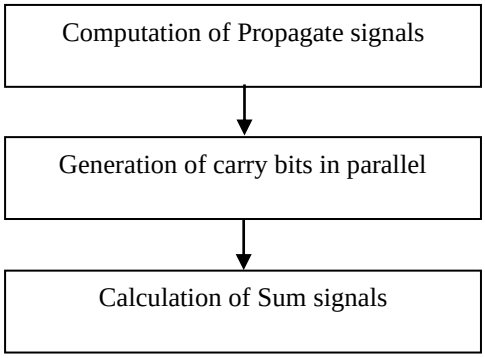

Fig. 2 Methodology of Parallel Prefix Adder

V. IMPLEMENTATION

The programming environment for implementing the circuit is based on Verilog HDL. In implementation of this design, Prefix adder is designed for 8-bits using structural style of modeling and is implemented, tested on the Spartan-3 FPGA board. In structural modeling, adder is divided into 3 sections i.e. upper, middle and lower sections. Where, all the three sections operate on the data simultaneously. Multiplexer, XOR gates and AND gates are basic building blocks of the adder. The 8-bit adder is divided into two 4-bit adders. Each 4-bit adder has 7 multiplexers, 4 2-input AND gates and 8 2-input XOR gates associated. The entity part or the peripheral view of the adder is given in Fig. 3.

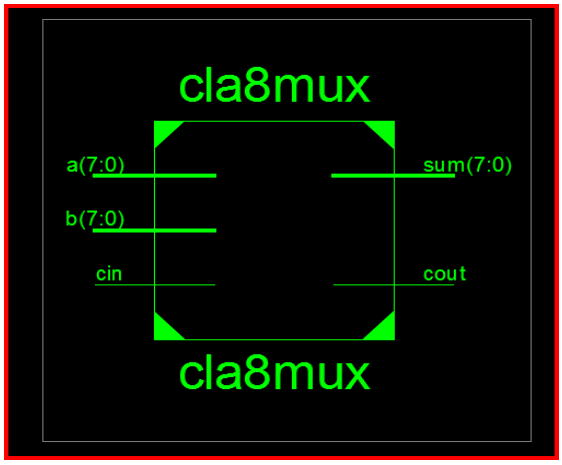

Fig. 3 Entity view of Adder.

Table 1 shows the device utilization summary obtained from the synthesis report of structural modeling of the adder. By analyzing the synthesis results there is drastic reduction of resources of FPGA when modeled and power consumption is also reduced to a greater extent.

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Because of this implementation, system requires very less space while designing hardware and eliminates the complexity in hardware design.

Table 1

Specifications	Used	Available	Utilization
Number of slice LUTs	15	9112	1%
Number of occupied slices	7	2,278	1%
Number with an unused Flip-Flop	15	15	100%
Number of Bonded IOBs	26	232	11%

The power of presented parallel prefix adder is estimated using X-Power estimator Spartan3_XPE_11_1.xls. Table 2 shows the delay and power estimations of the adder.

Table 2

Specifications	Delay	Power	Power-Delay Product
Result	8.459ns	24mW	0.203n

.

Simulation results are as shown in the Fig.4 for inputs
a = 8'b11000101
b = 8'b00101001
cin = 1;
and the outputs obtained are
sum = 11101111 and
cout = 0.

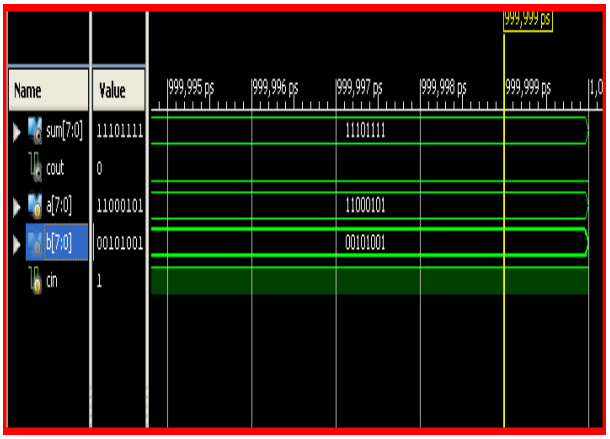

Fig.4 Simulation results of Adder

Fig.5 shows the RTL schematic of the 8-bit Parallel Prefix Adder obtained by using structural style of modeling.

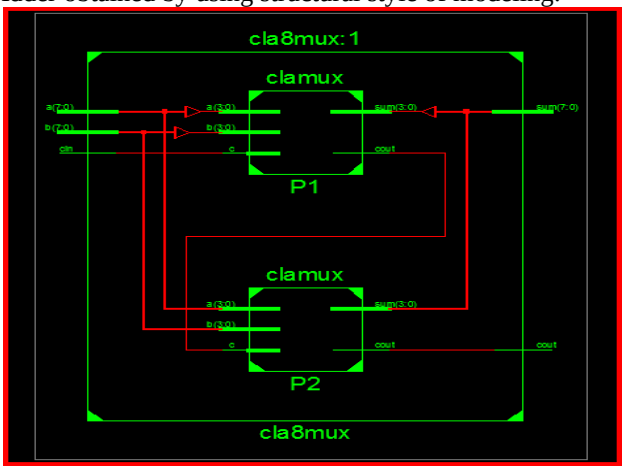

Fig. 5 RTL schematic of adder.

Fig.6 shows internal RTL schematic of the adder.

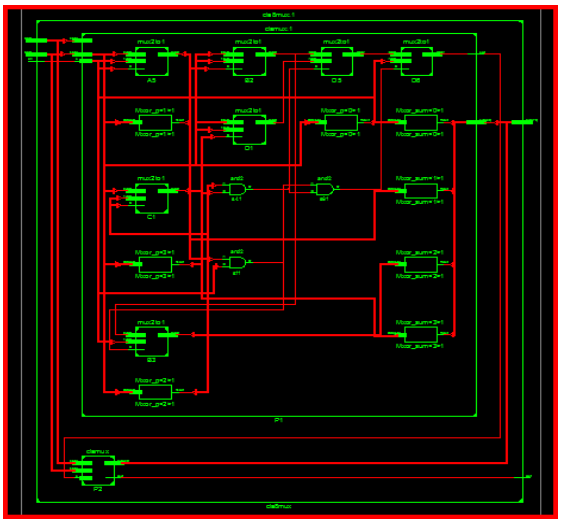

Fig.6 Internal Schematic of the 4-bit adder.

VI. CONCLUSION

The present work comprises of design of low power 8-bit Parallel Prefix Adder carried out at frequency of 200.00 MHz and the proposed design is optimized using structural style of modeling style. The designed circuit has been simulated using Xilinx ISE 13.2 and implemented on FPGA. With significance of implementation of design using only propagation signals and the usage of multiplexers leads to large reduction in power and delay. The power is estimated using X-Power Tool Spartan3_XPE_11_1.xls at voltage levels of 1.14V and 2.375V giving more optimized outcomes. The static power is 22mW while dynamic is 2mW. Hence, the implemented design greatly reduces the static and dynamic power consumption.

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