International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-2 Issue-1, March 2013

Design of Low Power Sram Memory Using 8t Sram Cell

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Abstract-Low power design has become the major challenge of present chip designs as leakage power has been rising with scaling of technologies. As modern technology is spreading fast, it is very important to design low power, high performance, and fast responding SRAM (Static Random Access Memory) since they are critical component in high performance processors. The Conventional 6T SRAM cell is very much prone to noise during read operation. To overcome the problems in 6T SRAM cell, researchers have proposed different SRAM topologies such as 8T, 9T, 10T etc. bitcell design. These designs can improve the cell stability but suffer from bitline leakage noise. In this paper, an SRAM memory has been designed to overcome power consumption problem. It also improves the Cell stability by increasing the Read Static-Noise-Margin.

Keywords- CMOS logic, SRAM, VLSI, Read-Static Noise Margin (SNM), Stability and Power Consumption.

I. INTRODUCTION

The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System-On-Chip and high performance VLSI circuits. Due to the need of battery operated device, the scaling in CMOS technology continues. Nanoscale CMOS SRAM memory design faces several challenges like reducing noise margins and increasing varia9bility, due to the continuous technology scaling. In SRAM the data is lost when the memory is not electrically powered. Advances in chip design using CMOS technology have made possible the design of chips for higher integration, faster performance, and lower power consumption. To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to smaller dimensions over the last few years. Power consumption of SRAMs account for a significant portion of the overall chip power consumption and due to high density, low power operation is a feature that has become a necessity in today's microprocessors. Hence, power consumption of SRAM modules must be reduced and has been under extensive investigation in the technical literature. The most effective approaches to meet this objective are to design SRAM cells whose operation is ultra-low power. Recent published works have shown that the Conventional 6T SRAM suffers severe stability degradation due to access disturbance at low–power mode [1]. The goal of this paper is to design a single 8T SRAM memory so that the Read stability can be improved by improving the Read Static-Noise-Margin and also tries to reduce Power Consumption and thus can design an SRAM memory in 45nm process technology [2].

Revised Manuscript Received on 30 March 2013.
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II. CONVENTIONAL 6T SRAM CELL

The conventional 6T memory cell comprised of two CMOS invertors cross coupled with two pass transistors connected to a complimentary bit lines as shown in Figure 1. The gate of access transistors N3 and N4 are connected to the WL (word line) to have data written to the memory cell or read from the memory cell through the BL or BLB (bitlines) during write and read operation.
The bit lines act as I/O buses which carry the data from the memory cell to the sense amplifier. Although it is not necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. SRAM cell perform three different operations, read, write and hold operation.

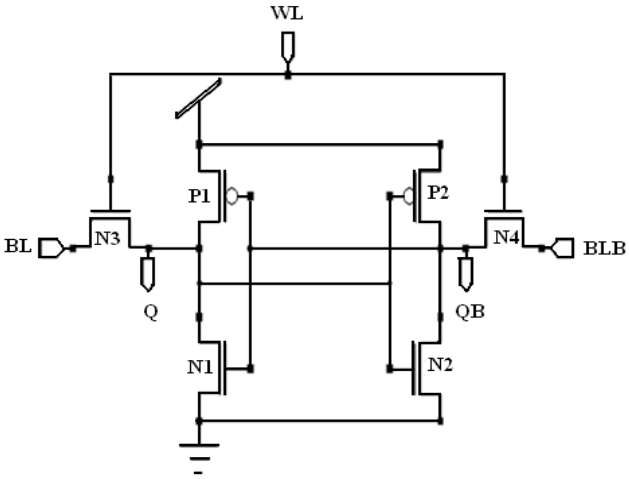

Figure 1. Conventional 6T SRAM Cell

III. STATIC-NOISE-MARGIN (SNM)

The stability of SRAM circuit depends on the Static Noise Margin. A basic SNM is obtained by drawing and mirroring the inverter characteristics and finding the maximum possible square between them. This is a graphical technique of estimating the SNM.

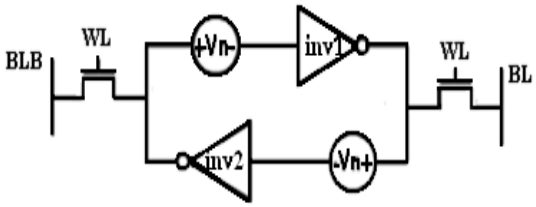

Figure 2. The standard setup for SNM definition [6]

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Figure 2 shows a common way of representing the SNM graphically for a bit-cell holding data. It plots the Voltage Transfer Characteristic (VTC) of Inverter 2 (inv2) and the inverse VTC-1 from Inverter 1(inv1). The resulting two-lobed curve is called a "butterfly curve" and is used to determine the SNM [2]. The SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve.

Consider the case when the value of the noise sources with value Vn are introduced at each of the internal nodes in the bit cell. When the value of Vn increases from 0, this causes the VTC-1 for first inverter in Figure 2 to move downward and the VTC for the second inverter to move to the right [3]. The resulting two-lobed curve is called as a "butterfly curve" as shown in Figure 3 and is used to determine the SNM. Values of SNM vary in different operation mode. SNM is becoming important factor to check the stability during read operation. It's visible in the Figure 3 that during read operation, the SNM takes its lowest value and the cell is in its weakest state.

The SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell [4][5]. Any change in the noise, changes the value of the SNM during cell operation. Though the SNM is important during hold, cell stability during active operation represents a more significant limitation to SRAM operation.

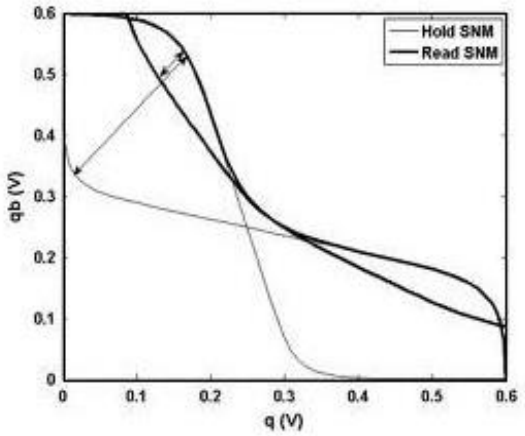

Figure 3. General SNM characteristics during Standby and Read operation

3.1. READ STATIC-NOISE-MARGIN

The cell is most vulnerable when accessed during a read operation because it must retain its state in the presence of the bitline precharge voltage [7].

If the cell is not designed properly, it may change its state during a read cycle which results in either a wrong data being read or a destructive read where the cell changes state. Thus, the worst noise margin is obtained during read access. Figure 4 shows the equivalent circuit during read operation.

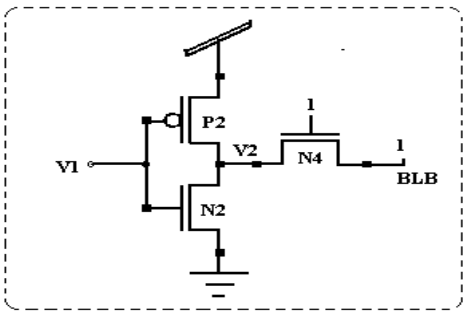

Figure 4. Circuit used to measure read noise margin

The SNM is calculated when the word line is set high and both bit line are still precharged high. At the start of read access, the bit lines are precharged to V_{dd} and then the wordlines are activated to access the cell. The node having the '0' data pulls one of the bitlines to GND causing a voltage swing which is read by sensing circuits.

The internal node of the bit-cell representing a zero gets pulled upward through the access transistor due to the voltage dividing effect across the access transistor and drive transistor. This increase in voltage severely degrades the SNM during the read operation.

The circuit for measuring the read margin is shown in Figure 4. One of the inverters is used and the bitline is connected to V_{dd} to simulate a read operation. A DC voltage sweep is applied at node V1and the voltage at node V2 is measured to obtain the VTC.

IV. PROBLEMS IN 6T SRAM CELL

The conventional 6T-cell schematic is shown in Figure 5. This most commonly used SRAM cell implementation has the advantage of very less area [8].

However, the potential stability problem of this design arises during read and writes operation, where the cell is most vulnerable towards noise and thus the stability of the cell is affected. If the cell structure is not designed properly, it may change its state during read and write operation [9]. There are two types of noise margin which affects the Cell stability that are discussed shortly.

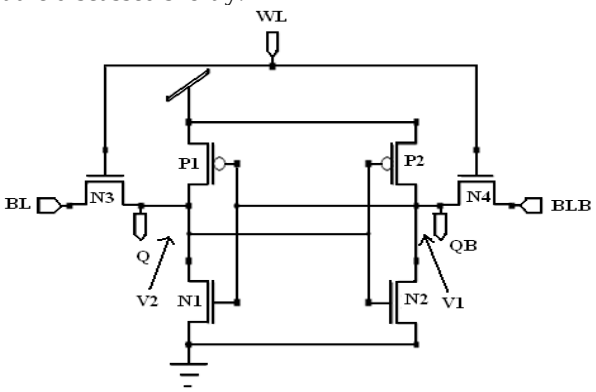

Figure 5. Voltage Stability Problem of 6T SRAM Cell

During the read operation, a stored "0" can be overwritten by a "1" when the voltage at node V1 reaches the V_{th} of nMOS N1 to pull node V2 down to "0" and in turn pull node V1 up even further to "1" due to the mechanism of positive feedback. This results in wrong data being read or a destructive read when the cell changes state [10].

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V. EXISTING 8T SRAM CELL

With the aggressive scaling in technology, substantial problems have been encountered when the conventional 6T (six transistors) SRAM cell configuration is utilized. This cell shows poor stability at very small feature sizes, the hold and read static noise margins are small for robust operation. Therefore, an extensive literature can be found on designing SRAM cells for low power operation in the deep sub-micron/nano ranges. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. An 8T cell can be found to solve the problem. This cell employs two more transistors to access the read bitline. The transistor configuration (i.e. M1 through M6) is identical to a conventional 6T SRAM cell. Two additional transistors M7 and M8 (thus yielding an 8T cell design) are employed in to reduce the leakage current.

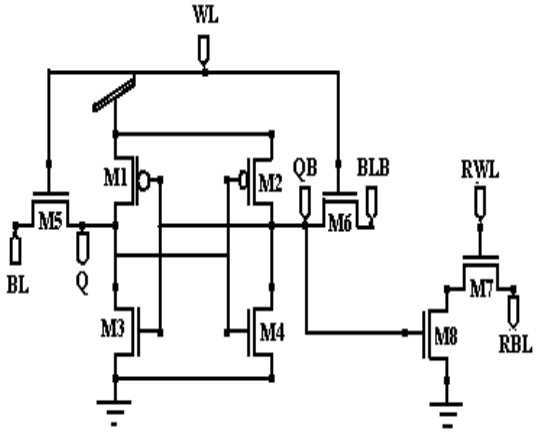

Figure 6. Existing 8T SRAM Cell

To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was proposed [11], for which separate read/write bit and word signal lines are used as shown in Figure 6, to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation.

Write access to the cell occurs through the write access transistors and from the write bitlines, BL and BLB. Read access to the cell is through the read access transistor and controlled by the read wordline, RWL. The read bitline, RBL, is precharged prior to the read access. The wordline for read is also distinct from the write wordline. By doing this the worse-case stability condition encountered previously in a 6T SRAM cell, is avoided and high read stability is retained.

However, for the 8T structure, the read bitline leakage is greater, especially in deep submicron/nano ranges. When the column for Read (RBL) is not accessed, the leakage current through M7 may cause a severe voltage drop at the read bitline, leading to large Power dissipation, thus error may appear at the output.

VI. SINGLE ENDED 8T SRAM CELL

In this paper the existing 8T SRAM Cell is being compared with the single ended 8T SRAM design as shown in Figure 7 that enhances data stability by improving the Read Static Noise Margin and also reduces the Power Consumption. In this design, a transmission gate is used for Read purpose. The additional signal RWLB is an inversion signal of read wordline (RWL). It controls the additional transistor M7 of the transmission gate. While the RWL and RWLB are asserted and once the transmission gate is ON, a stored node is connected to RBL. Thus a stored value at Q is being transferred to or read through RBL.

One of the major advantages of this design is that it is not necessary to prepare a precharge circuit as required in prior 8T SRAM cell and a sense amplifier circuit as required in 6T SRAM cell because the stored value is directly passed through transmission gate. A charge/discharge power on the RBL is consumed only when the RBL is changed. Consequently, no power is dissipated on the RBL if an upcoming data is the same as the previous state. The design reduces a bitline power in both cases that the consecutive "0"s and consecutive "1"s are read out.

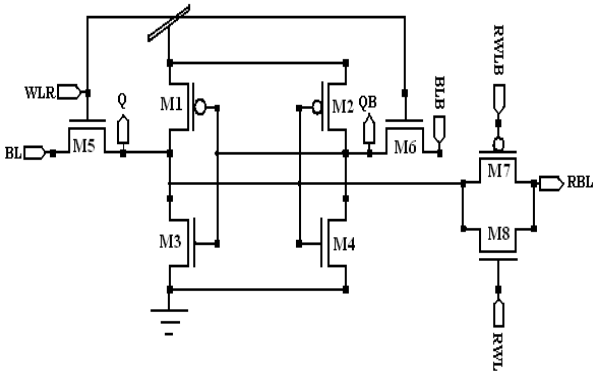

Figure 7. Single Ended 8T SRAM Cell

VII. SRAM MEMORY SYSTEM FOR WRITING AND READING DATA BIT

The single ended 8T SRAM circuitry is being used for making an SRAM memory since the usage of SRAM Cell is in cache memory. For generating a memory, there is a requirement of Address decoder, Data write circuitry and data Read Operation. Since the proposed circuitry do not require precharge circuit, so there is no elaboration of precharge circuitry as in 6T SRAM Cell. The memory has been designed for 32 bit storing capacity for read and writes operation. At a time, 8 bits will be activated for read or write purpose. The selection of wordline represents the selection of a particular row. The data lines of the cells form the column of the memory matrix. For read operation, the Read Bitline (RBL) is also included to form a separate read column of the memory matrix. The data flow is thus visualized to be vertical for both read and write operations. Once a wordline is driven high by the row decoder, every cell in the row is accessible. The memory Cell design of existing 8T and Single Ended 8T SRAM is shown in Figure 8 and Figure 9.

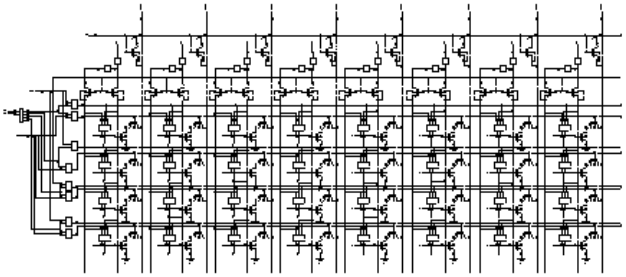

Figure 8. Schematic diagram of (4×8) existing 8T Memory system

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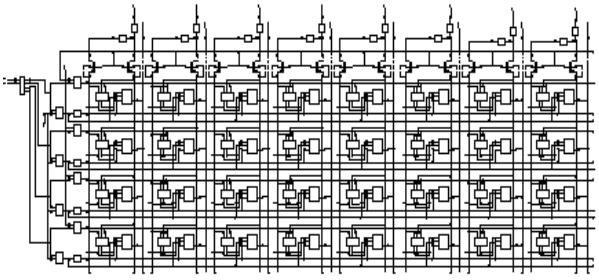

Figure 9. Schematic diagram of (4×8) Single Ended 8T Memory system

7.1. PERIPHERAL CIRCUITS

The peripheral circuits of SRAM memory includes Address decoder, Data write circuitary and data Read Operation which are as follows.

7.1.1. Address Decoder

The proposed design SRAM memory system has storage capacity of 4 words of 8 bits each. To address these words in a unique manner a 2:4 row decoder are used. A 2:4 decoder is an elementary row decoder given in [12] designed to select one of the 2^N wordlines by raising its voltage to V_{OH}. It has 2 input and 4 output lines. This address can accept addresses ranging from 00 to 11. According to the address input, the address decoder activates one of the rows by asserting one of the wordlines and all the other word address line remains low. Figure 10 shows the selection of particular row by providing inputs to the address lines A1 and A2.

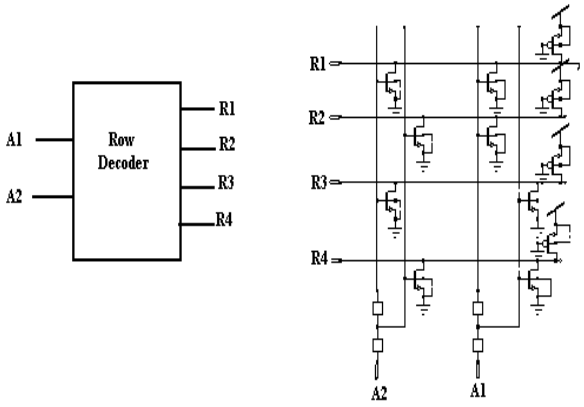

Figure 10.Row decoder circuit for 2 address bits and 4 word lines.

7.1.2. Data Write Circuitry

The write circuitry contains d_7, d_6, d_5.....d_1 data lines with its inverted inputs which are buffered to provide complimentary pairs (d_i,d_{ibar}). Two control bits have been included in the design WEN and RWL. The WEN (write enable) signal which is enabled only when data is written into the memory. The WEN signal and the particular row decoder is being provided with an AND operation and then passed into the memory design, so that the data can be written into a particular row. When the right enable control bit has a value WEN=1,the n MOS act as close switches connecting the data pairs to the bit and bit-bar colons. Every bit pair is fed to the appropriate location that defines the 8 bit column groups.

7.1.3. Data Read Operation

The data written into the SRAM cell is retained as long as the power is present. When the memory is idle i.e., when the memory words are not accessed, then the value of the stored bit remains intact within the node Q and QB. During read operations the control signal RWL is performed an AND operation with the particular selected row through row decoder from where the data is to be read. The respective RWL is being applied to the nMOS of the transmission gate and the inverse of RWL i.e., RWLB is applied to pMOS of transmission gate. When RWL becomes 1 then its inverse RWLB become 0, thus the input of transmission gate is in the ON state. The value stored in the respective node Q is being passed to RBL column and thus the stored data is being read.

VIII. SIMULATION RESULTS

All simulations have been performed on Tanner EDA tool version 12.6 using 45nm technology with input voltage ranging from 0.6V to 1V in steps of 0.2 V. In order to prove that proposed design shows better performance for Read-SNM and Power Consumption, simulations are carried out for different voltages. To establish an impartial testing environment both circuits have been tested on the same input patterns which covers all the combination of input stream.

8.1. READ-SNM ANALYSIS

The Read-SNM of the existing and the proposed 8T has been simulated for various Input voltages. The effect of Power Supply Voltage is important parameter which changes the cell stability during read mode and has been widely acceptable. It is preferable that the supply voltage must be maximum for increase SNM and also for cell stability.

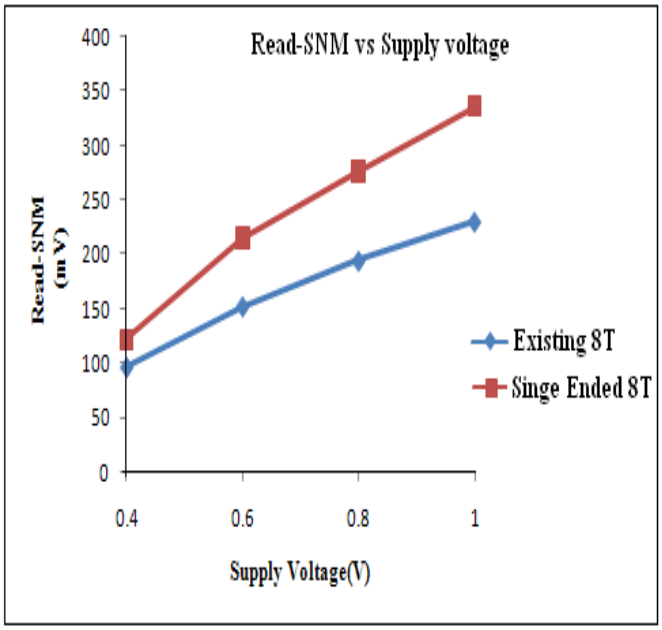

Figure 11. Read SNM vs. Power supply voltage of Existing and Single Ended 8T SRAM Cell

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For this analysis, the supply voltage is varied from 0.4V to 1V. The noise margin for all operation is proportional to the supply voltage. The Read-SNM of the proposed 8T single bit SRAM Cell is higher than the existing 8T single bit SRAM Cell as shown by the Figure 11.

8.2. POWER CONSUMPTION ANALYSIS

The existing and Single Ended 8T have been simulated and checked at various voltages for Power Consumption. Table 1 show that the power consumption of the single ended SRAM Cell design increases with increasing supply voltage from 0.6V to 1V. The Single Ended 8T design of the SRAM Cell has remarkably less power consumption compared to the existing 8T SRAM design at various input voltages. Table 2 shows variation of power consumption for existing and Single Ended 8T (4×8) SRAM memory design. It is clear from Table 2 that Single Ended 8T SRAM memory design consumes less power than existing 8T SRAM memory design.

Table 1. Power consumption vs. Supply voltage of existing and proposed 8T for single bit SRAM Cell.

Different SRAM Cells	Power Consumption (uW)		
	0.6v	**0.8v**	**1v**
Existing 8T	0.20	0.76	1.57
Single Ended 8T	0.078	0.24	0.43

Table 2. Power consumption vs. Supply voltage of existing and proposed 8T for (4×8) SRAM memory.

Different SRAM Memory Cells	Power Consumption (uW)		
	0.6v	**0.8v**	**1v**
Existing 8T	60.99	113.52	211.21
Single Ended 8T	52.37	88.75	187.44

IX. ONCLUSIONS

The design and implementation of the SRAM memory is shown in this paper. The single ended 8T SRAM memory is designed to accomplish read stability. The total power consumption is also significantly lower as compared to the existing 8T SRAM memory system. So the single ended 8T SRAM memory can be used in internal CPU. The low power operation is achieved without sacrificing performance of memory. The introduction of transmission gate helps in enhancing the stability of the SRAM Cell.

ACKNOWLEDGEMENTS

I whould like to sincerely thank Prof. B. P. Singh, Head of Department of Electronics & Communication, Mody Institute of Technology and Science, Lakshmangarh who inspired me to do this work. In addition I would like to thank Prof. J. V. Desai, Dean, Faculty of Engineering, Mody Institute of Technology and Science for providing resources to carry out the work.

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