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Low Power 4-2 Compressor for Arithmetic Circuits

Riya Garg, Suman Nehra, B. P. Singh

***Abstract*: Most of the VLSI circuits used adders as a crucial portion, since they form the base element of all arithmetic functions. Increasing demand for portable equipments requires area and power efficient VLSI circuits. This paper presents 4-2 compressor using two different 8T full adder designs. The aim of this paper is to reduce the power consumption of 4-2 compressor without compromising the speed and performance. All pre-layout and post-layout simulations have been performed at 45nm technology on Tanner EDA tool version 12.6 and compared in terms of power consumption, power-delay product (PDP) over various input voltages, temperatures and frequencies.**

***Index Terms*: 2T (2 transistors), 3T, 8T and PDP.**

I. INTRODUCTION

Addition is a fundamental operation in many VLSI systems such as application specific DSP architectures and microprocessors. Full adder is fundamental unit in various circuits, especially, in performing arithmetic operations such as compressors, comparators, parity checkers, multipliers etc. It is the nucleus of many other useful operations such as subtraction, multiplication, division, exponentiation, address calculation and can significantly influence the overall achievable performances of the system [1]. At the same time, the sustained massive growth of the mobile appliances market is pushing the demand for power-efficient VLSI circuits. For this reason, low power high speed adders are highly desirable.

The role of full adders in arithmetic circuits can be classified into two categories [2]:

- The chain structured such as ripple carry adders (RCA) and array multipliers. In these applications, the critical path often traverses from the carry input to the carry output of the full adders. It is demanded that the generation of the carry-out signal is fast. Otherwise, the slower carry-out generation will not only extend the worst case delay, but also create more glitches in the later stages, hence, consume more power.
- The tree structured, which is frequently used in multipliers.

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A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. The 4-2 compressor has been widely employed in the high speed multipliers for the construction of Wallace tree to lower the delay of the partial product accumulation stage [3], [4]. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing.

A. 1-bit full adder

A 1-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b and c_{in} and two outputs sum and carry [5]. Expressions for sum and carry are;

$$sum = a \oplus b \oplus c_{in} \quad (1)$$

$$carry = (a \oplus b)c_{in} + ab \quad (2)$$

Fig. 1 Block diagram of 1-bit full adder

The block diagram of 1-bit full adder, as shown in Fig. 1 is used as a basic building block in many VLSI circuits and systems such as comparators, parity checkers, ripple carry adder (RCA), carry skip adder, carry select adder, array multiplier, 4-2 compressor and microprocessors etc [6]. Thus, enhancing the performance of the 1-bit full adder block leads to the enhancement of the overall system performance.

B. 4-2 compressor

A 4-2 compressor consists of five inputs and three outputs. It is called compressor, since it compress four partial products into two. This can be implemented with two stages of full adders (FA) connected in series as shown in Fig. 2.

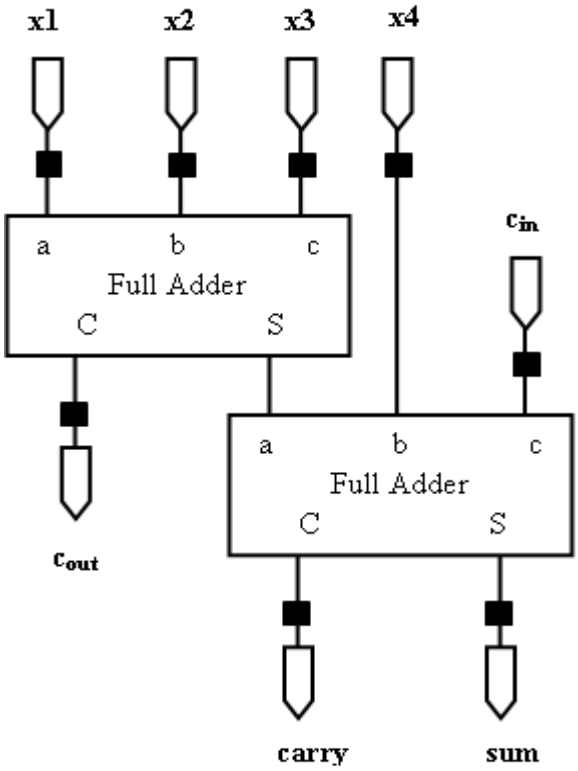

Fig. 2 Block diagram of 4-2 Compressor composed

Fig. 3 shows the logic decomposition of 4-2 compressor architecture. It is mainly consisted of six modules, four of which are XOR circuits and the other two are 2:1 MUX.

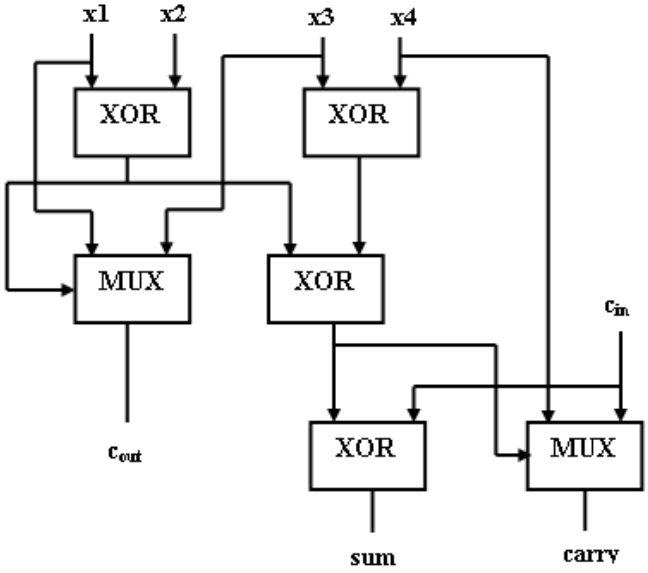

Fig. 3 Logic diagram of 4-2 Compressor composed

The input variables in Fig. 3 are denoted by x1, x2, x3, x4, and c_{in}. The variables c_{in} is the c_{out} generated by the preceding stage [7], [8], [9]. The design of 4-2 compressor is based on modified set of equations for the c_{out}, sum and carry outputs as;

$$\text{sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus c_{in} \quad (3)$$

$$c_{out} = (x1 \oplus x2)\, x3 + x1x2 \quad (4)$$

$$\text{carry} = (x1 \oplus x2 \oplus x3 \oplus x4)\, c_{in} + (x1 \oplus x2 \oplus x3)\, x4 \quad (5)$$

The carry output (c_{out}) is connected to the carry input (c_{in}) of the next 4-2 compressor. Without propagating the carry to the higher bit, the 4-2 compressor can add four partial products because the carry output (c_{out}) does not depend on the carry input (c_{in}). This makes it a carry-free adder stage.

II. Proposed Work

The existing 8T and proposed 8T full adder have been used to implement 4-2 compressor. These full adders have been implemented using two number of 3T XNOR gate in cascade and the carry output has been implemented using 3T XNOR gate and 2T multiplexer. The performance of 4-2 compressor has been analyzed to verify the performance of 1-bit full adder in complex VLSI circuitry [9], [10]. The schematic and layout design of 4-2 compressor using existing 8T full adder are shown in Fig. 4 and Fig. 5.

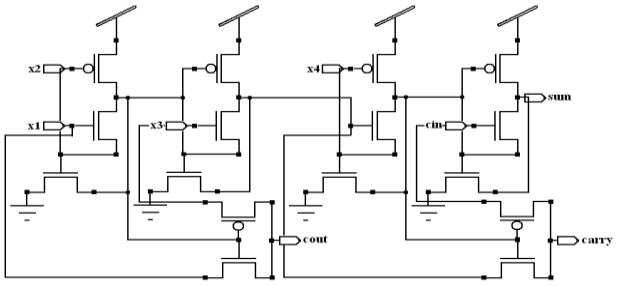

Fig. 4 Schematic of 4-2 compressor using existing 8T full adder

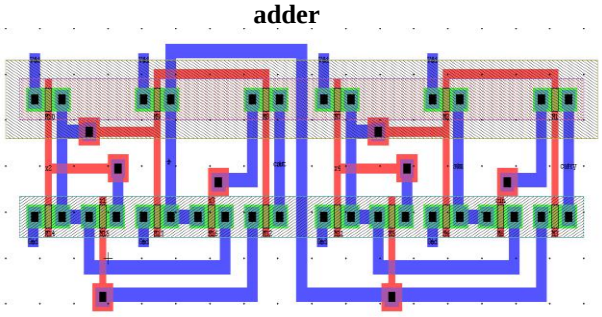

Fig. 5 Layout of 4-2 compressor using existing 8T full adder

Fig. 6 shows the schematic of 4-2 compressor using proposed 8T full adder. Layout design of 4-2 compressor using proposed 8T full adder is shown in Fig. 7 [11-13].

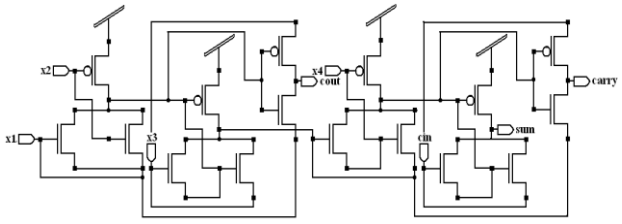

Fig. 6 Schematic of 4-2 compressor using proposed 8T full adder

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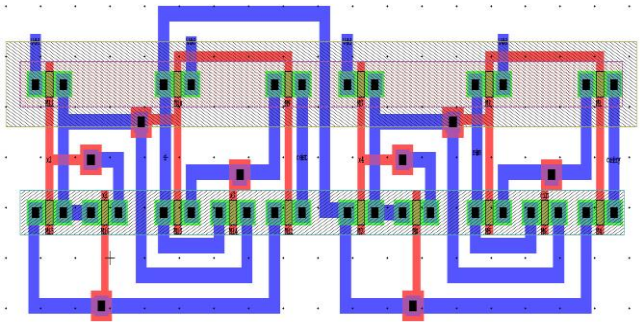

Fig. 7 Layout of 4-2 compressor using proposed 8T full adder

III. SIMULATION RESULTS

The 4-2 compressor using proposed 8T full adder and existing 8T full adder both the designs are analyzed in terms of power consumption and power-delay product at varying input voltages, frequencies and temperatures. To establish an impartial testing environment both circuits were simulated on same input patterns which covers each and every combination of the input stream. All schematic simulations are performed on Tanner EDA tool version 12.6 at 45nm technology with input voltage ranging from 0.4 V to 1.0 V in steps of 0.1 V.

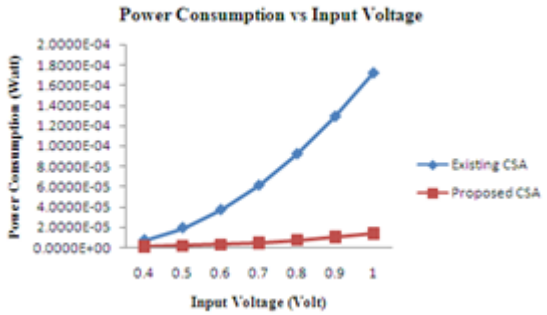

Fig. 8 Power consumption over varying input voltage

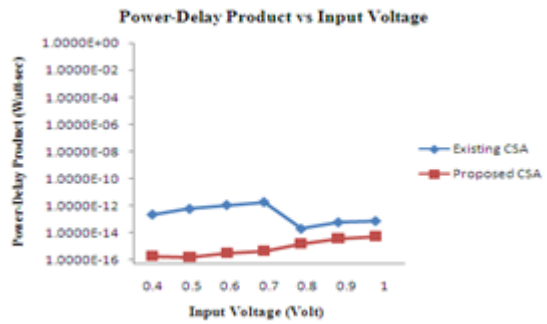

Fig. 9 PDP over varying input voltage

Fig. 8 and Fig. 9 depicts that the 4-2 compressor using proposed 8T full adder has less power consumption and PDP with varying input voltage as compared to the 4-2 compressor using existing 8T full adder circuit.

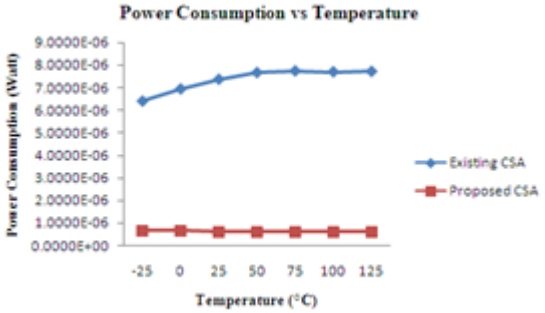

Fig. 10 Power consumption over varying temperature

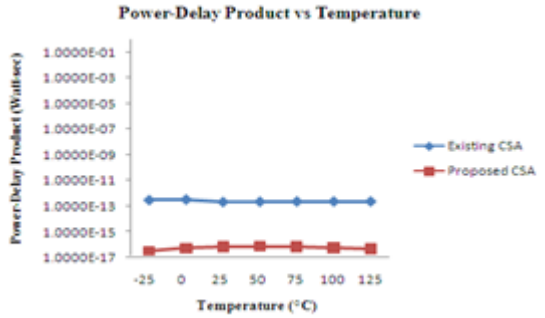

Fig. 11 PDP over varying temperature

The 4-2 compressor using existing 8T full adder and proposed 8T full adder are compared in terms of power consumption and PDP with varying temperature is shown in Fig. 10 and Fig. 11 respectively. The results shows that the 4-2 compressor using proposed 8T full adder has better temperature sustainability which remains constant over large range of temperature than 4-2 compressor using existing 8T full adder.

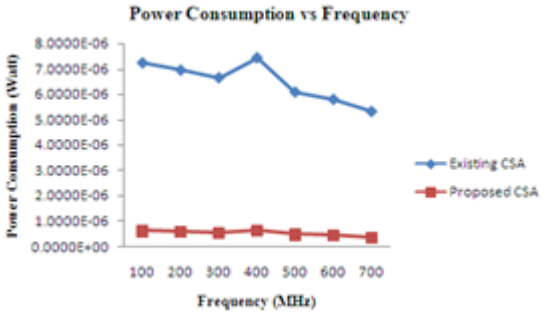

Fig. 12 Power consumption over varying frequency

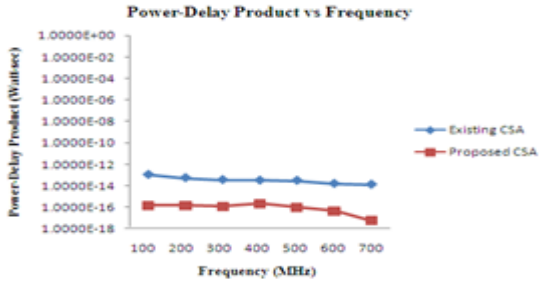

Fig. 13 PDP over varying frequency

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Similarly Fig. 12 and Fig. 13 show the comparison of power consumption and PDP with varying operating frequency. This shows that the 4-2 compressor using proposed 8T adder has better results than the existing one.

IV. CONCLUSION

The 4-2 compressor has been designed using a proposed 8T full adder and existing 8T full adder. The proposed design shows 92% and 99% improvement in terms of power consumption and PDP in comparison to existing design. Thus, the power consumption and PDP of proposed design is remarkably improved with respect to varying input voltage, temperature as well as frequency as compared to the 4-2 compressor using existing design. Hence, it proves itself to be a better option for low power devices and complex systems. All simulations are performed on 45nm standard model on Tanner EDA tool version 12.6.

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Ms. Riya Garg was born in Aklera, Rajasthan, INDIA on 13/01/1991. She has done B.Tech in Electronics and Communication Engineering from the Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan, INDIA in 2011. Presently, she is pursuing M.Tech. in VLSI Design from same university.

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He has authored four books, namely; Microprocessors, Interfacings and Applications, Advance Microprocessors & Microcontrollers, New Age International, New Delhi. Microelectronic Devices & Circuits: Indefinite Admittance Matrix Approach, New Age International, New Delhi. Electronic Devices and Integrated Circuits; Pearson, Education, New Delhi.

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