Unified Power Quality Conditioner for two feeders in a Distribution System

Aparna.Ch, Vijay Kumar.K, Prathap.T

Abstract— A UPQC consists of a series voltage-source converter (VSC) and a shunt VSC both joined together by a common dc bus. This paper proposes a new connection for a unified power quality conditioner (UPQC) to improve the power quality of two feeders in a distribution system. It is demonstrated how this device is connected between two independent feeders to regulate the bus voltage of one of the feeders while regulating the voltage across a sensitive load in the other feeder. Since the UPQC is connected between two different feeders (lines), this connection of the UPQC will be called an interline UPQC (IUPQC). This paper gives the structure; control and capability of the IUPQC under some special conditions like sag has been created in feeder 1 and 2 are discussed. The efficiency of the proposed configuration has been verified through simulation studies using MATLAB.

Keywords: Interline Unified power quality conditioner (IUPQC), power quality, sensitive load, voltage sag, voltage-source converter (VSC).

I. INTRODUCTION

Voltage source converter (VSC) based custom power devices are increasingly being used in custom power applications for improving the power quality (PQ) of power distribution systems. Devices such as distribution static compensator (DSTATCOM) and dynamic voltage restorer (DVR) have already been discussed extensively in [1]. A DSTATCOM can compensate for distortion and unbalance in a load such that a balanced sinusoidal current flows through the feeder [2]. It can also regulate the voltage of a distribution bus [3], [4]. A DVR can compensate for voltage sag/swell and distortion in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated [5], [6]. A unified power-quality conditioner (UPQC) can perform the functions of both DSTATCOM and DVR [7], [8]. The UPQC consists of two voltage-source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor.

It is also possible to connect two VSCs to two different feeders in a distribution system. In [9], a configuration called IDVR has been discussed in which two DVRs are connected in series with two separate adjacent feeders. The dc buses of the DVRs are connected together. The IDVR absorbs real power from one feeder and maintains the dc link voltage to mitigate 40% (about 0.6 p.u.) voltage sag in the other feeder with balanced loads connected in the distribution system. It is also possible to connect two shunt VSCs to different feeders through a common dc link. This can also perform the functions of the two DVRs mentioned above, albeit with higher device rating.

This paper presents a new connection for a UPQC called interline UPQC (IUPQC). The single-line diagram of an IUPQC connected distribution system is shown in Fig. 1. Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations, supply the system loads L-1 and L-2. The supply voltages are denoted by v_s1 and v_s2. It is assumed that the IUPQC is connected to two buses B-1 and B-2, the voltages of which are denoted by v_t1 and v_t2, respectively. Further two feeder currents are denoted by i_f1 and i_f2, while the load currents are denoted by i_L1 and i_L2. The load L-2 voltage is denoted by v_L2.

Fig1. Single-line diagram of an IUPQC-connected distribution system

The purpose of the IUPQC is to hold the voltages v_t1 and v_t2 constant against voltage sag/swell, temporary interruption in either of the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say Feeder-1) to holdVt2constant in case of a sag in the voltage. This can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed. The performance of the IUPQC has been evaluated through simulation studies using MATLAB.

II. STRUCTURE AND CONTROL

The IUPQC shown in Fig. 1 consists of two VSCs (VSC-1 and VSC-2) that are connected back to back through a common energy storage dc capacitor C_{dc}. Let us assume that the VSC-1 is connected in shunt to Feeder-1 while the VSC-2 is connected in series with Feeder-2. Each of the two VSCs is realized by three H-bridge inverters [10], [11]. The schematic structure of a VSC is shown in Fig. 2. In this structure, each switch represents a power semiconductor device (e.g., IGBT) and an anti-parallel diode as shown in Fig. 2.
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All the inverters are supplied from a common single dc capacitor and each inverter has a transformer connected at its output.

III. SYSTEM DESCRIPTION

An IUPQC connected to a distribution system is shown in Fig. 4. In this figure, the feeder impedances are denoted by the pairs \((R_{11}, L_{11})\) and \((R_{12}, L_{12})\). It can be seen that the two feeders supply the loads L-1 and L-2. The load L-1 is assumed to have two separate components—an unbalanced part (L-11) and a non-linear part (L-12). The currents drawn by these two loads are denoted by \(I_{1,1}\) and \(I_{1,2}\), respectively. We further assume that the load L-2 is a sensitive load that requires uninterrupted and regulated voltage. The shunt VSC (VSC-1) is connected to bus B-1 at the end of Feeder-1, while the series VSC (VSC-2) is connected at bus B-2 at the end of Feeder-2. The voltages of buses B-1 and B-2 and across the sensitive load terminal are denoted by \(V_{t1}\), \(V_{t2}\) and \(V_{l2}\) respectively. The aim of the IUPQC is two-fold:

- To protect the sensitive load L-2 from the disturbances occurring in the system by regulating the voltage \(V_{l2}\)
- To regulate the bus B-1 voltage \(V_{t1}\) against sag/swell and/or disturbances in the system.

In order to attain these aims, the shunt VSC-1 is operated as a voltage controller while the series VSC-2 regulates the voltage across the sensitive load.

The system parameters used in the study are given in Table I. The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2. The voltage of bus B-1 and load L-1 currents, when no IUPQC is connected to the distribution system, are shown in Fig. 5. It can be seen from Fig. 8.2 that due to the presence of unbalanced and non-linear load L-1, the voltage \(V_{t1}\) is both unbalanced and distorted. Also, the load L-11 causes an unbalance in the current \(i_{12}\) while load L-12 causes distortion in the current \(i_{11}\). We shall now demonstrate how these waveforms can be improved using the IUPQC.

### Table 1 System Parameters

<table>
<thead>
<tr>
<th>System quantities</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>System fundamental frequency (f)</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Voltage source (v_{l1})</td>
<td>11 kV (L-L, rms), phase angle 0°</td>
</tr>
<tr>
<td>Voltage source (v_{l2})</td>
<td>11 kV (L-L, rms), phase angle 0°</td>
</tr>
<tr>
<td>Feeder-1 ((R_{11}+j2\pi f L_{11}))</td>
<td>Impedance: 6.05 + j36.28 Ω</td>
</tr>
<tr>
<td>Feeder-2 ((R_{12}+j2\pi f L_{12}))</td>
<td>Impedance: 3.05 + j18.14 Ω</td>
</tr>
<tr>
<td>Load L-11 Unbalanced RL component</td>
<td>Phase-a 24.2 + j60.50 Ω</td>
</tr>
<tr>
<td></td>
<td>Phase-b 36.2 + j85.54 Ω</td>
</tr>
<tr>
<td></td>
<td>Phase-c 48.2 + j94.25 Ω</td>
</tr>
<tr>
<td>Load L-12 Non-linear component</td>
<td>A three-phase diode rectifier that supplies a load of 250 + j31.42 Ω</td>
</tr>
<tr>
<td>Balanced Load L-2 impedance</td>
<td>72.6 + j54.44 Ω</td>
</tr>
</tbody>
</table>
IV. IUPQC OPERATION

As mentioned before, the shunt VSC (VSC-1) holds the voltage of bus B-1 constant. This is accomplished by making the VSC-1 to track a reference voltage across the filter capacitor C_f. The equivalent circuit of the VSC-1 is shown in Fig. 10(a) in which U1. Vdc denote the inverter output voltage where V_d is the dc capacitor voltage and U1 is the switching action equal to ±n1 where n1 is the turns ratio of the transformers of VSC-1. In Fig. 10(a), the inverter losses and leakage inductance of the transformers are denoted by R_f1 and L_f1, respectively. All system parameters are referred to the line side of the transformers.

It is assumed that the dc capacitor is initially uncharged and both the feeders along with the IUPQC are connected at time zero. It can be seen from Fig. 11, that the three-phase B-1 voltages, are perfectly balanced with a peak of 11 kV. Once these voltages become balanced, the currents drawn by Feeder-1I1 become balanced. The load L-2 bus voltages, are shown in Fig.15 are also perfectly sinusoidal with the desired peak of (11 kV) as the converter VSC-2 injects the required voltages in the system. The bus B-2, voltage v(t), can be seen to have a much smaller magnitude (about 10.75 kV peak).

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V. TRANSIENT PERFORMANCE OF IUPQC

Now, the performance of IUPQC has been evaluated considering various disturbance conditions. We shall also discuss and evaluate the limits of performance.

A. Voltage Sag in Feeder-1

With the system operating in the steady state, a 6 cycle (100 ms) voltage sag occurs at 0.15 s in which peak of the supply voltage reduces to 6 kV from their nominal value of 9 kV. The various waveforms of only one phase (phase-a) are shown in Fig.17. The trends in the other two phases are similar. It can be seen that the dc capacitor voltage, \( V_{dc} \), drops as soon as the sag occurs. If the bus voltage remains constant, the load power also remains constant. However, since the source voltage has dropped, the power coming out of the source has reduced. In order to supply the balance power requirement of the load, the \( V_{dc} \) drops. The current through Feeder-1 is also shown in Fig. 19. It can be seen that in order to supply the same load power at a reduced source voltage, the feeder current increases. Also, the transients in this current occur at the inception and the removal of the sag due to the change in the source voltage.

It has been observed that bus B-1 voltage \( Vt1 \) starts getting distorted when the voltage sag causes the peak of the source voltage to drop below 6.0 kV. Also, for deeper voltage sags, the peak of reduces and the VSC-1 is not able to hold the bus voltage.

B. Voltage Sag in Feeder-2

With the system operating in the steady state, Feeder-2 is subjected to a voltage sag at 0.15 s in which the peak of all three phases of the supply voltage \( Vs2 \) reduces to 6.0 kV from their nominal value of 9.0 kV. The sag lasts for 3 cycles (50 ms). The system response is shown in Fig.22. The bus B-2 voltage, the dc link voltage \( V_{dc} \), It can be seen that \( V_{dc} \) drops to around 2.3 kV during the sag. The bus B-1 voltage and load L-2 voltage are shown in Fig.17,18. The load L-2 voltage remains balanced and sinusoidal barring some glitches at the inception and removal of the sag. However, the dc capacitor will collapse if the peak of the voltage falls below 3.0 kV.
V. CONCLUSIONS

The paper illustrates the operation and control of an interline uniform power quality conditioner (IUPQC). The device is connected between two feeders coming from different substations. An unbalanced and non-linear load L-1 is supplied by Feeder-1 while a sensitive load L-2 is supplied through Feeder-2. The main aim of the IUPQC is to regulate the voltage at the terminals of Feeder-1 and to protect the sensitive load from disturbances occurring upstream. The performance of the IUPQC has been evaluated under various disturbance conditions such as voltage sag in either feeder, fault in one of the feeders and load change. It has been shown that in case of a voltage sag, the phase angle of the bus voltage in which the shunt VSC is connected plays an important role as it gives the measure of the real power required by the load. The IUPQC can mitigate a voltage sag of about 0.65 p.u. (9 kV to 6 kV) in Feeder-1 and 0.65 p.u. (i.e.9 kV to 6 kV) in Feeder-2 for long duration. The IUPQC discussed in the paper is capable of handling system in which the loads are unbalanced and distorted. Extensive case studies have been included to show that an IUPQC might be used as a versa- tile device for improving the power quality in an interconnected distribution system.

From above discussion, it has been observed that an IUPQC is able to protect the distribution system from various disturbances occurring either in Feeder-1 or in Feeder-2. As far as the common dc link voltage $V_{dc}$ is at the reasonable level, the device works satisfactorily. The angle controller ensures that the real power is drawn from Feeder-1 to hold the dc link voltage constant. Therefore, even for a voltage sag or a fault in Feeder-2, VSC-1 passes real power through the dc capacitor onto VSC-2 to regulate the voltage.

In conclusion, the performance under some of the major concerns of both customer and utility e.g., harmonic contents in loads, unbalanced loads, supply voltage distortion, system disturbances such as voltage sag has been studied. The IUPQC has been shown to compensate for several of these events successfully.

REFERENCES


