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Design and Implementation of Intelligent Control of a Fly back Quasi Resonant Converter

T.Anitha, S.Arulselvi

Abstract: ***Power supply voltages in digital systems have been reduced considerably in recent years and often digital components requiring different voltages are present in the same board. This has increased the demand for multiple output power distribution systems with tight load regulation. In this paper, a detailed analysis and design of a multi-output flyback zero voltage switching (ZVS) quasi resonant converter(QRC) has been carried out. The effect of cross regulation due to load resistances and leakage inductances are studied and obtained. To reduce the effect of cross-regulation, conventional PI controllers are designed and simulated. In order to improve the performances of the converter due to nonlinearity, intelligent controller like fuzzy logic controller is proposed and simulated. The output results for load regulations are presented and the performances of both the controllers are compared. The result reveals that fuzzy logic controller gives satisfactory performances.***

Index Terms*— dc-dc converters, flyback converter, fuzzy logic control , cross regulation.*

I. INTRODUCTION

Multi-output PWM dc-dc converters are widely used in communications, aerospace and computer systems, as they are usually more compact and less expensive than a collection of single-output converters. Fig. 1 shows the schematic of single power converter with multiple outputs, e.g. flyback converter with multiple secondary windings, and regulates one output. This leads to poor load regulation in the others outputs. In some cases each output is regulated by feedback control and others tracks as best they can. This scheme is known as cross regulation [1].

In aerospace applications the allowable size and weight are highly restricted to accommodate greater payload. In the effort to increase the power density of power supplies, the switching frequency is pushed to high values which, in PWM converter realizations, normally lead to considerable power loss. Another significant drawback of the switch-mode operation is the EMI produced due to large di/dt and dv/dt. To overcome these short comings, new families of QRCs are introduced [1]-[3]. The design and control of multi-output forward FM-ZCS-QRC is presented [1].

The detailed analysis and technique of determining the cross regulation characteristics of a two-output half-bridge clamped series resonant converter (SRC) operating in the discontinuous conduction mode below resonance is reported[4]. This topology requires a wide range of frequency band in order to regulate disturbances the output voltage against load variations and supply disturbances. To eliminate this frequency (CF)-ZVS-QRC is proposed[5]. It has two switches, the presence of the auxiliary switch provide inductor freewheeling thereby reducing the control range of frequencies when compared with the conventional FM-QRCs. The converter may thus be called a CF-ZVS-QRC. The elaborate study of cross regulation due to leakage inductances and variation in load resistances is not reported in the above said paper. Hence, an attempt is made in this paper, to study the effect of cross regulation due to leakage inductances and variation in load resistances.

Also this paper presents, the design and implementation of a closed loop control to reduce the effect of cross regulation using conventional PI and fuzzy logic controllers for the multi-output flyback ZVS-QRC. All simulation works are carried out using MATLAB/SIMULINK software. The performances of two control techniques are compared.

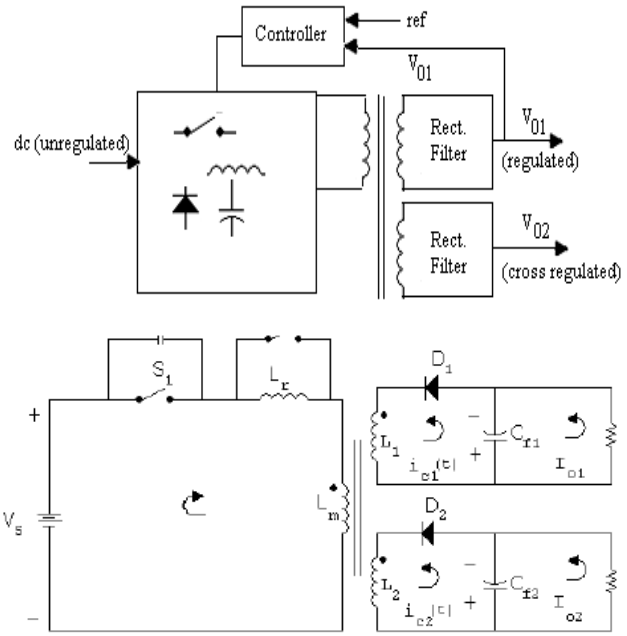

Fig. 1. Multiple outputs using single power converter.

II. ANALYSIS OF MULT-OUTPUT FLYBACK ZVS-QRC

The circuit diagram of multi-output fly back ZVS-QRC is shown in the Fig. 2. The switch S_1 is the main switch. The elements L_r and C_r form the resonant tank circuit.

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By adding an auxiliary switch S_2 in parallel with the resonant inductor L_r, the switching frequency band required to regulate the output voltage for a given load change is reduced. The auxiliary switch S_2 is used to control the off time of the switching period. Here, the converter is operated in half-wave mode. The elements L_m, L_1 and L_2 represent the primary, secondary1 and secondary2 inductances, respectively. The current through the primary of the transformer is assumed as magnetizing current I_m, which is equal to i_{Lr}. The following parameters are defined [2][5] for the analysis: Characteristics impedance=Z_0, resonant angular frequency =ω_0, resonant frequency = f_0 , resonant capacitor voltage = v_{cr} . Normalized Load Resistance $R=\frac{R_o^{'}}{Z_o}$

Voltage conversion ratio M_1 = V_{o1} / V_s
Voltage conversion ratio M_2 = V_{o2} / V_s

To simplify the analysis, the equivalent circuit diagram for the converter by transferring the elements from secondary to primary is shown in Fig. 3.Further modifications of Fig. 3 is shown in Fig. 4. Referring to Fig. 2 and Fig. 4, $V_0^{'}=V_{oi}^{'}$ and $V_{0i}=V_{oi}^{'}$, where i =1, 2.Whenever a switching device changes from one state to another, the circuit configuration changes. Each configuration is referred to as a stage. In this QRC, six different stages are identified for each switching cycle and they are discussed as follows:

A. *Linear capacitor charging stage (t_o, t_1)*

The switch S_1 is opened to begin a new cycle at t = t_o. During this stage, the primary current I_m flows through the resonant capacitor C_r and its voltage increases linearly from zero to $(V_s+V_o^{'})$. The capacitor voltage v_{cr} is governed by the equation

$$V_{cr}(t)=\frac{I_m t}{C_r} \qquad (1)$$

When capacitor voltage $v_{cr(t)}$ reaches $(V_s+V_o^{'})$ at t = t_1, the diode D_m gets forward biased. The duration of this stage is given by

$$T_{d1}=t_1-t_2=\frac{C_r(V_s+V_o^{'})}{I_m} \qquad (2)$$

B. *Resonant inductor discharging stage (t_1, t_2)*

Stage 2 begins when the diode D_m conducts. The elements L_r and C_r form a series resonant circuit. The state equations are

$$\frac{dV_{cr}}{dt}=\frac{i_{Lr}(t)}{C_r}$$

$$\frac{di_{Lr}}{dt}=\frac{(V_s+V_o^{'})-V_{cr}(t)}{L_r} \qquad (3)$$

With initial conditions $V_{cr}(0)=(V_s+V_o^{'})$ and $i_{Lr}(0)=I_m$. The solutions for the above equations are

$$V_{cr}(t)=(V_s+V_o^{'})+I_m Z_o \sin(\omega_o t)$$
$$i_{Lr}(t)=I_m \cos(\omega_o t)$$
$$V_{Lr}(t)=-I_m Z_o \sin(\omega_o t) \qquad (4)$$

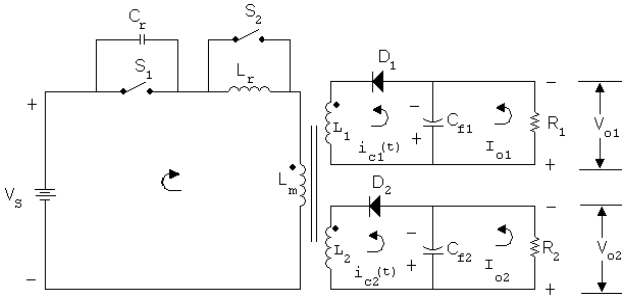

Fig. 2 circuit diagram of multi-output fly back ZVS-QRC

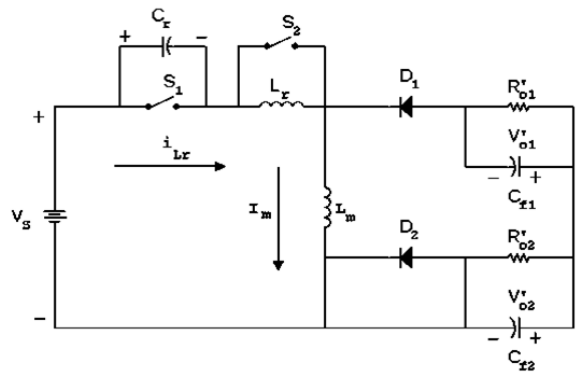

Fig. 3 Equivalent circuit diagram for the converter after transferring the elements from secondary to primary.

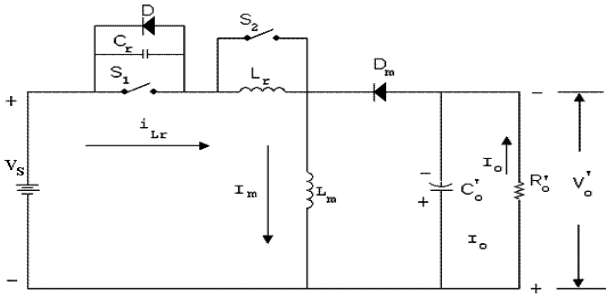

Fig. 4 Final equivalent circuit of the multi-output flyback ZVS-QRC.

At t_1, $i_{Lr}(t)$ reaches zero and $V_{cr}(t)$ reaches its peak value (refer Fig. 5) as

$$V_{cr}(t)=V_{cpeak}=(V_s+V_o^{'})+I_m Z_o \qquad (5)$$

When $V_{Lr}(t)$ reaches zero at t = t_2, the switch S_2 is turned ON to reduce losses as shown in Fig. 5. The duration of this stage is T_{d2} which is equal to $t_2 - t_1$.

$$T_{d2}=t_2-t_1=\frac{\pi}{\omega_o} \qquad (6)$$

At t = t_2, the voltage across C_r then becomes $(V_s+V_o^{'})$

C. *Holding stage (t_2, t_3)*

This is the new stage, which characterizes the multi-output flyback ZVS-QRC. The constant switching frequency operation is achieved by introducing the holding stage, during which i_{Lr} and V_{cr} are held constant. The voltage V_{Lr} is clamped at zero value by keeping the switch S_2 closed. Then for this stage, voltage and current equations are given by

$$V_{cr}(t)=(V_s+V_o^{'})$$
$$i_{Lr}(t)=I_m \qquad (7)$$

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This stage continues until S_2 is turned OFF at t = t_3. The duration of this stage is T_{d3} which is equal to $t_3 - t_2$. The conversion ratio M_1 and M_2 can also be varied by varying T_{d3}.

D. *Resonant inductor charging stage (t_3, t_4)*

Resonance of L_r and C_r resumes when S_2 is turned OFF at t = t_3 and the corresponding equations are

$$\frac{di_{Lr}}{dt} = \frac{(V_S + V_o') - V_{cr}(t)}{L_r}$$

$$\frac{dV_{cr}}{dt} = \frac{i_{Lr}(t)}{C_r} \qquad (8)$$

With initial conditions $V_{cr}(0) = (V_S + V_o')$ and $i_{Lr}(0) = -I_m$. The solutions for the above equations are

$$i_{Lr}(t) = I_m \cos(\omega_o t)$$

$$V_{cr}(t) = (V_S + V_O') - I_m Z_O \sin(\omega_o t) \qquad (9)$$

This stage terminates when $V_{cr}(t)$ becomes zero. The duration of this stage is Td_4 which is equal to $t_4 - t_3$.

$$T_{d4} = \frac{1}{\omega_o}\arcsin\left(\frac{V_S + V_o'}{I_m Z_o}\right)$$

$$T_{d4} = \frac{(\alpha - \pi)}{\omega_o}$$

$$\alpha = \pi + \arcsin\left(\frac{V_S + V_o'}{I_m Z_o}\right) \qquad (10)$$

where α lies in the range $\pi < \alpha < 3\pi/2$. Then the inductor current i_{Lr} is given by the equation $i_{Lr}(t_4) = I_m \cos(\alpha)$.

E. *Linear inductor charging stage (t_4, t_5)*

The switch S_1 is turned ON at t=t_4 as shown in Fig. 5, when V_{cr} becomes zero to reduce turn-on loss. The current i_{Lr} increases linearly and reaches I_m at t = t_5. Beyond t_4, the capacitor voltage is clamped to zero by the diode D as shown in Fig. 4. The corresponding state equation is

$$\frac{di_{Lr}}{dt} = \frac{V_S + V_o'}{L_r} \qquad (11)$$

With initial condition, $i_{Lr}(t)$ is given by

$$i_{Lr} = \left(\frac{V_S + V_o'}{I_m Z_o}\right) + I_m \cos(\alpha) \qquad (12)$$

This stage terminates when inductor current becomes I_m. The duration of this stage is given by

$$T_{d5} = \left(\frac{I_m Z_o (1 - \cos(\alpha))}{(V_S + V_o')\omega_o}\right) \qquad (13)$$

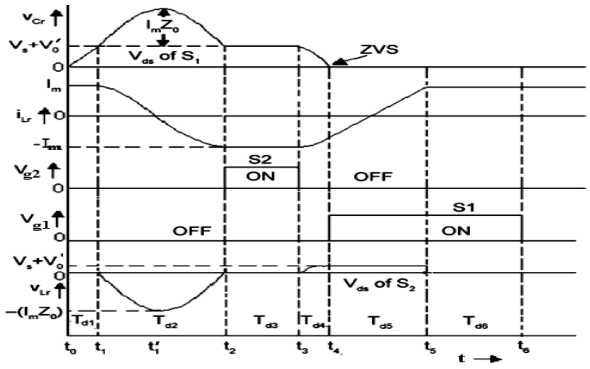

Fig. 5 Theoritical waveforms of multi-output flyback ZVS-QRC.

F. *Constant current stage (t_5, t_6)*

Once the inductor current $i_{Lr}(t)$ reaches I_m at t_5, the diode D_m turns OFF. The switch S_1 conducts as long as it is kept ON. At t_6, the switch S_1 is turned OFF which starts the new cycle. The duration of this stage is T_{d6} which is equal to $t_6 - t_5$. The theoretical waveforms of the multi-output flyback ZVS-QRC are shown in Fig. 5.

III. OPEN LOOP SIMULATION

A. *Design Procedure*

The design parameter of a multi-output fly back ZVS-QRC[5-6], tabulated in Table 1 are used for analysis and simulation studies.

Table 1 : Design parameters

V_s (V)	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	L_r µH	C_r µF	f_s kHz	f_o kHz
12	5	12	1	0.5	28.2	0.033	25	165

Selecting normalized frequency, f_{ns} as 0.15 and the switching frequency f_s as 25 kHz, the resonant frequency is calculated as $f_o = f_s/0.15$ = 165 kHz. The condition for zero voltage switching is

$$I_m Z_o > (V_S + V_o') \qquad (14)$$

Maximum magnetizing current I_m at nominal load

$I_m = (M+1)I_o = 2.1A$

Where, $I_o = I_{o1}n_1 + I_{o2}n_2$ and $M = V_S / V_o'$.

Therefore to satisfy (14), Z_o>12Ω, using Z_o and f_o values, the resonant components L_r and C_r are calculated as 28.2µH and 0.0333µF, respectively.

B. *Open loop simulation results*

The open loop simulation of multi-output fly back ZVS-QRC is carried out using MATLAB/SIMULINK software. The simulated resonant capacitor voltage (V_{cr}), resonant inductor current(I_{Lr}) and gate pulses applied to S_1(V_{g1}) and S_2 (V_{g2}) for the nominal load conditions of secondary are shown in Fig. 6. It is seen that these waveforms agree closely with the theoretical waveforms as shown in Fig. 5. It is observed from Fig. 7and 8 that in open loop operation, the converter output deviates from the required output voltage 5V and 12V and settles at a new value after a sudden load current changes at time t = 9 msec from 1A to 1.42A. Hence a closed loop control is needed to regulate the output voltages against load variation.

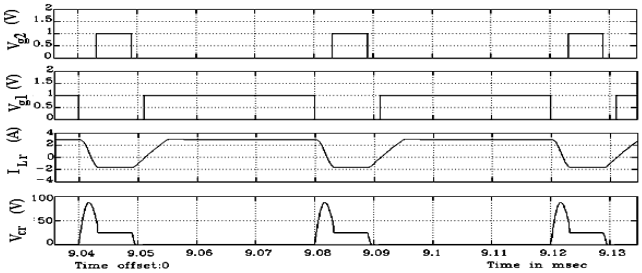

Fig. 6 Simulated waveforms showing the gate pulse of switches, resonant inductor current, and resonant capacitor voltage.

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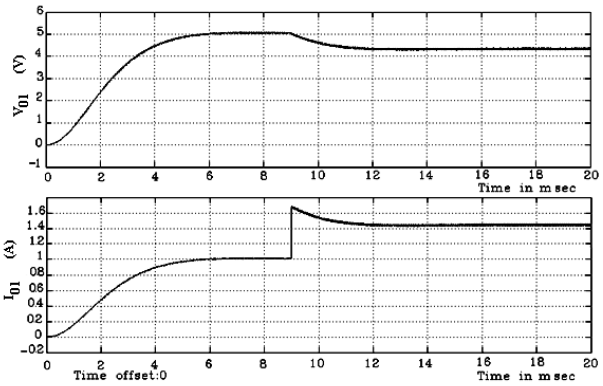

Figure 7 Output voltage (V_{01}) and current (I_{01}) of secondary 1 for sudden load current (I_{01}) variation of 1A to 1.42A.

IV. CLOSED LOOP SIMULATION

The block diagram of closed - loop control is shown in Fig. 9. To regulate the output voltage V_{o1}, the switching frequency of the PWM pulses are varied depends on error. Since output V_{01} is very sensitive to load variation by producing large deviations from nominal value for small variations in load. Hence a closed-loop control is designed to maintain tight regulation of V_{01} against load variation and V_{02} is cross-regulated.

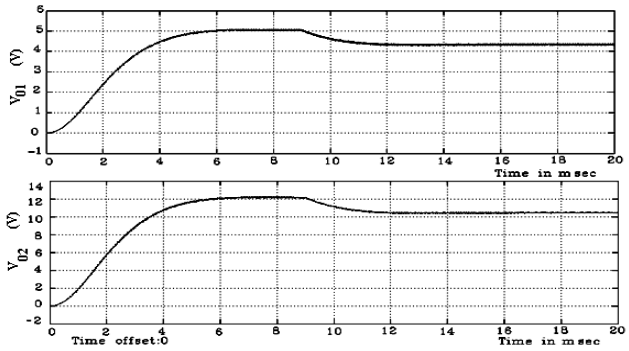

Fig. 8. Output voltages V_{01} and V_{02} of secondary1 and 2 for sudden load current (I_{01}) variation of 1A to 1.42A.

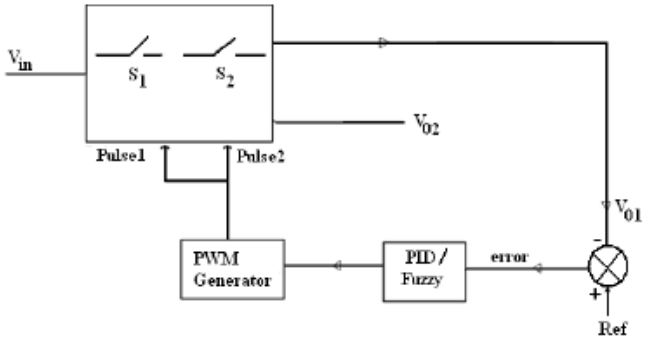

Fig. 9 Block diagram of closed loop control of multi-output ZVS flyback QRC.

A. *Cross Regulation Characteristics*

In practical transformer, there is some flux links one winding but not the other, by "leaking" into the air or by other mechanism. This flux leads to leakage inductances that are in series with the windings. The winding order in a transformer has a large effect on the leakage inductance. Transformer windings should be arranged in concentric fashion for minimum leakage inductance. In multiple output transformer, the secondary with the highest output power should be placed closest to the primary for the best coupling and hence lowest leakage. If a secondary winding has relatively few turns, the turns should be spaced so that they traverse the entire width of the winding area, for improved coupling [7].These points are considered to reduce the cross-regulation effect during real time experimentation in this work.

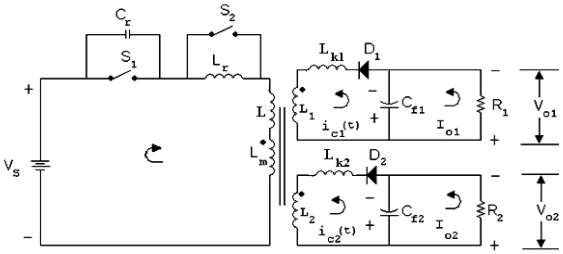

Fig. 10 Multi-output flyback with leakage inductances

Normalized load of Secondary1 is $Q_1 = R_{o1} / Z_o$

Normalized load of Secondary2 is $Q2 = R_{o2} / Z_o$

$$L_{ks} = L_{k1} L_{k2} / (L_{k1}+L_{k2})$$

$$a = L_{k1} / L_{k2}$$

$$k = L/L_{ks} \qquad (15)$$

1) Characteristics1 (M_2/M_1) vs (Q_1/Q_2) with varying 'M_1': Fig.11 shows the effect of converter gain M_1 on the cross regulation characteristics of the converter. Since the output voltage V_{o1} is regulated, the variation in M_1 provides the effect of change in the line voltage of the power supply. It is observed that the slopes of the curves are smaller at higher values of converter gain M_1. Hence, for a low percentage cross regulation error, the transformer should have higher turns ratio, which leads to low bandwidth. Therefore, the converter cannot operate effectively at high switching frequencies. This is in contrast to the condition that M_1 must be small for good self-regulation. Hence in this paper M_1=0.42 is considered.

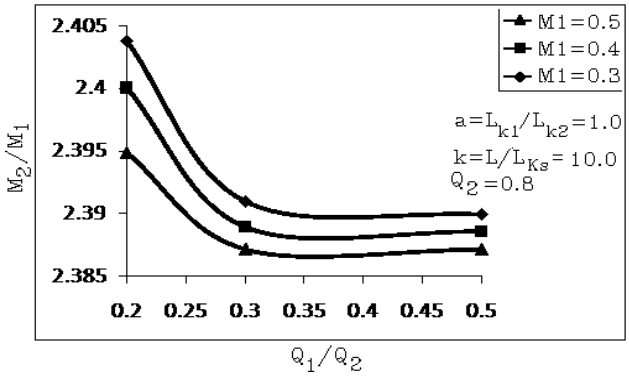

Fig.11. Cross regulation characteristics with M_1 as parameter.

2) Characteristics2 (M_2/M_1) vs (Q_1/Q_2) with varying 'a': Fig. 12 shows the cross regulation characteristics curves with the ratio of leakage inductances 'a' as a parameter (15). The leakage inductances depend on the techniques of winding the transformer. The slope of the characteristic curves is nearly independent of the ratio 'a' and gain M_2 is high at high 'a', which means that the converter design parameters are highly dependent on the ratio of leakage inductances. Hence, the transformer must be wound very carefully with close tolerances on the leakage inductances.

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The secondary winding of output 1 must be wound for low leakage flux for achieving low values of parameter 'a'. The secondary winding of output 2 may be wound closer to the core and beneath the secondary winding of the output 1 as considered in this paper. Another alternative may be to add an inductor in series with the secondary winding of output 2 to reduce the value of ratio 'a'.

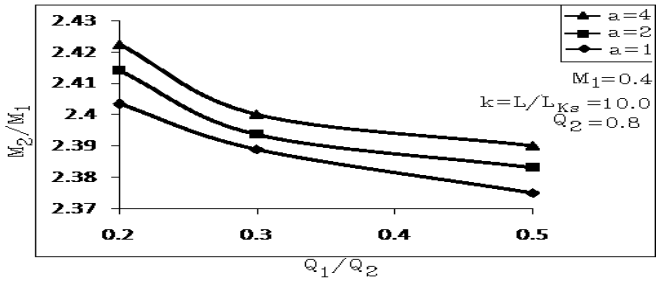

Fig. 12 Cross regulation characteristics with a = L_{k1} / L_{k2} as parameter.

2) *Characteristics3 (M_2/M_1) vs (Q_1/Q_2) with varying 'k':* Fig. 13 gives the cross regulation characteristics with the ratio k as a parameter. The slope of the characteristics curves is high for small ratio k. Hence, the parameter k must be designed to be high for low cross regulation error, which means that the resonant inductor must be higher than the leakage inductances. A large value of resonant inductor means a high value of characteristics impedance and consequently the converter current capability is not high. Furthermore, because of large resonant inductance, the converter cannot be operated at high switching frequencies.

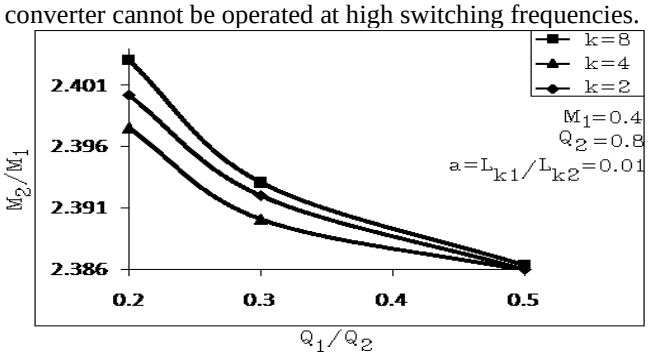

Fig. 13. Cross regulation characteristics with k = L / L_{ks} as parameter.

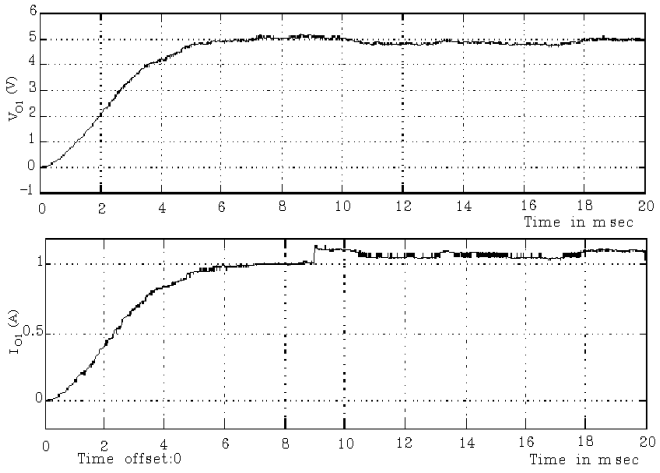

Fig. 14. Output voltage (V_{o1}) and current (I_{o1}) of secondary 1 for sudden load current (I_{o1}) variation of 1A to 1.42A with PI.

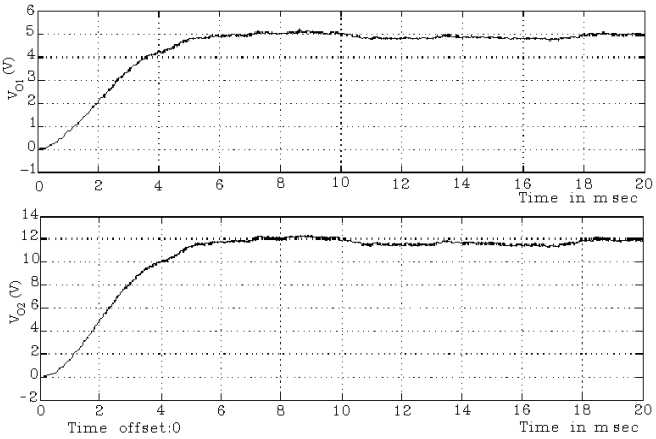

Fig. 15. Output voltage (V_{o1}) and (V_{o2}) of secondary 1 & 2 for sudden load current (I_{o1}) variation of 1A to 1.42A with PI.

B. Closed-loop control using PI controller

The conventional PI controller parameters are obtained by Z-N open loop method[8] as proportional gain K_c= 0.72 and integral gain K_i=1.347. Regulated output voltages V_{o1} and V_{o2} for sudden increase in load current (I_{o1}) at time t=9 msec from 1A to 1.42A are shown in Fig.14 and 15.

From the simulation results, it is observed that the output voltage V_{01} is well regulated and settles at its reference voltage 5V within 17msec with zero offset. The output voltage is also cross-regulated within 20 msec with zero offset.

However, PID controllers are more sensitive to operating point and parameter variations. It works satisfactorily only around small operating regions. The complex structure and non-linear characteristics of QRC necessitates the design of non-linear control. Hence in this paper, an attempt is made to design a fuzzy logic controller for the proposed converter to regulate the output voltage against load variations.

C. Closed-loop control using fuzzy logic control (FLC)

The inputs to the CFLC are the error voltage (e) and change in error (ce). The output is the change in switching frequency (Δu). Depending on the magnitude and sign of e and ce, the switching frequency of the main switch S_1 and auxiliary switch.

S_2 is varied to regulate the output voltage. For ease of computation, the variables e, ce and Δu are divided into five fuzzy subsets using triangular membership function as shown in Fig.16. Regulated output voltages V_{o1} and V_{o2} for sudden increase in load current (I_{o1}) at time t = 9msec from 1A to 1.42A are shown in Fig.17 and 18. The improved performances of FLC are given in Table III.

TABLE II FUZZY RULE BASE

e	NB	NS	Z	PS	PB
NB	NB	NB	NS	NS	Z
NS	NB	NS	NS	Z	PS
Z	NS	Z	Z	PS	PB
PS	NS	Z	PS	PB	PB
PB	Z	PS	PB	PB	PB

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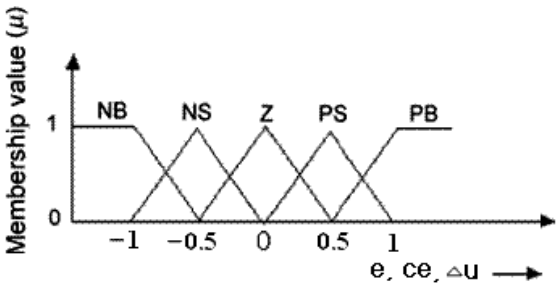

Fig. 16. Membership function diagram of c, ce, Δu.

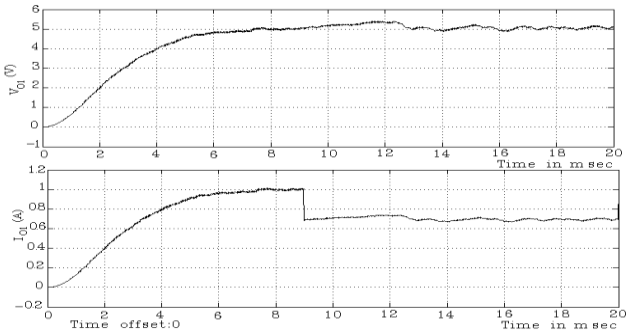

Fig. 17. Regulated output voltage (V_{o1}) and current (I_{o1}) of secondary1 for sudden load current (I_{o1}) variation of 1A to 1.42 A with FLC.

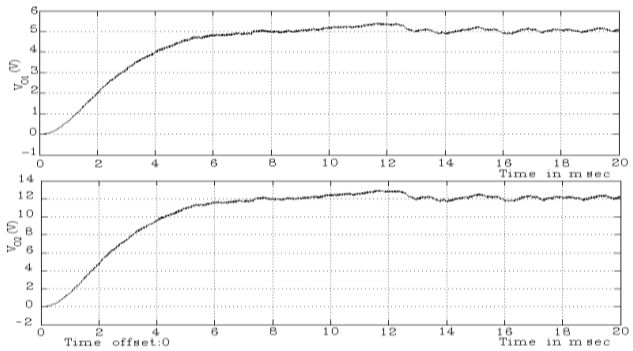

Fig. 18. Regulated output voltage (V_{o1}) and (V_{o2}) of Secondary1 & 2 for sudden load current (I_{o1}) variation of 1A to 1.42A with FLC.

TABLE III. PERFORMANCE MEASURES

	PI controller		Fuzzy logic controller	
	Up load	Down load	Up load	Down load
ISE	0.04546	0.04473	0.04429	0.04415
T_r(sec)	0.0063	0.0058	0.0072	0.006
Offset(V)	0.17	0.076	0.14	0.056
T_s(msec)	17	17.5	13.5	15

V. CONCLUSION

The performances of the multi output flyback converter with conventional PI controller and fuzzy logic controller are compared. The ISE value, rise time(T_r), settling time(T_s) and offset for sudden load current increase from 1A to 1.42A and sudden load current decrease from 1A to 0.7A are tabulated in Table III. It can be concluded that fuzzy logic controller is a better choice than conventional PI controller in terms of less ISE and offset.

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