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Design and FPGA Implementation of a Lifting Scheme 2D DWT Architecture

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Abstract*: This paper presents an area efficient, and simple design, of multilevel two dimensional discrete wavelet transform (2-D DWT) modules for image compression. The proposed architecture is based on lifting scheme approach, using the (5/3) wavelet filter, aiming to reduce the hardware complexity and size of the on-chip memory. This architecture consists of a control unit, a processor unit, two on-chip internal memories to speed up system operations, and an on-board off-chip external memory (Intel strata parallel NOR flash PROM). The 2-dimensinal discrete wavelet transform lifting scheme algorithm has been implemented using MATLAB program for both modules forward discrete wavelet transform (FDWT) and inverse discrete wavelet transform (IDWT) to determine suitable word length for DWT coefficients and the peak signal to noise ratio (PSNR) for the retrieved image. The decomposition algorithm of this transform is designed and synthesized with the VHDL language and then implemented on the FPGA Spartan 3E starter kit (XC3S500E) to check validation of results and performance of design.

Keywords*: Two dimensional discrete wavelet transform (2-D DWT), lifting scheme, (5/3) wavelet filter, and FPGA applications.

I. INTRODUCTION

The discrete wavelet transform (DWT) has become one of the most used techniques for signal analysis and image processing applications. The discrete wavelet transform (DWT) performs a multiresolution signal analysis which has adjustable locality in both time and frequency domains [1]. Due to it is well time–frequency characteristics, one of the most significant uses for (DWT) has been for image compression as in the (JPEG 2000). The (9/7) and (5/3) wavelet filters are employed as the default filters for lossy and lossless compression respectively [2]. Since the DWT is implemented by using convolution method which is based on filter bank structures, it requires large number of arithmetic computations and large storage area, features that are not desirable for either high speed or low power hardware applications [2]. The lifting scheme was introduced by Win Swelden in 1995 [4] to eliminate the need for multiple addition and multiplication processes necessary for convolving any filter with the image.

Many recent 2-D DWT architectures have been developed and implemented to reduce the number of slices, internal memory requirements, hardware complexity, and increase the design performance. The lifting scheme 2D DWT architecture that was developed in [2] presents a flexible architecture for serial-parallel based (5/3) filter to implement 1-D DWT and 2-D DWT for image size (256×256), the design was implemented by using Xilinx XCV600E device.

The other architecture in [3] was based on a new convolution approach that reduces the hardware complexity and multipliers delay, the design implemented on Xilinx vertex-II device.

The architecture in [6] presented the design that can be used for both lossy and lossless compression based on lifting scheme approach.

The other architecture in [7] proposed a lifting based 2-D DWT for biothogonal (9,7)/(4,3) filters that uses recursive pyramid algorithm, as a result of implementation the architecture has the (66.7%~88.9%) hardware utilization.

This paper focuses on the hardware implementation of the lifting scheme as applied for two dimensional discrete wavelet transform using the (5/3) lifting filter. The proposed architecture is designed by using VHDL language and implemented on FPFA Spartan 3E starter kit. The input image size is (256×256) pixel that cannot be possible to be stored in the internal block RAM. Because of the limited FPGA internal memory size in the Spartan 3E, so an external memory is used to store the original image. There is an on board 128Mbit Intel strata flash (parallel NOR flash PROM) which is used for image storing and all decomposition subbands. For result testing, the Xilinx chip scope tool is used as a validation tool. The Discrete Wavelet Transform (DWT) The basic (DWT) can be realized by convolution using the FIR (Finite Impulse Response) filter banks to do the transform [1]. The one-dimension (DWT) filter bank consists of two analysis filters, a low pass filter (LPF) and a high pass filter (HPF), which separate the frequency contents of input signal into the approximation (low frequency) coefficients and the details (high frequency) coefficients. The two dimensional (DWT) can be obtained by applying the one dimensional (DWT) along the rows and columns of the input image [7]. At the first level of computation, the input image is decomposed horizontally by applying one-dimensional (DWT) on each row to get two coefficients (L and H), then it is decomposed vertically by applying one-dimensional (DWT) on each column to get four wavelet coefficients (LL, LH, HL, and HH) as shown in Fig. 1.

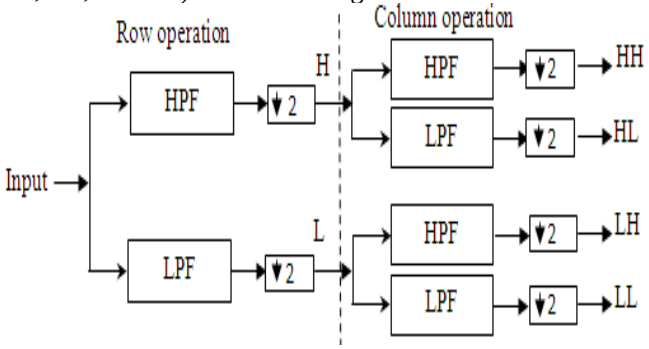

Fig 1. Block diagram of the 2-D DWT application [1].

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For multi-level decomposition the same operations mentioned above are performed on the (LL) subband as the input instead of the original image, giving pyramid wavelet transform.

II. THE LIFTING SCHEME

The Lifting scheme (LS) is a method to simplify performing the wavelet transform in an efficient way. The (LS) has some advantages when compared with classical filter banks method, such as the fewer and simpler arithmetic computations required, the simple and fast hardware implementation, the ease of inverse implementation, occupying less memory storage, in addition, the (LS) is more appropriate for high speed and low power applications such as the image/video processing applications. The disadvantages of lifting scheme that the multiplier and adder delays are longer than convolution ones (has longer critical paths) [3]. The (LS) can be performed by three steps: the split stage, the predict stage, and the update stage. In the split stage the input signal or image is separated into even and odd indexed samples. The predict stage computes the high pass filter coefficients representing the details subband. The update stage gives low pass filter coefficients which stands for the approximation subband of the DWT process. For (5/3) wavelet filter the predict and update stages are represented in following equations [4]:

$$D[2n+1] = X[2n+1] - 0.5(X[2n] + X[2n+2]) \quad (1)$$
$$A[2n] = X[2n] + 0.25(D[2n-1] + D[2n+1] \quad (2)$$

Where:
X[n]: is the input signal.
D[2n+1]: the details coefficients.
A[2n]: the approximations coefficients.

From lifting scheme wavelet transform equations, it is noticed that hardware design requires only adders and shifters instead of multipliers. Fig. 2 shows the lifting scheme 2-D DWT block diagram.

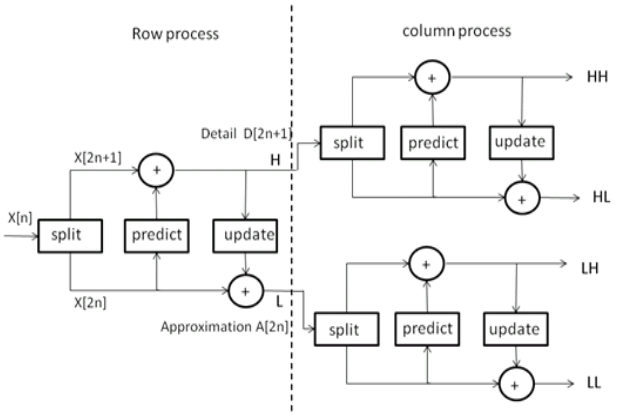

Fig 2. Block diagram for the two dimensional FDWT using lifting scheme.

III. PROPOSED ARCHITECTURE FOR DWT

This section presents and explains the overall design of a 2-D DWT module, hardware and software tools that are used for design simulation, implementation, and the output results verification. The following sections explain the main design steps, starting with word length, data type representation for hardware design, simulation and testing the results with MATLAB program. After that, the VHDL design used for DWT processor unit, arranging the on-chip internal memory units, and control unit are given. The chip scope program is used as a verification tool for checking and testing the application results.

A. Data Representation And Word Length:

At first, before designing the 2-D DWT processor, data type representation and image pixels word length must be taken into consideration. There are two ways for data representation with hardware design, either floating point or fixed point. By representing data in floating point method the results will be more accurate due to the greater range of numbers (32 bits or 64 bits), but this accuracy requires more silicon area on FPGA and needs more complex design [10]. Fixed point representation has the advantages of less silicon area on FPGA, and easier to implement a design [10]. So the fixed point method is used to represent the data. The most common representation for fixed point numbers is the 2´s complement, this type is appropriate with hardware design for arithmetic computations [10].

Another important consideration is the word length, which means, the number of bits per pixel. The original image data word length is 8-bits per pixel, this amount of bits is not enough for wavelet transform coefficients. It is observed that the retrieved image in inverse discrete wavelet transform has distortion, because of overflow condition. The overflow occurs when the addition operation result may be larger than can be held in the word length being used. In DWT the word length of wavelet coefficients will grow gradually in FDWT in each DWT level, and as the DWT levels are more. To select the appropriate word length, the MATLAB program is used for writing appropriate code to simulate the (5/3) wavelet filter in (FDWT) and (IDWT). With (FDWT) MATLAB program the cameraman picture of size (256×256×8) is used as original input image, it is analyzed for three levels of decomposition by using different word lengths, then the (IDWT) is used to reconstruct the retrieved image from the third level, as shown in the Fig. 3. Where, (a) original image, (b) one decomposition level, (c) two decomposition levels, and (d) three decomposition levels.

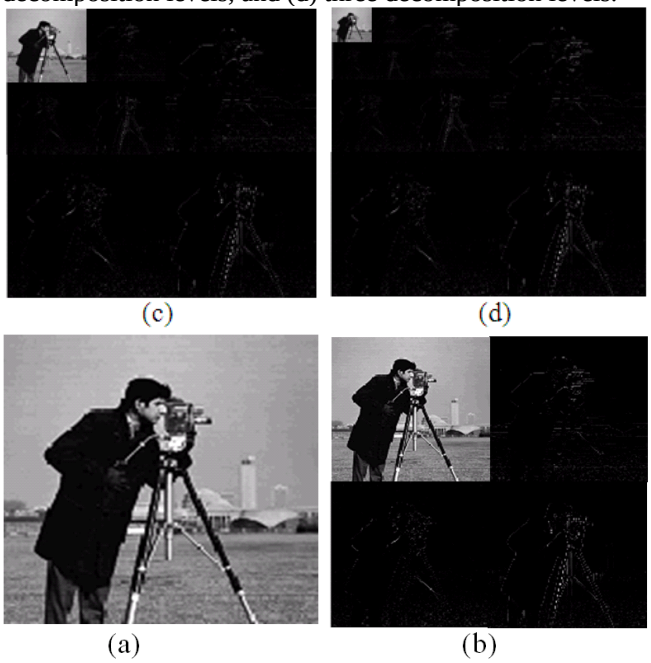

Fig 3. FDWT for three decomposition levels.

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The mean square error (MSE) and peak signal to noise ratio (PSNR) are used to determine the retrieved image accuracy. The table (1) shows word length effects on the PSNR values, this table is calculated by using MATLAB environment.

$$MSE = \frac{1}{n}\sum_{i=1}^{n}(pi - qi)^2 \qquad (3)$$

$$PSNR = 10\log\frac{(255)^2}{MSE} \qquad (4)$$

Where:
n: number of image pixels.
pi: original image pixel.
qi : retrieved image pixel.

Table (1). PSNR values for the images with three levels of decomposition.

images	PSNR				
	8bit	9bit	10bit	11bit	12bit
Cameraman	18.04	53.52	∞	∞	∞
Lena	17.88	72.03	∞	∞	∞
Peppers	13.98	38.94	∞	∞	∞
Goldhill	18.25	54.98	∞	∞	∞

From the table above, noticed that the 10bit data length make the (PSNR=Infinity) for three levels, the wavelet coefficients should be large enough to prevent the overflow, so the filter coefficients and the 2-D DWT coefficients are represented by 12bit.

B. Fdwt Architecture Design:

The block diagram of FDWT system design is shown in the Fig. 4. This system consists of four different components. These components are discussed in the following sections:

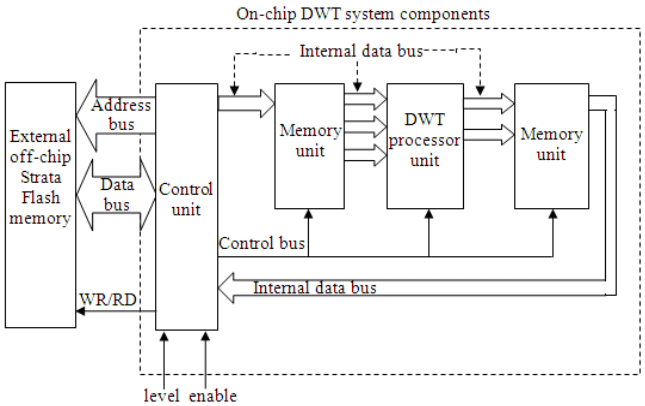

Fig. 4. Block diagram of the proposed architecture for FDWT.

B.1. INTERNAL MEMORY UNITS:

There are two internal on-chip memory units in the system design, each one has size (2N) for (N×N) image, these memory units are used as a cache memory, to speed up the DWT system assignments because the internal memory is faster than external memory. Each of these internal memory units is a single dual port block ram, therefore only one clock cycle is needed for reading or writing two words of data in two random memory locations. The memory units are also used to make an agreement between the 12 bits system word length and the 16 bits external memory word length.

The first memory unit works as a split stage for the lifting scheme wavelet transform, this unit works on separating the even indexed pixels from the odd indexed pixels. The separation process can be done by putting out even memory locations from (port A) output port, and odd memory locations from (port B) output port. This unit consists of a dual port block ram with two registers connected to the block ram output ports as shown in the Fig. 5.

This arrangement delivers three outputs (X[2n], X[2n+1], and X[2n+2]) form the memory unit at each clock cycle to the DWT processor unit. Since, the DWT processor has two outputs for each clock cycle the (LPF, and HPF) coefficients, a second memory unit is necessary. This memory unit is also a dual port block ram used as dual input ports and single output port. This unit brings out the wavelet coefficients toward the external memory.

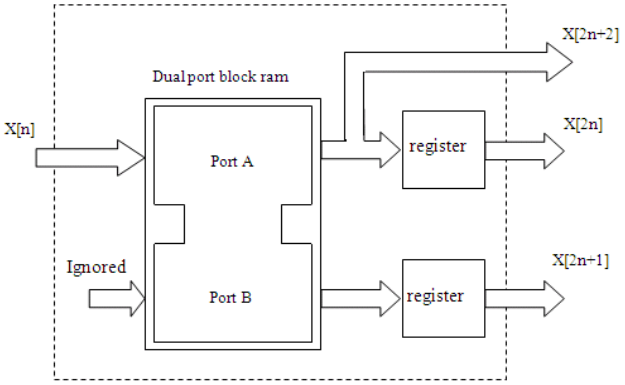

Fig. 5 Organization of the first memory unit.

B.2. DWT PROCESSOR UNIT:

This unit represents the hardware design of the (5/3) lifting scheme filter, it contains predict stage and update stage. The same unit is used for row operations and then for column operations. This unit has three input ports connected to the three output ports of the first memory unit, and has two output ports connected to the input ports of the second memory unit as shown in the Fig. 4. In the hardware implementation of the filter design there are three registers to store incoming data from the first memory unit (three input data per clock cycle). Four adders and two shifters are used instead of multipliers, also a register is used to store the previous value of the details coefficients (D[2n-1]) for the next computation according to the lifting equations (1), and (2).

B.3. CONTROL UNIT:

There are two duties for the control unit. The first, it controls the on-chip DWT system components, see Fig. 4, by providing control signals (read, write, status, and enable), also it gives the appropriate addresses for memories units, and controls the data flow in the proposed design. The second, it provides complete interface signals and buses with external memory (read, write, enable, address bus, and data bus). The control unit is designed with finite state machine (FSM) method. There are two input signals that are connected to the switches of the FPGA kit, these control signals must be asserted by the user before starting the system operations.

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First one is the DWT level signal, used to select the wanted decomposition levels. The Second is the enable signal, used to enable the system components to perform DWT operations. After setting the (enable and level) signals, the control unit is responsible for all system operations starting with reading image data from external memory, enable DWT processor unit operations, and writing DWT sub bands to the external memory.

B.4. EXTERNAL MEMORY (STRATA FLASH):

The external memory is the on board 128Mbit Intel strata flash (parallel NOR flash PROM). It is used for storing the original image and later the DWT coefficients. This memory is configured as 8 Mword (128Mbit), each memory location is of 16 bit word size, the strata flash memory has 23 bit memory address bus width, 16 bit data bus width, and three important control signals that must be taken in to consideration (chip select, output enable, and write enable).

The strata flash memory controller is designed by using the VHDL language to be appropriate for the proposed design. This controller is included in the proposed DWT control unit, already mentioned. There are some configurations on FPGA starter kit board that must be set properly to deal with strata flash, such as, the on board components that shares connections with strata flash memory which must be disabled, to ensure that only one data source is active at a time [8].

Another configuration is setting the on board FPGA mode jumpers, also see [8]. In this proposed design, the FPGA chip configured to the BPI Up (byte peripheral interface) mode, this means that the memory address starts at address (0) and increments through the address space.

The original image data is converted to hexadecimal format before storing it in the memory, the conversion operation is achieved by using a MATLAB program. In order to store the original image in the on board memory, the strata flash controller is used for writing image data file, in hexadecimal format, in the addressed memory locations. Then the DWT proposed architecture is downloaded on the FPGA chip to perform DWT operations and store wavelet coefficients in the strata flash memory.

V. APPLICATION RESULTS

A. FPGA Synthesize And Implementation:

The proposed architecture designed with VHDL is then synthesized, placed, and routed by using Xilinx ISE 10.1 software. The proposed design is implemented on the Xilinx (XC3S500E) chip using Spartan 3E FPGA starter kit. The grayscale cameraman picture with size (256×256) is stored as an original image in the on board strata flash memory. After implementing the proposed design on the FPGA device the resources utilization have been shown in the table (2), and the maximum operation frequency is 62.797MHz.

Table (2). The Device Utilization Summary.

Logic utilization	Used	available	utilization
Number of slices	1299	4656	27%
Number of slices flip flops	767	9312	8%

The Fig. 6 (a) and (b) show the RTL schematic and its inner view obtained from the Xilinx ISE of the implemented DWT after performing the synthesis.

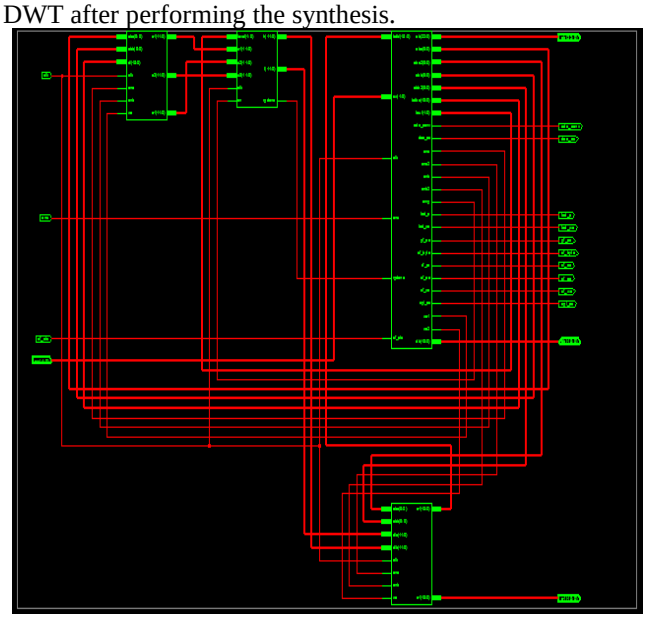

Fig. 6 (a) RTL schematic view of the DWT design.

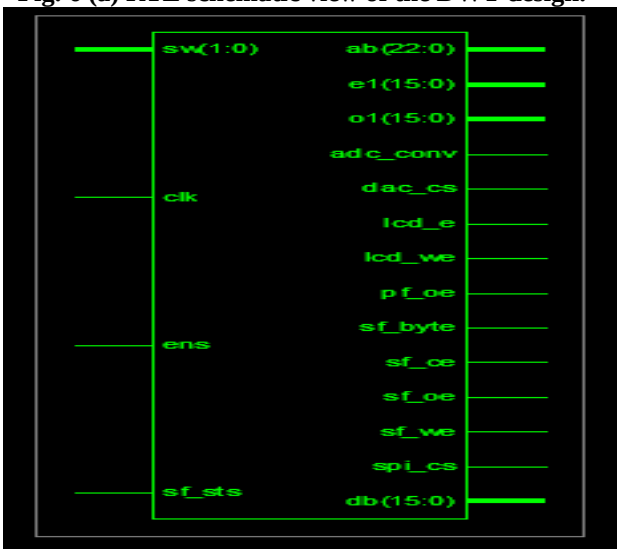

Fig. 6 (b) RTL schematic inner view of the DWT design.

B. Results Verification And Checking:

The results are checked by using chipscope program, the chip scope is a xilinx product that inserts a software logic analyzer onto the FPGA chip, it is used for verification of the FPGAs designs. The chipscope product can be integrated in the ISE project as a component, it can be connected to inputs, outputs, and intermediate signals of the design that are implemented on the FPGA device. In this research, after implementing the proposed design on the FPGA device, there are two control signals must be set, the level signal (it is input to the control signal unit) giving that the wanted decomposition levels number, and the enable signal which must be switched to logic (1) in order to start the proposed design operations. During the proposed design operations for computing the DWT coefficients, the Xilinx chipscope program was used as a validation tool once the system was running in a Spartan 3E starter kit. Fig. 7 shows the signals of the proposed design.

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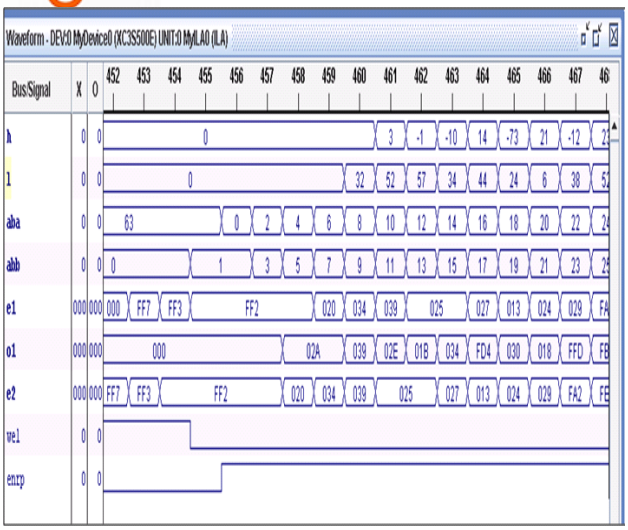

Fig. 7 The chipscope program shows proposed design signals

C. Reading The External Memory:

After completing the DWT operation, all the subbands are stored in the external on board Strata Flash memory. The PicoBlaze application [9] is used for reading strata flash memory contents, this design is loaded on the FPGA chip to provide serial data communication between the Spartan 3E kit and the personal computer through RS-232 serial link. The Hyper Terminal program is adequate for managing this communication. Once the PicoBlaze application is loaded into the Spartan 3E, a new hyper terminal session can be started. This session needs configuring the serial port setting (baud rate, data bits, parity, stop bits, and flow control) before connection with the PicoBlaze application. When a correct connection is established between Spartan 3E (PicoBlaze) and the personal computer (Hyper Terminal) a list of commands will be appeared on the Hyper Terminal program, from this list the read command will be used for reading strata flash memory contents, and storing the data into a text file with hexadecimal format. Then the MATLAB program is used for some duties, such as reading and separating the text file contents according to the DWT subbands, and applying IDWT on each level subbands in order to get the retrieved image. Fig. (8) shows the original image and the retrieved image. The PSNR between the original image and retrieved image can be computed by using equations (3), and (4) giving that the PSNR=52.1122db.

(a) (b)

Fig. 8 Shows (a) original image, (b) retrieved image.

VI. CONCLUSIONS AND FUTURE WORKS

The lifting scheme proves to be a very good alternative for the convolution in the DWT applications on FPGA. It gives faster, easier, less demanding, and more effective FPGA solutions. The best word length for DWT coefficients proved to be 12 bits which gave highest PSNR and is suitable for three DWT levels as used and for higher levels also. The image is saved in the strata flash prior to arrange for DWT, and the subbands coefficients are then stored as they result during the hardware application also in the same chip. The strata flash was used because it is easier to be reached and implemented. DWT hardware application was tested using chip scope. While data verification was performed using the Xilinx PicoBlaze in conjunction with the PC hyper terminal. IDWT was performed using MATLAB facilities since no hardware architecture is available till now for it. It is suggested to test this design for larger image, say 512×512, and using more DWT levels, say 4,5..etc. Also it is needed to establish another hardware design for the IDWT, where it is expected to get better PSNR due to using the same environment for both DWT activities.

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