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Design of Low Power and Area Efficient Architecture for Reconfigurable FIR Filter

N.Durairajaa, J.Joyprincy, M.Palanisamy

Abstract: ***Finite Impulse Response (FIR) filters are widely applied in multi-standard wireless communications. These filters provide linear phase and absolute stability. The FIR offers a low sensitivity for the coefficient quantization errors. These properties increase the usage of FIR filter. In this paper, reconfigurable digital filter architecture is proposed. The approach is well suited if the filter order is fixed. The filter is dynamically reconfigured by changing the filter order. The order is changed by turning of the multiplier whose inputs are mitigate to be eliminated. The complexity of linear phase FIR filters is dominated by the number of adders (sub-tractors) in the coefficient multiplier. The Common Sub-expression Elimination (CSE) algorithm reduces number of adders in the multipliers and dynamically reconfigurable filters can be efficiently implemented. The proposed filter architectures offers power and area reduction over the existing FIR filter implementation.***

Index Terms: Approximate filtering, low power filter, reconfigurabledesign, commonsubexpressionelimination(CSE).

I. INTRODUCTION

The explosive growth in mobile computing and portable multimedia applications has increased the demand for low power digital signal processing (DSP)system. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$y(n) = \sum_{k=0}^{N-1} c_k x(n-k) \qquad (1)$$

where N represents the length of FIR filterc_k the kth coefficient, and $x(n-k)$ the input data at time instant $n-k$.

In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary.

Many previous efforts for reducing power consumption of FIR filter generally focus on the optimization of the filter coefficients while maintaining a fixed filter order [1]–[3]. In those approaches, FIR filter structures are simplified to add and shift operations, and minimizing the number of additions/subtractions is one of the main goals of the research. However, one of the drawbacks encountered in those approaches is that once the filter architecture is decided, the coefficients cannot be changed; therefore, those techniques are not applicable to the FIR filter with programmable coefficients. Approximate signal processing techniques [4] are also used for the design of low power digital filters [5], [6]. In [5], filter order dynamically varies according to the stop band energy of the input signal. However, the approach suffers from slow filter-order adaptation time due to energy computations in the feedback mechanism. Previous studies in [6] show that sorting both the data samples and filter coefficients before the convolution operation has a desirable energy-quality characteristic of FIR filter. However, the overhead associated with the real-time sorting of incoming samples is too large. Reconfigurable FIR filter architectures are previously proposed for low power implementations [7]–[9] or to realize various frequency responses using a single filter [10]. For low power architectures, variable input word-length and filter taps [7], different coefficient word-lengths [8], and dynamic reduced signal representation [9] techniques are used. In those works, large overhead is incurred to support reconfigurable schemes such as arbitrary nonzero digit assignment [7] or programmable shift [8]. In higher order filters are required for channelization and consequently the complexity and power consumption of the receiver will be handsets, where its full utilization is possible, low power and low area implementation of FIR channel filters is inevitable. In [11], the filter multiplications are done via state machines in an iterative shift and add component and as a result of this there is huge savings in area. For lower order filters, the approach in [11] offers good trade-off between speed and area.

In this paper, we propose a simple yet efficient low power re-configurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system. The primary goal of this work is to reduce the dynamic power of the FIR filter.

The main contributions are summarized as follows. 1) A new reconfigurable FIR filter architecture with real-time input and coefficient monitoring circuits is presented. Since the basic filter structure is not changed, it is applicable to the FIR filter with programmable coefficients or adaptive filters. 2) We provide mathematical analysis of the power saving and filter performance degradation on the proposed approach. The analysis is verified using experimental results, and it can be used as a guideline to design low power reconfigurable filters.

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* Correspondence Author
N.Durairajaa, Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamilnadu, India.
J.Joyprincy, Electronics and Communication Engineering, SNS College Of Technology, Coimbatore, Tamilnadu, India.
M.Palanisamy, Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamilnadu, India.

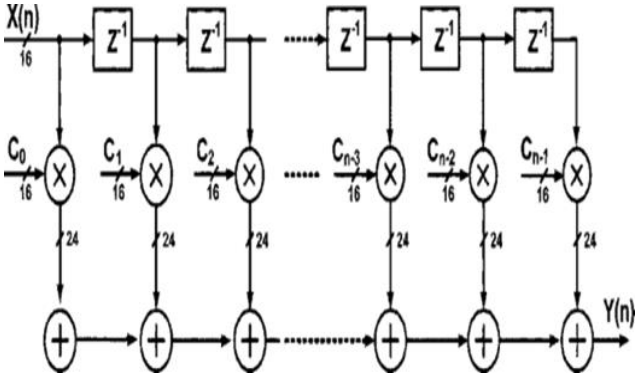

Fig. 1. Architecture of the direct form FIR filter

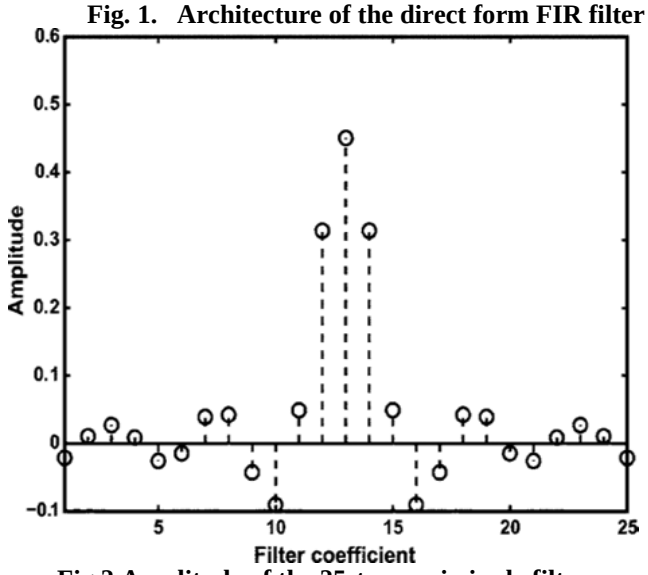

Fig.2.Amplitude of the 25-tap equi-ripple filter coefficients.

The rest of the paper is organized as follows. In Section II, the basic idea of the proposed reconfigurable filter is described. Section III presents the reconfigurable hardware architecture and circuit techniques used to implement the filter. Section VI presents common sub-expression elimination(CSE)method. Discussions on the design considerations and mathematical analysis of the proposed reconfigurable FIR filter are presented in Section V. Section VI shows the numerical results followed by conclusions in Section VI.

II. RECONFIGURABLE FIR FILTERING TO TRADE OFF FILTER PERFORMANCE AND COMPUTATION ENERGY

As shown in Fig. 1, FIR filtering operation performs the weighted summations of input sequences, called as convolution sum, which are frequently used to implement the frequency selective—low-pass, high-pass, or band-pass—filters. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of multipliers, significant power savings can be achieved. However, performance degradation should be carefully considered when we change the filter order.

Fig. 2 exemplary shows the coefficients of a typical 25-tap low-pass FIR filter. The central coefficient has the largest value—the coefficient has the largest value in the 25-tap FIR filter and the amplitude of the coefficients generally decreases as k becomes more distant from the centretap. The data inputs x(n) of the filter, which are multiplied with the coefficients, also have large variations in amplitude. Therefore, the basic idea is that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers is proportionately small; thus, turning off the multiplier has negligible effect on the filter performance. For example, since two's complement data format is widely used in the DSP applications, if one or both of the multiplier input has negative value, multiplication of two small values gives rise to large switching activities, which is due to the series of 1's in the MSB part. By canceling the multiplication of two small numbers, considerable power savings can be achieved with negligible filter performance degradation.

In the fixed point arithmetic of FIR filter, full operand bit-widths of the multiplier outputs is not generally used. In other words, as shown in Fig. 1, when the bit-widths of data inputs and coefficients are 16, the multiplier generates 32-bit outputs. However, considering the circuit area of the following adders, the LSBs of multipliers outputs are usually truncated or rounded off, (e.g., 24 bits are used in Fig. 1) which incurs quantization errors. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible. In the following, we denote threshold of input and threshold of coefficient as x_{th} and c_{th}, respectively. By threshold, we mean that when the filter input x(n) andcoefficient c_k are smaller than x_{th} and c_{th}, respectively, the multiplication is canceled in the filtering operation. When we determine x_{th} and c_{th}, the trade-off between filter performance and power savings and should be carefully considered

III. ARCHITECTURE OF RECONFIGURABLE FIR FILTER

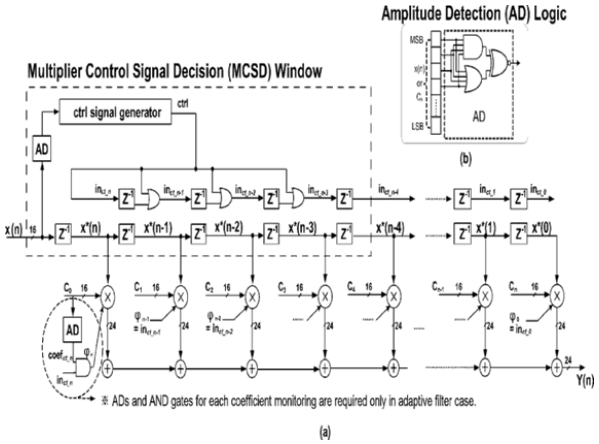

Fig.3.(a) Proposed reconfigurable FIR filter architecture. (b) Amplitude detection logic (AD).

In this section, we present a direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Fig. 3(a). In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Fig.3(b) is used. When the absolute value of x(n) is smaller than the threshold x_{th}, the output of AD is is set to "1".The design of AD is depedent on the input threshold x_{th}, where the fan in's of AND and OR gate are decided by x_{th}.

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If x_{th} and c_{th} have to be changed adaptively due to designer's considerations, AD can be implemented using a simple comparator.

Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances. In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then, if the amplitude of input x(n) abruptly changes for every cycle, the multiplier will be turned on and off continuously, which incurs considerable switching activities. The Multiplier control signal decision window (MCSD) in Fig. 3(a) is used to solve the switching problem. Using *ctrl* signal generator inside MCSD, the number of input samples consecutively smaller than x_{th} are counted and the multipliers are turned off only when m consective input samples are smaller than x_{th}. Here,m means the size of MCSD [in Fig.3(a),m is equal to 4].

Fig.4(a) shows the ctrl signal generator design. As an input smaller than x_{th} comes in and AD output is set to "1",the counter is counting up. When the counter reaches m, the ctrl signal in the figure changes to "1",which indicates that m consective small inputs are monitored and the multipliers are ready to turn off. One additional bit, int_{c-n} accompanies with input data all the way in the following flip-flops indicate that the input sample is smaller than x_{th} and the multiplication can be canceled when the coefficient of the corresponding multiplier is also smaller than c_{th}.

Once the in_{ct-n} signal is set inside MCSD and holds the amplitude information of the input. A delay component is added in front of the first tap for the synchronization between x*(n) and in_{ct-n} in Fig.3(a) since one clock latency is needed due to the counter in MCSD.

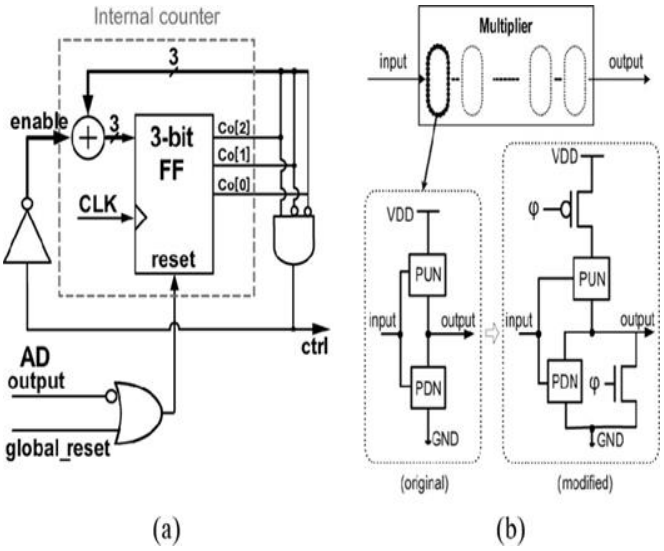

Fig.4.(a) Schematic of ctrl signal generator. Internal counter sets signal to"1"when all input samples inside MCSD are similar than x_{th} (m=4 case).(b) Modified gate schematic to turn off multiplier.

In case of adaptive filters, additional ADs for monitoring the coefficient amplitudes are required as shown in Fig. 3(a). However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed.

When the amplitudes of input and coefficient are smaller than x_{th} and c_{th}, respectively, the multiplier is turned off by setting n signal[Fig.3(a)] to"1". Based on the simple circuit technique [11] in Fig. 4(b), the multiplier can be easily turned off and the output is forced to "0". As shown in the figure, when the control signal n is "1", since PMOS turns off and NMOS turns on, the gate output is forced to "0" regardless of input. When is "0", the gate operates like standard gate. Only the first gate of the multiplier is modified and once the is set to "1,there is no switching activity in the following nodes and multiplier output is set to "0".

The area overheads of the proposed reconfigurable filter are flip-flops for in_{ct-n} signals, AD and ctrl signal generator inside side MCSD and the modified gates in Fig. 4(b) for turning off multipliers. Those overheads can be implemented using simple logic gates, and a single AD is needed for input monitoring as specified in Fig. 3(a). Consequently, the overall circuit overhead for implementing reconfigurable filter is as small as a single multiplier.

IV. COMMON SUBEXPRESSION ELIMINATION (CSE) METHOD

4.1 BASIC CONCEPT

The complexity of linear-phase FIR filters is dominated by the complexity of coefficient multipliers. The number of adders (sub-tractors) used to implement the multipliers determines the complexity of the FIR filters. Many approaches including coefficient coding using efficient arithmetic schemes, coefficient optimization techniques, distributed arithmetic techniques, Read Only Memory (ROM) based signs, and common sub-expression elimination techniques have been proposed. Among these, the CSE techniques in [Hartley, R.I. 1996] produced the best hardware reduction. It is well known that CSE methods based on canonical signed digit coefficients reduce the number of adders required in the multipliers of FIR filters.

A new CSE algorithm using binary representation of coefficients for the implementation of higher order FIR filter with a fewer number of adders than CSD-based CSE methods is used. The CSE method is more efficient in reducing the number of adders needed to realize the multipliers when the filter coefficients are represented in the binary form. The observation is that the number of unpaired bits (bits that do not form Common Sub-expressions (CSE)) is considerably few for binary coefficients compared to CSD coefficients, particularly for higher order FIR filters. As a result, the proposed binary-coefficient based CSE method offers good reduction in the number of adders in realizing higher order filters. The reduction of adders is achieved without much increase in critical path length of filter coefficient multipliers.

The goal of CSE is to identify multiple occurrences of identical bit patterns that are present in the CSD representation of coefficients and to eliminate these redundant multiplications to minimize the number of Logical Operators (LOs). (LOs represent the adders required in computing the sum of partial products in the multiplier, which determine the area and power requirements of the filter circuit. In graphical algorithm is to identify and eliminate 2-b sub-expressions). In the CSE method was optimized to realize high-speed FIR filter implementations by reducing Logic Depth (LD). (LD is defined as the number of adder-steps in a maximal path of decomposed multiplications).

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A more efficient method eliminated the most commonly occurring 2-b sub-expressions. As an additional criterion in the sub-expression identification process, an estimation of a latch count improvement was also considered. A modification of the 2-b CSE technique in to identify the proper patterns for elimination of redundant computations and to maximize the optimization implemented.

The two key metrics that determine the complexity of coefficient multiplications in FIR filters are the number of LOs and the LD. LD is the number of adder steps in a maximal path of decomposed multiplications, which determines the speed of filtering operations. Therefore, the focus of low-complexity FIR filter implementation algorithms is on reducing the number of LOs and LD in coefficient multipliers.

A method for optimizing the CSE method in to implement higher order channel filters for wideband receivers with less complexity. This technique is based on the extension of conventional two nonzero bit (2-b) Common Sub-expressions (CSs) in to form three nonzero bit and four nonzero bit Super Sub-expressions (SSs) (called 3-b and 4-b SS, respectively) by exploiting identical shifts between a 2-b CSs and a third nonzero bit or between two 2-b CSs. The method in is targeted to reduce the number of full adders needed to realize each adder in the coefficient multiplier. The CSE techniques utilize the CSs that occur within the CSD representation of the filter coefficients called Horizontal Common Sub-expressions (HCSs) and that occur among the adjacent coefficients called Vertical Common Sub-expressions (VCSs) to eliminate redundant computation.

4.2 HORIZONTAL CSE (HCSE)

Horizontal CSE utilizes CSs that occur within each coefficient to eliminate redundant computations. The coefficient $h_k = 0.10\text{-}1010101010010\text{-}1$ is used as an example to illustrate the HCSE method. In direct implementation (i.e., implementation of the multiplier using shifts and adds without using CSE) the filter tap output is

$$Y_k = 2^{-1}x_1 - 2^{-3}x_1 + 2^{-5}x_1 + 2^{-7}x_1 + 2^{-9}x_1 + 2^{-11}x_1 + 2^{-14}x_1 - 2^{-16}x_1 \quad (4.1)$$

Where x1 is the input signal. It requires seven LOs (adder and/or sub-tractor) to implement (3.1). The bit patterns [1 0 1] and [1 0 −1] are repeated twice in h_k which can be expressed as CSs ($x_2 = x_1 + 2^{-2}x_1$ and $x_3 = x_1 - 2^{-2}x_1$, respectively).

Using CSs, the output (3.1) can be expressed as

$$Y_k = 2^{-1}x_3 + 2^{-5}x_2 + 2^{-9}x_2 + 2^{-14}x_3 \quad (4.2)$$

Note that only five LOs two LOs for CSs x_2 and x_3 three LOs are needed for HCSE implementation, which is a saving of two LOs when compared to direct implementation.

4.3 VERTICAL CSE (VCSE)

The Vertical CSE utilizes CSs that exist across adjacent coefficients to eliminate redundant computations. The VCSE technique can be illustrated using the four-tap symmetrical filter coefficient set given in Table 3.1. The numbers in the first row in Table 3.1 represent the number of bitwise right shifts. The coefficient multipliers are realized by employing vertical CSs of [1 1] and [1 −1] that occurs between h0 and h1 indicated inside the circles in Table. 3.1. The VCS of [1 1] can be expressed as $x_4 = x_1 + x_1[-1]$ and the VCS of [1−1] can be expressed an $x_5 = x_1 - x_1[-1]$, where $x_1[-1]$ represents the input x_1 delayed by one unit.

By using VCSs, the output y0 corresponding to coefficients h0 and h1 can be expressed as

$$y_0 = 2^{-1}x_4 + 2^{-3}x_5 - 2^{-6}x_4 + 2^{-8}x_1. \quad (4.3)$$

Table 4.1 VCSE in FIR Filter Coefficients

	1	2	3	4	5	6	7	8
h_0	1	0	1	0	0	-1	0	1
h_1	1	0	-1	0	0	-1	0	0
$h_2=h_1$	1	0	-1	0	0	-1	0	0
$h_3=h0$	1	0	1	0	0	-1	0	1

V. DESIGN CONSIDERATIONS AND MATHEMA-TICAL ANALYSIS ON THE RECONFIGURABLE FIR FILTER

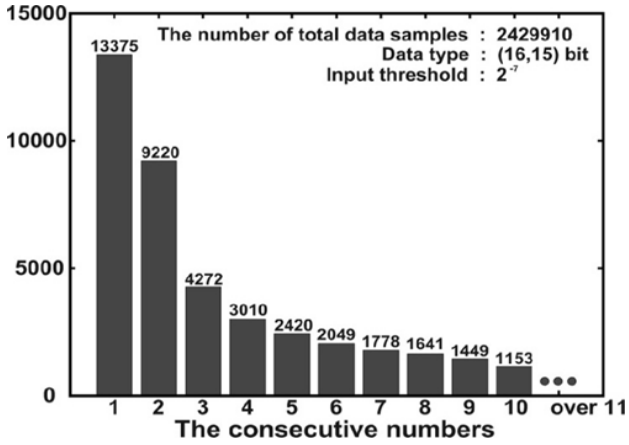

Fig.7.comparision results between analysis and experimental results.

In this section, we present design considerations on the pro-posed reconfigurable FIR filter. Mathematical analysis which describes the trade-off between power savings and filter performance degradation is also presented in this section

A. Design considerations

In following discussions, as a metric of power savings, we use the power consumption ratio, , which means the ratio of the reconfigurable filter power consumption to the conventional filter power(p_{reconf} /$p_{convenf}$). As a measure of filter performance degradation, we use mean-square error(MSE) between the proposed reconfigurable filter output and original filter output .

The most important factors that have a large effect on the proposed filter performance and power consumption are x_{th} and c_{th}. When x_{th} and c_{th} are set too large, it can give rise to large, it can give rise to large power savings with considerable distortion in the filter output. On the other hand, if x_{th} and c_{th} are too small, power savings become trivial.

Fig.5 Number of consective input samples whose amplitude are smaller than x_{th} in sound and speech signals.

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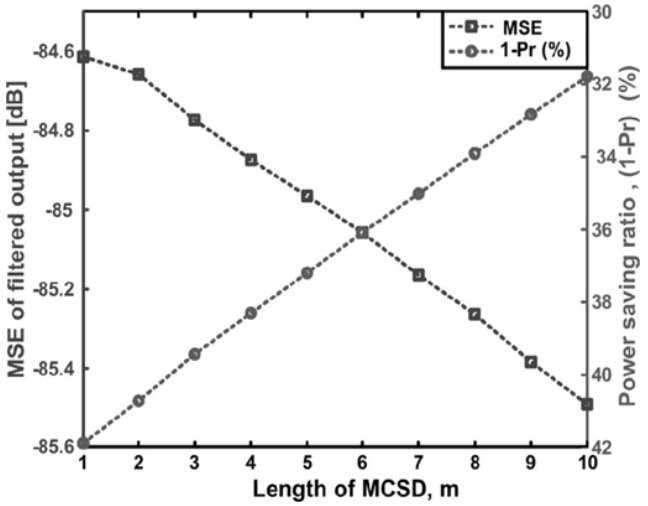

Fig.6.Power saving ratio versus performance degradation percentage change for different MCSD length, m in the case of 75-tap equi-ripple filter

The other one to be considered is , the length of MCSD. Fig. 5 shows the number of input samples whose (x axis) consecutive input values are smaller than input threshold. The input signals used in the simulation are more than ten samples of sounds and speeches. In Fig. 5, if we choose a specific value in the axis, the total number of canceled multiplications is the accumulated number of samples from the selected value to the right.

Therefore, if becomes larger, the number of input samples that make multipliers turned off decreases; then, power reduction becomes smaller and filter performance degradation becomes lower as well. Fig. 6 shows the trade-off between the power ratio(1-pr) and the MSE for different m values in case of a 75-tap equi-ripple filter with x_{th} and c_{th} and c_{th} of 2^{-7}.

B. Mathematical analysis

Mathematical modeling on the power savings and performance degradation of the proposed reconfigurable FIR filter are presented in this subsection. Detailed derivations can be found in the Appendix. Assuming the input signal as stationary random Markov process as commonly used in communication systems [12],when the future state is independent of its past states and conditionally dependent only on the present state, power saving ratio,$(1\text{-}p_r)$,can be expressed as,

$$1 - P_r = \Pr_c \Pr_x P_{cut2cut}^{m-1} \quad (2)$$

where $\Pr_c (= \Pr\{|c_k| \le c_{th}\})$ and $\Pr_x (= \Pr\{|x(n-k)| \le x_{th}\})$ are the probability that the amplitude of the coefficient and input signal are less than the given thresholds, i.e., $|c_k| \le c_{th}$ and $|x(n-k)| \le x_{th}$, respectively. $P_{cut2cut}$ is the conditional probability meaning that future state of input samples is smaller than x_{th} under present state being also smaller than x_{th} i.e., $\Pr\{|x(n)| \le x_{th} | |x(n-1)| \le x_{th}\}, \forall\, n$.

VI. NUMERICAL RESULTS

In this section, we have designed and implemented various types of reconfigurable FIR filters. Mathematical analysis in the previous section are verified by comparing with the experimental results.

A. Reconfigurable FIR Filter Specifications

Following are the specifications on the FIR filters implemented.

- Input sequence and coefficients are 16-bit data with fractional part of 15 bit. Hence, the data range is [-1,1].
- The output of the multiplier in the FIR filter are quantized into 16bit and the final filter output is 24bit.
- We use 2^{-7} as an input threshold, x_{th}, and coefficient threshold, c_{th}. The value of MCSD window length, m ,are differently assigned for the filters. The values of x_{th},c_{th}, and m can be controlled by users considering the performance degradation and power savings trade-off presented in section V-B.

B. Numerical Results

The proposed reconfigurable FIR filters are very-log coded and synthesized using TSMC 0.25 CMOS technology. The first gate of each of the multipliers is replaced with the modified gates as shown in Fig. 4(b). Power consumption is measured in the spice level simulation using nanosim [13] with the operation frequency of 100MHz, 2.5-V supply voltage.

TABLE I. Average Power Saving Ratio(1-P_r)(%),The Average Mse And Smr For Various Filter Types In Speech Signal Case

type	25taps (ω_p = 0.10, ω_s = 0.38, R_a = -70dB)				50taps (ω_p = 0.10, ω_s = 0.26, $R_a \simeq$ -70dB)				75taps (ω_p = 0.10, ω_s = 0.20, $R_a \simeq$ -70dB)			
	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)
Equi-ripple	3	19.18%	-88.74	49.30	3	31.84%	-88.29	48.75	3	39.45%	-84.77	45.19
Least-squares	3	19.78%	-88.76	49.32	3	31.83%	-88.49	48.95	3	41.19%	-86.29	46.71
type	25taps (ω_p = 0.10, ω_s = 0.20, R_a = -30dB)				50taps (ω_p = 0.10, ω_s = 0.155, $R_a \simeq$ -30dB)				75taps (ω_p = 0.10, ω_s = 0.135, $R_a \simeq$ -30dB)			
	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)
Equi-ripple	3	7.61%	-95.12	55.34	3	17.53%	-84.67	45.16	5	26.02%	-82.55	42.71
Least-squares	3	7.02%	-94.33	54.54	3	22.57%	-88.41	48.79	5	30.31%	-82.93	43.25
type	25taps (ω_p = 0.10, ω_s = 0.20, R_a = -20dB)				50taps (ω_p = 0.10, ω_s = 0.13, $R_a \simeq$ -20dB)				75taps (ω_p = 0.10, ω_s = 0.12, $R_a \simeq$ -20dB)			
	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)
Equi-ripple	3	14.68%	-92.17	51.86	3	9.73%	-94.22	54.92	3	17.64%	-88.43	48.60
Least-squares	3	7.02%	-93.61	53.90	3	14.93%	-86.57	46.96	5	28.69%	-80.20	40.57
type	25taps (ω_c = 0.12)				50taps (ω_c = 0.12)				75taps (ω_c = 0.12)			
	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)	m	1-P_r (%)	MSE (dB)	SMR (dB)
Hamming	4	24.54%	-91.42	51.63	4	33.64%	-90.42	50.72	4	41.92%	-80.78	41.08
Bohman	3	24.94%	-99.56	59.79	3	37.04%	-86.47	46.75	3	42.48%	-87.00	47.30

[1] ω_p : normalized passband, ω_s : stopband edge frequency, ω_c : cut-off frequency R_a : stopband attenuation

Table I shows the average power saving ratio,1-P_r,and average MSE of filter output for the implemented FIR filters. As shown in the table average power saving is up to 41.9% in case of 75-tap hamming filter. MSE values in the table clearly shows the minor degradation in the filter performance. Our mathematical analysis on power saving and filter performance degradation(MSE) was also compared with the experimental results for various reconfigurable filters as seen in Fig.7.We can notice from that the difference between the mathematical modeling and experimental results are very small. To analyze the filter performance degradation, we define signal power to MSE ratio of the filter output (SMR) considering the effective ratio of the desired signal and the distorted error signal power as

$$\mathrm{SMR} = \frac{\sigma_y^2}{\sigma_e^2} \approx \frac{\sum_{k=0}^{N-1}\sum_{k=0}^{N-1} c_k c_h r(h-k)}{\Pr_c^2 \sum_{\substack{k=0 \\ k\in C_{tc}}}^{N-1}\sum_{\substack{h=0 \\ h\in C_{tc}}}^{N-1} c_h c_k r_x(h-k) prob_{cut}(x_{th}, |h-k|, m)}. \quad (4)$$

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Table I also presents the SMR results of various filters. For most of the cases, the SMR is larger than 45 dB, meaning that MSE is almost ignorable. For given applications, if SMR is comparable or larger than the signal to quantization error power ratio or the SNR of a given system, which are usually less than 30 dB [12], the performance degradation of proposed reconfigurable FIR filter can be considered negligible. The area overhead to support the proposed reconfigurable scheme is around 5.3% in case of 25-tap filter and it is even smaller for 50- and 75-tap filters, which are shown in Table II. Fig. 8 also illustrates the filter order changes due to canceling multiplications according to the input samples' amplitudes.

TABLE II. Area Comparision Between Reconfigurable And Conventional Fir Filters

Parameter	Conventional	Reconfigurable Filter	CSE Based Reconfigurable
No. of Gate counts	22,362	28,582	16,255

As a hardware area metric, C(tap) in table III presents the number of 2-input and gate counts per one filter tap. Our proposed filter shows larger power savings than the filters in [5] consumes less power than our proposed filter; however, MSE is even larger. Under the similar 1-P_r(around 41.9%) obtained by adjusting parameter values, our proposed filter has much less MSE as described using parenthesis in Table III.

Phonetic signal processing system is a good application to use the proposed reconfigurable filtering approach. Voice signal is usually composed of considerable portions of data samples with small amplitude. Though we focused on the FIR filters with fixed coefficients in this work, our proposed approach can be extended to the adaptive filter cases, where both data inputs and coefficients amplitude should be monitored simultaneously. It is used to audio and video signal processing systems

TABLE III
COMPARISION OF POWER REDUCTION OF OUR PROPOSED 75-TAP HAMMING FILTER WITH PREVIOUS WORKS

Ref.	Filter Description	Tech [μm]	Total Power	$P(tap)$	$1 - Pr$	MSE (dB)	$C(tap)$
[5]	75taps, 16 x 16	0.25	423mW @ 2.5V, 100MHz	5.64	71.15% (41.98%)	-45.91 (-49.49)	-
[7]	Equiv. 2.88 8 x 8	0.35	16.5mW @ 2.5V, 86MHz	19.03	-	-	234.6
[9]	8taps, 10 x 10	0.5	240mW @ 10MHz	-	39%	-	-
[14]	48taps, 16 x 12	0.25	0.28mW @ 2.5V, 44.1KHz	23.5	29%	-	215.5
our work	75taps, 16 x 16	0.25	653mW @ 2.5V, 100MHz	8.46	41.92%	-80.78	202.2

VII. CONCLUSION

In this paper, we propose a low power reconfigurable FIR filter architecture to allow efficient trade-off between the filter performance and computation energy. In the proposed reconfigurable filter, the input data are monitored and the multipliers in the filter are turned off when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Therefore, the proposed reconfigurable filter dynamically changes the filter order to achieve significant power savings with minor degradation in performance. According to the mathematical analysis, power savings and filter performance degradation are represented as strong functions of MCSD window size, the input and coefficient thresholds, and input signal characteristics.

Numerical results show that the proposed scheme achieves power savings up to 41.9% with less than around 5.34% of area overhead with very graceful degradation in the filter output. when the CSE method is used in the proposed approach the area overhead can be well reduced. The proposed approach can be applicable to other areas of signal processing, where a proper trade-off between power savings and performance degradation should be carefully considered. The idea presented in this paper can assist in the design of FIR filters and its implementation for low power applications.

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AUTHOR PROFILE

N.Duraiarjaa is pursuing his B.E degree in Electronics and Communication Engineering at SNS college of technology,Coimbatore

J.Joyprincy is pursuing her B.E degree in Electronics and Communication Engineering at SNS college of technology,Coimbatore

M.Palanisamy is pursuing his B.E degree in Electronics and Communication Engineering at SNS college of technology,Coimbatore

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