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Design and Analysis of High-performance Double Edge Triggered D-Flip Flop

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Abstract*: The power consumption of a system is a crucial parameter in modern VLSI circuits especially for low power applications. This paper proposed a new Double Edge Triggered D-Flip Flop (DETFF) which is suitable for low power applications. The proposed DETFF is having less number of clocked transistors than existing designs. The proposed DETFF is simulated with different clock frequencies ranging from 1MHz to 2GHz. Simulation results show lowest average power and least delay than existing designs. Further, the average power and the PDP are improved by 77.23% and 89.11% when compared with existing design respectively, which claims that proposed design is suitable for low power and high performance applications.

***Index Terms*: DETFF, power, delay, PDP**

I. INTRODUCTION

Technology scaling of a transistor feature size has provided a remarkable innovation in silicon industry for the past few decades. Designers are striving for small silicon area, higher speed, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. With the increasing use of mobile devices, consumer electronics markets demand a stringent constraint on reducing the power dissipation. In order to reduce the complexity of circuit design, a large proportion of digital circuits are designed to be synchronous circuits.

The most popular synchronous digital circuits are edge triggered flip-flops. The total clock related power consumption in synchronous VLSI circuits is due to power consumption in the clock network, power consumption in the clock buffers, and power consumption in the flip-flops [3]. D-type flip-flop's (DFF's) are one of the most fundamental building blocks in modern VLSI systems and it contributes a significant part of the total power dissipation of the system [12]. The design for low power issues can't be overcome without precised power prediction and optimization tools. Therefore, there is a critical need for certain tools to calculate power dissipation during the design to meet the power constraints to ignore the costly redesign effort. Power consumption is affected by many factors, $P = \alpha C V^2 f$ [5]. Voltage scaling is the most effective way to decrease power consumption, since power is proportional to the square of the voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage power to increase exponentially. By using double-edge triggered flip-flops (DETFFs), the clock frequency can be significantly reduced ideally, cut in half while preserving the rate of data processing.

The DETFF design aims at saving energy both on the distribution network (by halving the frequency) and flip-flops. It is preferable to reduce circuits' clock loads by minimizing the number of clocked transistors. A simple DETFF is implemented with about 50% extra transistors than the traditional SET flip flop, however, this issue is being resolved in recent intensive researches. It motivates to use DETFF for larger and complicated designs, especially for application specific integrated circuits (ASIC) design [13]. Several flop-flops have been proposed in the literature. The main attention has been in improving the performance of the VLSI circuits.

This paper is organized as follows: Section II explains the conventional DETFF circuits and a newly proposed DETFF circuit. The nominal simulations along with analysis are discussed in Section III. Results and performance for newly proposed design and conventional designs are compared in terms of average power, delay and PDP in Section IV. Paper ends in Section V with the conclusion

II. DOUBLE EDGE TRIGGERED FLIP-FLOP STRUCTURES

There are several ways to implement a DETFF; such ways can be categorized into two ideas. The first idea is to insert additional circuitry to generate internal pulse signals on each clock edge. The second idea is to duplicate the pathway to enable the flip-flop to sample data on every clock edge.

The DETFF doubles the rate of data processing or alternatively halves the clock rate thereby, either increasing the data throughput or reducing power consumption in the clock circuit respectively. Thus reduced power and high speed operation is possible.

A. Double Edge Triggered Flip-Flops:

The DET flip flop proposed in [1] is shown in figure 1. This flip-flop is basically a Master Slave flip-flop structure. This has two data paths. The upper data path consists of a Single Edge Triggered flip-flop implemented using transmission gates. This works on positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using transmission gates. Both the data paths have feedback loops connected such that, whenever the clock is stopped, the logic level at the output is retained. This flip flop has 20 transistors. In these 20 transistors, 10 transistors are clocked transistors.

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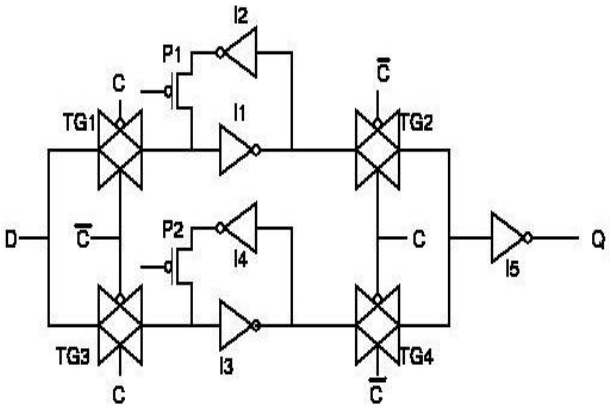

Fig.1: DETFF1 proposed in [1]

DET flip-flop proposed in [2] is shown in figure 2. This flip flop is similar to figure1 except that feedback has been changed. The upper data path is triggered on the rising edge and lower data path is triggered on falling edge. An inverter and a PMOS transistor are used to hold the logic level when the TG is closed. When the data value is high, the inverter switches the signal to low, which will make the PMOS transistor pull the data up to high. When data value is low, the inverter switches the signal to high, which will isolate the data from VDD and keep the value low. This flip-flop provides static functionality for high output since a PMOS transistor connected to VDD is used in the feedback network, but the static functionality for low output is not provided by this flip-flop. This will make the circuit to behave like a dynamic circuit.

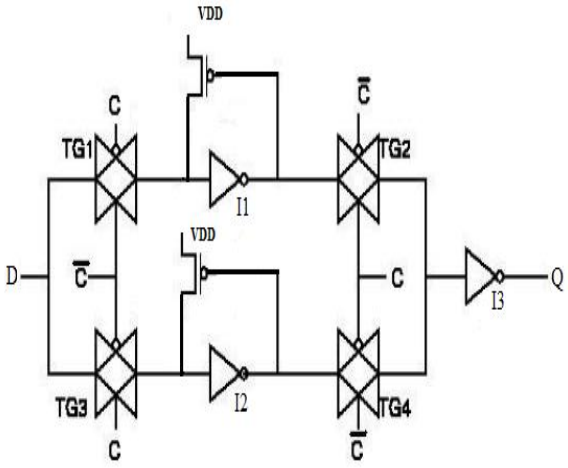

Fig.2: DETFF2 proposed in [2]

B. Proposed Double Edge Triggered Flip-Flop:

The proposed Double Edge Triggered Flip-Flop (DETFF) design is shown in Fig. 3. This flip-flop is basically a Master Slave flip flop structure and it consists of two data paths. The operation of the proposed flip-flop is similar to that of figure 1, but the number of clocked transistors is reduced from 10 to 6 by replacing the transmission gates by using n-type pass transistors. Basically, n-type pass transistors give weak high but in figure 3, the n-type pass transistors are followed by an inverter, which results in strong high.

Thus the proposed DETFF in figure 3 is free from threshold voltage loss problem of pass transistors. Then the feedback network of figure 1 is altered by replacing the p-type pass transistor by n-type pass transistor since, the area incurred by NMOS is less than that of PMOS transistor in order to compensate the mobility constraint of NMOS and PMOS transistors. Thus the proposed Double Edge Triggered Flip-Flop (DETFF) has become more efficient in terms of area, power and speed which claim for better performance than conventional designs.

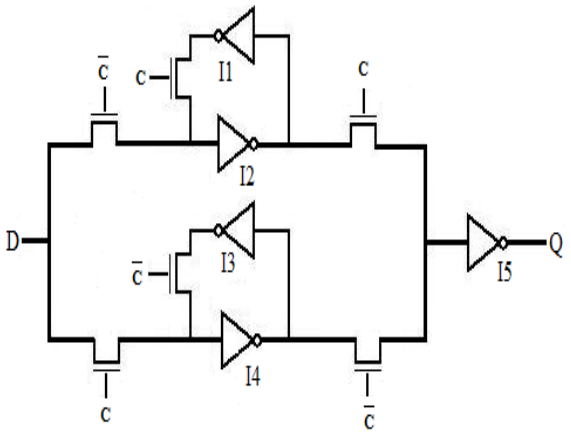

Fig 3: Proposed DETFF

III. TRANSIENT ANALYSIS

To evaluate the performance, different flip-flop structures discussed in this paper are designed using 130-nm CMOS technology. All simulations are carried out using HSPICE simulation tool at nominal condition with different range of frequencies from 1MHz to 2GHz. The simulated waveform of the proposed DET flip-flop is shown in Fig.4. This waveform shows that the proposed DETFF is storing the data in both rising edge and falling edge of the clock signal.

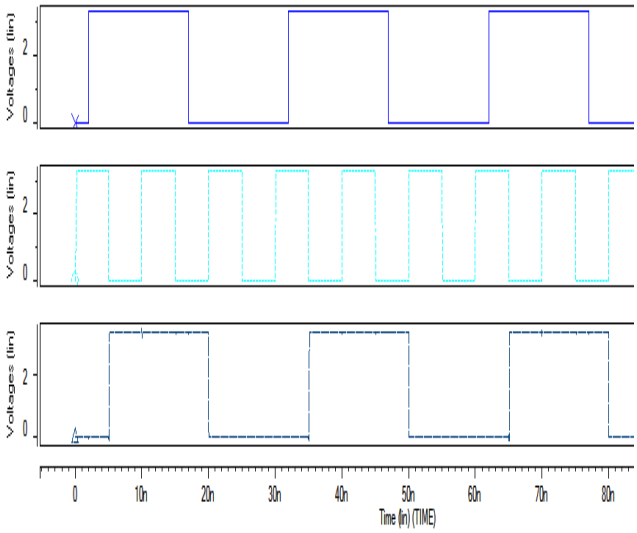

Fig 4: Output waveform for proposed DETFF

IV. PERFORMANCE COMPARISON

The performance of the proposed DETFF is evaluated by comparing the average power, delay and power delay product (PDP) for DETFF1, DETFF2 and proposed DETFF. In general, a PDP-based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency.

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The following tables from TABLE 1 to TABLE 6 furnished the performance parameters for different range of frequencies.

TABLE 1: Performance comparison at 1MHz

FLIP FLOP's	AVERAGE POWER(µW)	DELAY (ps)	PDP (aJ)
DETFF1	1.509	107.16	161.7
DETFF 2	17.45	110.91	1935.3
PROPOSED DETFF	0.115	94.98	10.92

TABLE 2: Performance comparison at 10MHz

FLIP FLOP's	AVERAGE POWER(µW)	DELAY (ps)	PDP (aJ)
DETFF1	3.25	34.98	113.6
DETFF 2	6.80	40.06	272.4
PROPOSED DETFF	0.74	34.98	25.88

TABLE 3: Performance comparison at 100MHz

FLIP FLOP's	AVERAGE POWER(µW)	DELAY (ps)	PDP (aJ)
DETFF1	9.22	36.22	333.9
DETFF 2	19.78	40.27	796.5
PROPOSED DETFF	6.56	34.63	227.1

TABLE 4: Performance comparison at 500MHz

FLIP FLOP's	AVERAGE POWER(µW)	DELAY (ps)	PDP (aJ)
DETFF1	45.69	37.06	1693.2
DETFF 2	51.03	41.05	2094.7
PROPOSED DETFF	41.56	35.58	1478.7

TABLE 5: Performance comparison at 1GHz

FLIP FLOP's	AVERAGE POWER(µW)	DELAY (ps)	PDP (aJ)
DETFF1	84.98	37.73	3206.2
DETFF 2	91.74	41.02	3763.1
PROPOSED DETFF	78.15	36.99	2890.7

TABLE 6: Performance comparison at 2GHz

FLIP FLOP's	AVERAGE POWER(µW)	DELAY (ps)	PDP (aJ)
DETFF1	169.4	39.61	6709.9
DETFF 2	183.2	41.67	7633.9
PROPOSED DETFF	162.4	38.72	6288.1

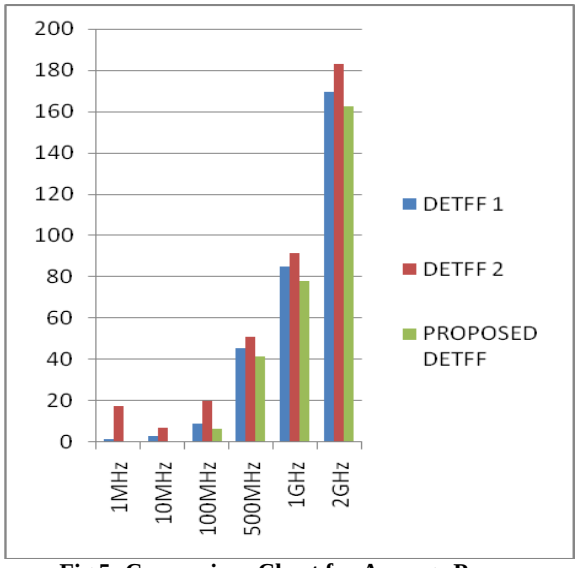

Fig 5: Comparison Chart for Average Power

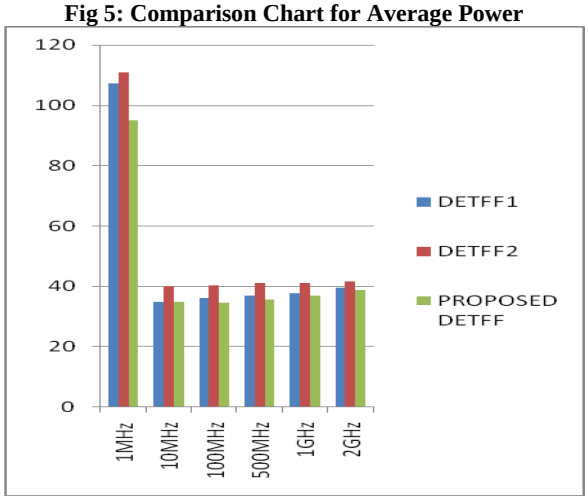

Fig 6: Comparison Chart for Delay

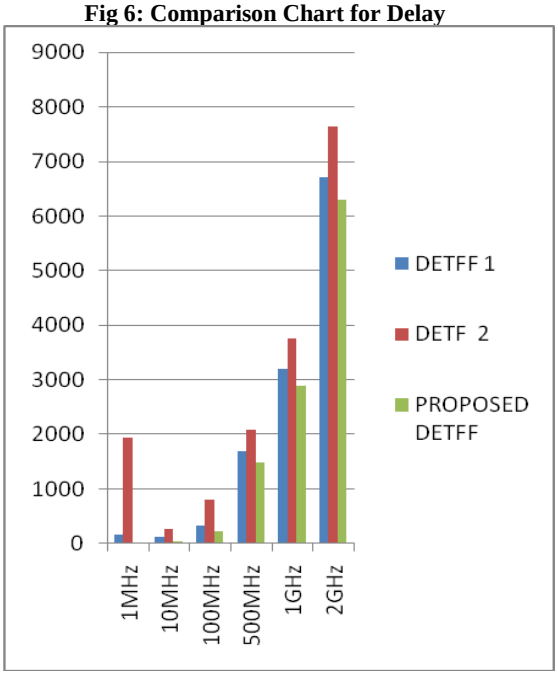

Fig 7: Comparison Chart for Power Delay Product (PDP)

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V. CONCLUSION

In this paper, we have proposed a high performance Double Edge Triggered D-Flip Flop design in 130nm CMOS technology, which is static in nature. We have made a performance comparison with other two previously published DET flip flops. The proposed DET flip-flop is having less number of clocked transistors than the other two existing designs. The DET flip-flops are simulated with different clock frequencies ranging from 1MHz to 2GHz. Simulation results show that the proposed DET flip-flop has improvement of 77.23% and 89.11% in terms of average power when compared with DETFF1 and DETFF2 respectively. The proposed design also has an improvement of 77.21% and 90.49% in terms of power delay product (PDP) as compared to DETFF1 and DETFF2 respectively. The proposed design has lesser average power and lowest PDP than existing designs. Therefore the proposed design is very well suited for low power and high performance applications.

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