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FPGA Based Cost Efficient Fir Filter Using Factored CSD Technique

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ABSTRACT*: *In this paper, an FPGA based area and power efficient FIR filter for wireless communication systems is presented. The implementation is based on Factored Canonic signed digit (FCSD) which eliminates the use of embedded multipliers. The proposed FIR filter has been implemented using Equiripple Symmetric structure on an FPGA. The developed FIR filter has been optimized in terms of MAC operation using symmetric structure. The symmetric structure requires less hardware for implementation as compared to transposed structure and also reduces hardware complexity. The performance of both symmetric and transposed structure is almost same but implementation cost varies significantly. A 20 tap FIR filter has been designed and simulated using 16 bit input and output precision with the help of Matlab. Factored Canonic signed digit (FCSD) approach is used to implement an FIR Filter taking optimal advantage of the look up table structure of FPGA. The behavioural simulation of proposed VHDL model has been performed using Modelsim simulator. The simulated model has been synthesized using Xilinx synthesis tool (XST) on Virtex 2 based xc2v3000-4ff1152 target FPGA device. The results show that symmetric FIR filter require 52.3 % less hardware as compare to transposed FIR structure. The developed symmetric FIR structure can operated at a maximum frequency of 45 MHz by consuming 6% slices, 2% flip flops and 5% Look up tables (LUTs) to provide cost effective solution for Digital Signal Processing Applications.

Index Terms*: *DSP, FCSD, FIR, FPGA, VHDL

I. INTRODUCTION

The aim of this work is to compare different approaches of number representation Implemented on a multiplier less FIR-filter structure on an FPGA. The two approaches to compare are three different implementations of the same filter. The first approach represents the tap values in binary number representation, the second approach in CSD (canonic signed digit) number representation. Decimator. Finite impulse response (FIR) digital filters are common DSP functions and are widely used in FPGA implementations. If very high sampling rates are required, full-parallel hardware must be used where every clock edge feeds a new input sample and produces a new output sample.

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During one of these steps, a transition from the analog domain to the digital domain is performed. The reason for a digital system is manifold, for one it makes it possible to transmit not just audio but data as well as shown in figure1. Furthermore this data can be encrypted.

The next step was to do analysis on filters and find the right filter type for this project based on predefined requirements. Since the available hardware resources limit the filter size, different filter structures and algorithms were analysed to reduce the required hardware resources.

Fig 1. RELEVENT COMPONENTS

For this MATLAB was used since it is very strong in creating and analysing filters. The next step was to create an environment on the FPGA in which the filter architecture could be implemented. A digital filter is programmable, in other words, its operation is determined by a program stored in the processor's memory. This means the Digital Filters can easily be changed without affecting the circuitry. They are easily designed, tested and implemented on a general-purpose computer or workstation. To overcome difficulties of cost and speed Several algorithms with the aim of reducing the number of adders needed in such a structure have been presented in literature.

Among the efficient algorithms are reducing the number of additions needed by taking advantage of common sub-expressions (CSE).

1. Exploiting the reduction of non-zero bits in different number representations.
2. Representing the multiplication as a graph-structure.
3. Implementing the design in a Distributed Arithmetic manner on a FPGA.

Since the analysis was restricted to MATLABs filter builder only the algorithms supported by it have been analysed. It was concluded that the best algorithm for this project is the Equiripple with a symmetric structure. A suitable filter architecture will have to support filters of an order up to 20 Taps,which is necessary to meet the hardware requirements and using VHDL. The proposed design is hardware co-simulated using System Generator 10.1, synthesized with Xilinx Product Version: ISE 10.1 – WebPACK software.

II. CSD AND FACTORED CSD ALGORITHM

In [1], we have proposed the binary common subexpression elimination (BCSE) method which provided improved adder reductions and thus low complexity FIR filters Numerous algorithms using Common Sub-Expressions (CSE) have been presented. The idea is as follows:The coefficient set S = *fc1; c2; c3g*, *c*1 = 1000-10000,*c*2= 0-10-1010010, *c*3 = 000010000- 1, can be represented in a Table 1. Such filters can be implemented on FPGAs using combinations of the general purpose logic fabric, on-board RAM and embedded arithmetic hardware. Full-parallel filters cannot share hardware over multiple clock cycles and so tend to occupy large amounts of resource. Hence, an efficient implementation of such filters is very important to minimize hardware requirement [2]. The computing canonical-signed-digit (CSD) is a number system for encoding a floating-point value in a two's complement representation. This encoding contains 33% fewer non-zeros than the two's complement form, leading to efficient implementations of add/subtract networks in hardwired Digital signal processing. The representation uses a sequence of one or more of the symbols, -1, 0, +1 (alternatively -, 0 or +) with each position possibly representing the addition or subtraction of a power of 2. For instance 23 is represented as +0-00-, which expands to $+2^5-2^3-2^0$ or 32-8-1=23.

A digital filter structure is said to be canonic if the number of delays in the block diagram representation is equal to the order of the transfer function, otherwise, it is a non-canonic structure. A CSD based digit reconfigurable FIR filter architecture was proposed, This architecture was independent of the number of taps because the number of taps and non-zero digits in each tap were arbitrarily assigned. The intention of the authors was to reduce the precision of coefficients and thus the filter complexity without affecting the filter performance. But the architecture in [2] demanded huge hardware resources and this makes the method infeasible for power constrained SDR receiver applications. In [3], a high speed programmable CSD based FIR filter was proposed. Encoding a binary number such that it contains the fewest number of non-zero bits is called canonic signed digit (CSD).Here, mapping a number to a ternary system {-1,0, 1} versus a binary system {0,1} is done.

The following are the properties of CSD numbers: No two consecutive bits in a CSD number are non-zero.

1. The CSD representation of a number contains the minimum possible number of non-zero bits, thus the name canonic
2. The CSD representation of a number is unique.

$$a'_{-1} = 0;$$
$$\gamma_{-1} = 0;$$
$$a'_{W} = a'_{W-1};$$
$$\text{for } (i = 0 \text{ to } W\text{-}1)$$
$$\{$$
$$\theta_i = a'_i \text{ XOR } a'_{i-1};$$
$$\gamma_i = \gamma_{i-1} \cdot \theta_i;$$
$$a_i = (1 - 2a'_{i-1}) \cdot \gamma_i;$$
$$\}$$

Fig 2 .Algorithm to obtain CSD representation

Among the N-bit CSD numbers in the range [-1,1), the average number of non-zero bits is N/3 + 1/9 + O(2-N).Hence, on average, CSD numbers contains about 33% fewer non-zero bits than two's complement numbers. The conversion of W-bit number in SW.(W-1) notation to CSD format is given as: A = a'_{W-1}. a'_{W-2}… a'_1 a'_0 = 2's complement number and Its CSD representation is a_{W-1}. a_{W-2}… a_1 a_0.

Table 1. Table representation of coefficient set S

C1	1				-1				
C2		-1		-1		1		1	
C3					1				-1

Thus, it is clear that the choice of the Factored -CSD algorithm to be applied is always a trade-off between computational complexity and fast convergence. So an optimized technique can be employed to achieve so. A filter for wireless applications has been designed and implemented on target FPGA device using Factored - CSD algorithm. The embedded multipliers and LUTs of target device have been efficiently utilized to enhance the Speed and to provide the Area efficiency. The results have shown enhanced performance in terms of Speed, Resource and Power consumption. The results are better than existing one, because we are reducing power consumption and improving area utilization**.**

So, for a real time applications such as filtering, combinational multipliers are used because of their high speed. Low pass FIR Filter is designed by choosing CSD algorithms and MATLAB FDA Tool is used Coefficients calculation. The CSD numbers has the minimum number of non-zero digits and no consecutive nonzero digits. When the multipliers in the digital filters are used with shifters, adders and subtractors, it reduces the number of adders and subtractors CSD expression. In order to apply FIR filters, flexible filter architecture has been designed and implemented as an RTL hardware model with VHDL. Digital filtering can be broken down to a sum of additions and multiplications. Since embedded multipliers are limited in FPGAs the designed architecture is based on a resizable parallel and sequential part which allows it to make the best use of the multipliers taken the desired clock frequency into account. The architecture supports symmetric FIR flters of an odd order number. An VHDL generation software for optimized FIR filters, the algorithm uses general coefficient representation for the optimal sharing of partial products in Multiple Constants Multiplications (MCM). The developed tool was compared to Matlab FDA toolbox [6]. Synthesis results show that our tool is able to produce significantly better hardware than FDA toolbox [7]. The proposed architectures have been implemented and tested on Virtex FPGA and synthesized on CMOS technology, two new approaches namely, CSM and PSM, for implementing reconfigurable higher order filters with low complexity. The CSM architecture results in high speed filters and PSM architecture results in low area and thus low power filter implementations [8]. The compact version of the title with the word "Efficiency" representing "Low Power" and "Small", and "Complex" representing "Complex-Valued Coefficients and Signals", resulting in: "Symmetry and Efficiency in Complex FIR Filters". By using this symmetry the number of multiplications can be halved by folding the delay pipe line. The symmetric structure is very interesting because it reduces the amount of required multipliers.

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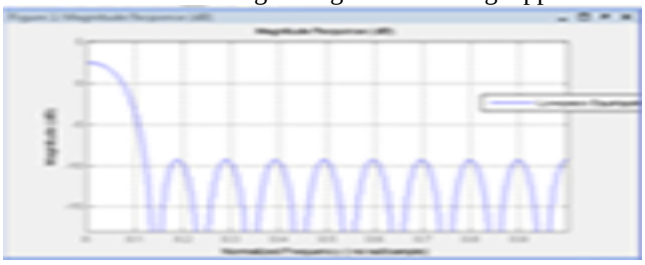
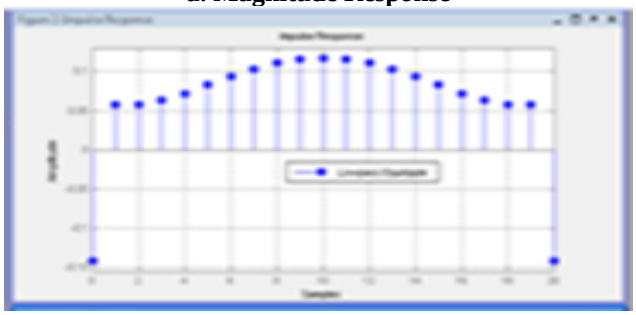
III. MATLAB BASED FILTER DESIGN

One of the key objectives is to learn how to implement actual design problem in hardware. The following steps will depict the procedure exactly as done by the author by taking a relevant example: 1. Define the filter specifications such as order, window function, cut-off frequency and sampling frequency. 2. Calculate the filter coefficient using MATLAB FDATool.3. Apply FCSD Algorithm on filter Coefficients.4. Configured the target FPGA , Virtex 2 based xc2v3000-4ff1152 kit for real time debugging. 5. Checked the FCSD Filter coefficients on target FPGA Chip. 6. Configured the target FPGA Virtex 2 based xc2v3000-4ff1152 kit for real.

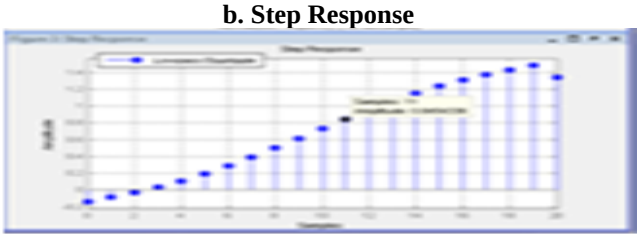
Here Figure3 shows, the design and simulation & proposed structure has been done using Matlab and implementation cost has been calculated in terms & multiplies and adders. The Symmetric structure has shown reduced consumed & multipliers. The Symmetric direct for FIR filter has consumed 21 multiplies as compared to 11 in case & transferred direct form FIR filter for providing cost and area efficiency. These results further implemented on Virtex 2 based xc2v3000-4ff1152 kit to realize the hardware to developed symmetric FIR structure can operated at a maximum frequency of 45 MHz by consuming 6% slices, 2% flip flops and 5% Look up tables (LUTs) to provide cost effective solution for Digital Signal Processing Applications.



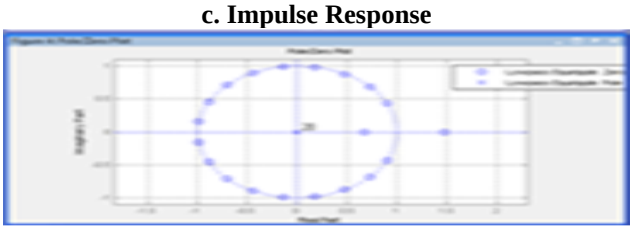
a. Magnitude Response



b. Step Response



c. Impulse Response



d. Pole Zero Plot

Fig 3. Various output response of Direct form Symmetric FIR

IV. HARDWARE IMPLEMENTATION RESULTS

The implemented architecture of are shown through tests. These tests are based on simulations performed in Modelsim and MATLAB. Furthermore, measurements are verified. It first deals with the state machine receiving the data samples from the ADC. Afterwards the filter architecture will be tested. This verifies that the state machine used to receive the samples from the ADC has been implemented correctly by simulating its behaviour in Modelsim. In order to verify correct behaviour, two parts must be tested. The first part is to verify that the state machine goes through the correct states. The second part is to see if the correct output is generated.

Figure 3 shows a Modelsim screenshot. The system starts with a reset and the init state is entered. Afterwards the DRDY signal goes high, thereby indicating the beginning of a data sample. The very first sample should be ignored. For this reason, the machine enters the idle state as a response to DRDY going low.

The machine remains in this state until DRDY goes high again. As can be seen in the Modelsim snapshot, there exists a DOUT buffer. This signal is necessary because the counter defining where to store the incoming bit is delayed one cycle compared to the incoming data bit. To synchronise them, the incoming data bit is delayed together with DOUT. Last but not least the same tests have been performed on the FPGA. The complete filter hardware was described in VHDL and synthesized using Xilinx ISE 10. The architecture has a maximum frequency is 45MHz. In order to use it for high speed optimisation of symmetric structure, the proposed architecture is implemented in Virtex 2 FPGA xc2v3000-4ff1152. For this, a board with the mentioned FPGA and Matlab is used. By analyzing the contents of the SDRAM with MATLAB it could be verified that the contents hold the same values as the Modelsim simulations. The analysis will determine which filter method suits the project best in terms of usage of hardware resources which is directly related to the filter order. Therefore, the parameter of concern is the filter order only. This section contains screendumps showing the utilization of the FPGA in Xilinx for different designs.

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 22.203ns (Maximum Frequency: 45.040MHz)
   Minimum input arrival time before clock: 5.373ns
   Maximum output required time after clock: 5.446ns
   Maximum combinational path delay: No path found
```

Fig.2 shows the utilization of a design with Direct Symmetric FIR filter implementation. Due to this reduction in required resources the proposed design can be implemented on Vertex 2 FPGA device to provide cost effective solution for DSP.Consequently all the plots shown in this figure 2 are based on data sampled with the FPGA, unless otherwise stated. In this proposed work a 20-tap low pass filter has been designed.

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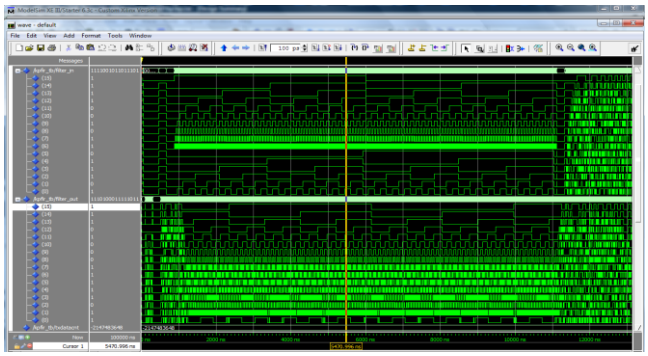

FIGURE 2. MODELSIM BASED RESPONSE OF FIR FILTER

The first step in design flow is to develop an optimized VHDL code using Symmetric Algorithm and implement it using simulation in Modelsim to develop proposed model of design. Figure 2 shows the developed model of proposed design using various Simulink and Matlab.

.

Table 3. Performance Comparison of csm and fcsd

S.No	Information	CSM	FCSD
1	4 Input LUTs	8976	1540
2	Slices	5023	967
3	Slice Flip Flop	4198	717

Table 2. Device utilization summary

INFORMATION	COUNT
No. of Slices	967 of 14336
No. of Flip Flops	717
No. of 4 Input LUT's	1540 of 28672
No. of Bounded IOBs	35 of 720
No of GCLK's	1 of 16

V. CONCLUSION

The cost effective design of 20 Tap FIR filter has been presented using symmetric architecture replace multiplier operations with shift and add operations on prime factors of the coefficients. The simulated VHDL model has been synthesized using Xilinx synthesis tool on Virtex 2 based xc2v3000-4ff1152 target FPGA device. The results show that symmetric FIR filter require 52.3 % less hardware as compare to transposed FIR structure. The developed symmetric FIR structure can operated at a maximum speed of 22ns by consuming 967 slices, 717 flip flops and 1540 Look up tables (LUTs) to provide efficient Signal Processing. This concludes that low-pass FIR filters are the right choice due to their stability and linearity. Moreover, it is concluded that the filter structure should be of a symmetric type since this reduces the amount of multiplications which is a critical resource in an FPGA

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