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Low Power MAC Unit for DSP Processor

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Abstract: Power dissipation is one of the most important design objectives in integrated circuit, after speed. Digital signal processing (DSP) circuits whose main building block is a Multiplier-Accumulator (MAC) unit. High speed and low power MAC unit is desirable for any DSP processor. This is because speed and throughput rate are always the concerns of DSP system. This paper explores the design of low power MAC unit with block enable technique to reduce power dissipation. The MAC unit is implemented using 130-nm CMOS process technology. The whole MAC chip is operated at 200 MHz with1.5V supply voltage. The result analysis shows that the power consumption is reduced by using block enable technique.

Index Terms—Adders, block enable, CAD tools, low power, MAC, multipliers.

I. INTRODUCTION

Dueto rapid growth of portable electronic systems like laptop, calculator, mobile etc.,and the low power devices have become very important in today world. Low power and high-throughput circuitry design are playing the challenging role for VLSI designer. For real-time signal processing, a high speed and high throughput MAC unit is always a key to achieve a high performance digital signal processing system [1]. The main motivation of this work is to investigate various pipelined multiplier/accumulator architectures and circuit design techniques which are suitable for implementing high throughput signal processing algorithms and at the same time achieve low power consumption.A regular MAC unit consists of multipliers and accumulators that contain the sum of the previous consecutive products.

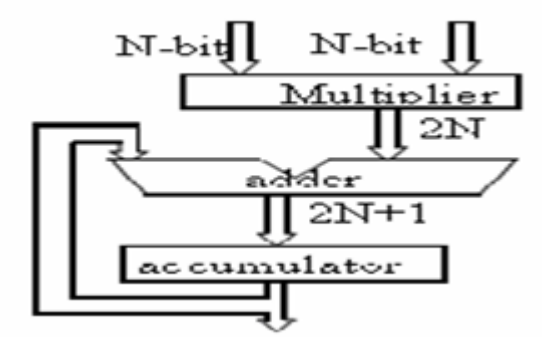

Figure 1. MAC unit basic structure [1]

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The function of the MAC unit is given by the following equation.

$$F = \sum A_i X B_i$$

The main work of this paper is to design a high speed and low power MAC unit with block enable technique.

The paper is organized as follows. Section II presents the basic operation and design of MAC unit. MAC unit with block enable technique and pipeline block enable logic are described at Section III and IV respectively. Section V shows the simulation results and Section VI concludes this work.

II. MULTIPLIER AND ACCUMULATOR UNIT

MAC unit consists of adder, multiplier, and an accumulator. For high speed MAC unit,faster adder and multiplier circuits are required. Figure 2 shows the MAC unit architecture.

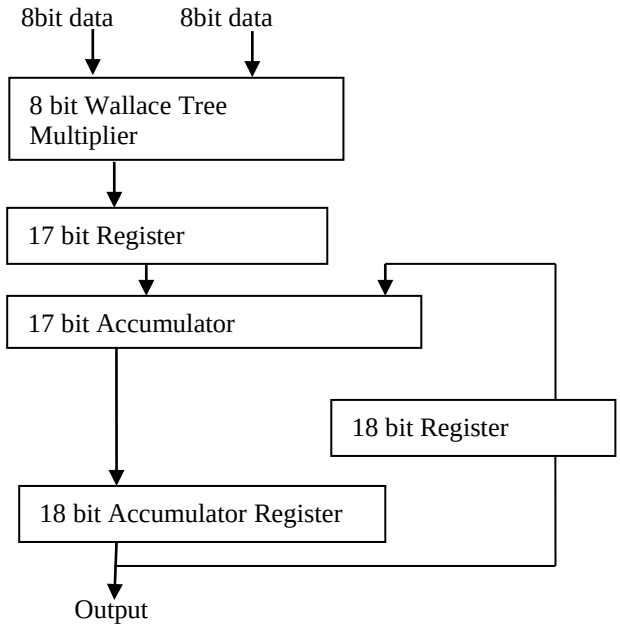

Figure 2.MAC Architecture

The inputs for the MAC are fetched from memory location and fed to multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location. This entire process is to be achieved in a single clock cycle [2]. The design of MAC unit architecture from Fig. 2 shows that the design consists of one 17 bit register, one 8-bit Wallace tree multiplier, 17-bit accumulator using carry look ahead adder (CLA) and two 18-bit accumulator register are used.

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In this project, Wallace tree multiplier and carry look adder are used to high performance MAC unit design.Wallace tree multiplier is used to multiply the values of A and B. CLA are used in accumulator and carry save adder (CSA) used in the final stage of the given multiplier for reducing power consumption of the MAC unit. The product of A_i x B_i is always fed back into the 17-bit CLA in accumulator and added again with the next product A_i X B_i. This MAC unit is capable of multiplying and adding with the previous product consecutively up to as many as eight times. Output = $\sum A_i$ X B_i..

This project design with 8 X 8 multiplier unit is carried out perform accumulation on 17-bitnumber. The MAC unit has 18-bit output and its operation is to add repeatedly the multiplication result.

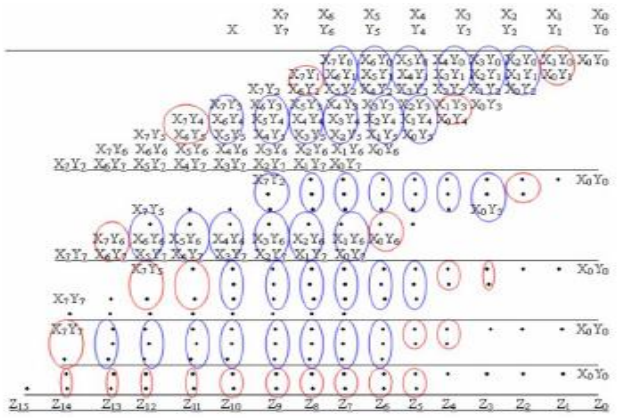

Figure 3. Algorithm for 8 bits X 8 bits Wallace tree multiplier [8]

Fig 3 shows the Wallace tree multiplication algorithm for 8X8 bits. There are five stages to go through to complete multiplication process [1]. Each stage uses 1bit full adder denoted by blue circleand 1 bit half adder denoted by red circle. Firstly, the partial products are using the half adders and full adders that are combined to build a CSA until there were just two rows of partial products left. Next, we add remaining two rows by using a fast carry propagate adder. In this work CSA using CLA is used to get final sum. Secondly, the schematic of the conventional 8 X 8 bits high speed Wallace tree multiplier is designed by referring to the algorithm.

III. CARRY LOOK AHEAD ADDER

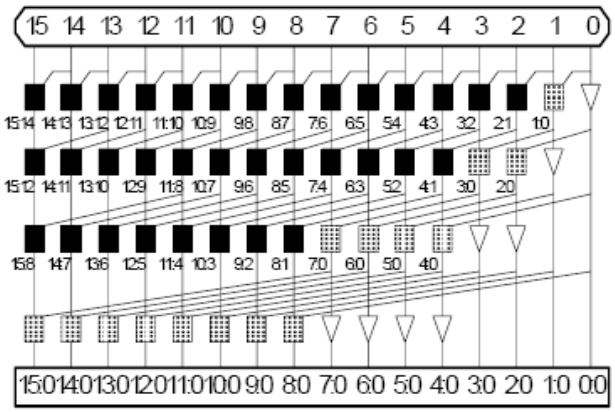

Figure 4.Kogge-Stone Adder

CLA is one of the best adder in terms of power-delay product. Kogge-Stoneadder possesses a regular layout and is preferred for highperformance applications. So this adder topology is used for 17-bit accumulator.

IV. BLOCK ENABLE TECHNIQUE

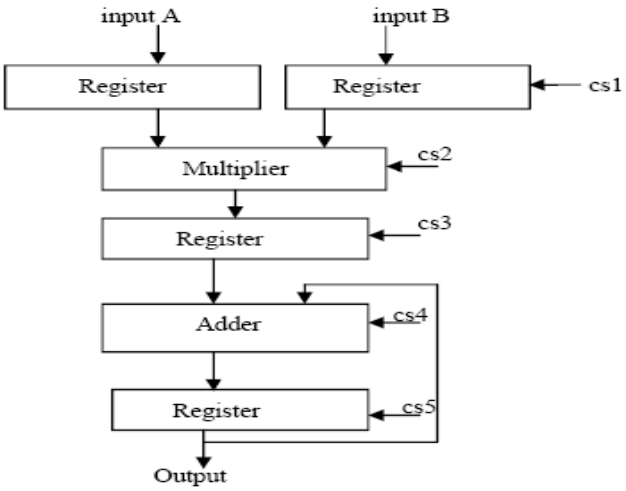

Figure 4. Block Diagram of a Pipeline MAC with block enable technique cs- control signal

Fig. 4 shows the Pipeline MAC unit with block enabling technique. The input registers pass the data to the multiplier. Within multiplier stage, there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. First we find out delay for each stage in block enable technique. Every block gets enabled only after the expected delay. Every block gets enabled only after the expected delay. The successive blocks are disabled until the inputs are available. This technique saves the power. In this project, we have designed a 1-bit MAC unit with pipeline structure and calculated power consumption.

V. PIPELINED BLOCK ENABLED LOGIC

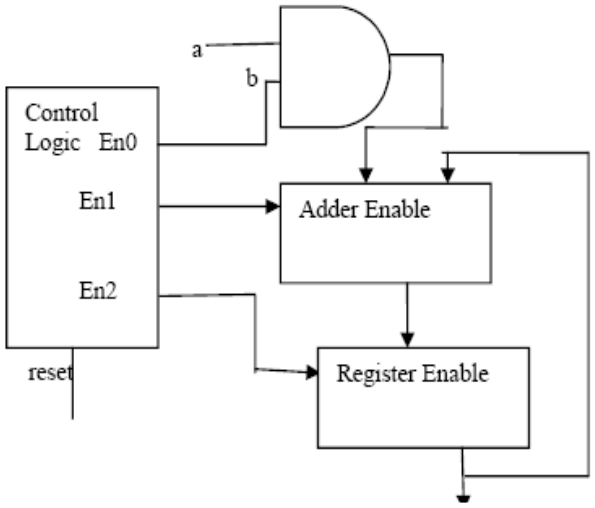

Figure 5. MAC with control logic

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Fig. 5 shows a three stage pipelined MAC with block enabled logic. In this logic, depending upon the delay of individual blocks, the control logic enables the clock, power and logic pins of the block, thus saving the power.

VI. ACCUMULATOR REGISTER

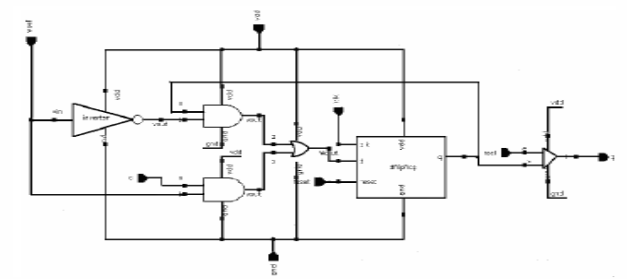

Figure 7. One bit Register Cell

Fig. 7 shows the 1 bit register. The register cell consists of a D-flip flop and two gates with clock input. The cell has three inputs and one output signal. The input signals are write select, read select and D input. Q is the output signal.

The D-flip flop will store the value of the input signal whenever write select is equal to 1, consequently, whenever the read select signal is equal to 1, this D-flip flop will pass its stored value to the output through a tristate buffer.

The basic building blocks of any MAC units are Multiplier, Adder and Register. Multiplier and adder blocks require full adders, and registers require flip-flops or latches.

VII. SIMULATION RESULTS

The MAC unit with enable technique in this paper has been simulated using Verilog-HDL and synthesized using Cadence RTL compiler under TSMC 130-nm CMOS process technology [9]. Table I shows the simulation results.

TABLE I: POWER, DELAY, SPEEDAND POWER –DELAY PRODUCT OF VARIOUS BLOCKS

Blocks	Power (µW)	Delay (ns)	Speed	Power-delay Product (10^{-15}J)
17-bit Accumulator	46.424	0.2281	4.384 GHz	10.589
18-bit Accumulator Register	62.8642	0.2834	3.528 GHz	17.815
8 X 8 bit Wallace Tree Multiplier	51.8628	0.4828	2.07 GHz	25.04
MAC Unit	163.86	1.086	92MHz	177.95

The main purpose of this work is to find the power, delay and speed of the MAC unit. The MAC units consist of flip flop to store 1-bit data, 1-bit adder and AND gate to control activity with enable technique. These basic building blocks are taken independently and analyzed for delay and power. The multiplexer [MUX] based full adder circuit is used for MAC architecture. This MUX based full-adder circuit shows better result in terms of speed and power consumption compared to other full-adder circuits.

VIII. CONCLUSION

In this paper, the design of 8X8 MAC unit has been implemented using block enable technique to reduce the power consumption. This MAC unit has 18 bit output and its operation is to add repeatedly the multiplication results. All the basic blocks of MAC unit are identified and analyzed its performance. Power and delay is calculated for the blocks. First, we design 1 bit MAC unit and calculate power consumption based on block enable technique. Using this block, the N bit MAC unit design. We calculated the power consumption of this N bit MAC unit. Table 1 shows the result of different blocks of MAC architecture. The improvement of power-delay product of the MAC unit can be used in high speed DSP application.

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