International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-1, Issue-6, January 2013

Arithmetic and Logic Unit Designing Using Reversible Logic Gate

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ABSTRACT: ***Owing to its unique technique of One-to-One Mapping between the inputs and the corresponding outputs, the ReversibleLogicGates are now finding profound as well as promising applications in emerging growing paradigms such as Quantum Computing, Quantum Dot Cellular Automata, Optical Computing, Digital Signal Processing, Low Power CMOS Design, Nanotechnology etc. The ReversibleLogic has received great attention in the past recent years due to its ability in reducing the power dissipation, the major concern in digital designing. To generate a useful gate function the ReversibleGates require constant inputs, called Ancillary Inputs, and some additional unused outputs, called Garbage Outputs, in order to maintain the reversibility of the digital circuits. The paper presents a novel design of different Arithmetic and Logic Units such as Half Adder, Half Subtracter and 1-Bit Comparator, using the existing ReversibleGates and the proposed new ReversibleCNOT, BJN, and PeresGates.***

Keywords- CNOT Gate, Peres Gate, BJN Gate.

I. INTRODUCTION

Normal Combinational Logic Circuits dissipate heat for every bit of informationlost during their operation. Due to this, the recovery of a piece of information once lost is completely impossible. However, if the same circuit is constructed using the ReversibleLogicGates, not only is the recovery possible but also the dissipation of heat reduced. In the 1960s, R. Landauer demonstrated that even with high technology systems when designed using Irreversible hardware result in high energy dissipation and efficiency loss[a]. He showed that the loss per bit of information exchange dissipates KT.ln2 Joules of energy where K is Boltzmann Constant and T the Absolute Temperature at which the operation is performed[a]. Later in 1973, Bennett showed that this amount of energy loss can be overcome if the circuit is designed using the ReversibleLogictechnique[b].

With the number of chip components doubling every 18 months[a], as per Moore's Law, the Irreversible Technologies would dissipate a lot of heat and reduce circuit life. It is here the ReversibleLogic comes into action in not only recovering the lost information but also dissipating less heat[b].

Revised Manuscript Received on 30 January 2013.
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A ReversibleLogicGate is an n-input, n-output device withOne-to-One Mapping, which helps determining the outputs from the inputs and vice versa. Wherever necessary, extra outputs can be added to make the output count equal to that of the input. The main challenges are reducing Number of Gates, Memory Usage, Delay and Quantum Cost.

1. Terms Related To Reversible Logic Gates

The terminology pertaining to the Reversible Logic Gates is contained in the terms explained below:

a. Reversible Logic

It is an n-Input and n-Output logic function, whichhas One-to-One Mapping between the inputs and the outputs[c].Because of this One-to-One MappingTechnique, the output vector can be uniquely determined from the input vector.

b. Quantum Cost

The Quantum Cost refers to the cost of the circuit in terms of the cost of the primitive gates. It is calculated knowing the number of primitive Reversible Logic Gates required for realizing the Arithmetic and Logic Circuit[d] units.

c. Delay

The Delay of a Reversible Logic Gate is the maximum number of gates in a path from any input line to its corresponding output line. The definition of delay is based on the following two assumptions[b]:

- ❖ Each gate performs computation in a unit time.
- ❖ All the inputs fed to the circuit are available before the computation begins.

d. Hardware Complexity

Hardware Complexity refers to the total number of logic operations in a circuit. It corresponds to the total number of AND, OR and Ex-OR operations performed in a circuit.

e. Ancillary Inputs

The Ancillary Inputs are defined as the inputs that are to be fed into the Reversible Logic Gates and maintained constant at either '0' or '1'. The inputs are to be maintained at a constant value of '0' or '1' in order to synthesize the given logical function[e].

f. Garbage Outputs

The technique of One-to-One Mappingcomplies that there must be same number of outputs for the given inputs. The Garbage Outputs are the unutilized outputs in the Reversible Logic Circuits that maintain the reversibility but do not perform any useful operations[f].

II. BASIC REVERSIBLE LOGIC GATES

Some of the basic ReversibleLogicGates with their block diagrams are given as under:

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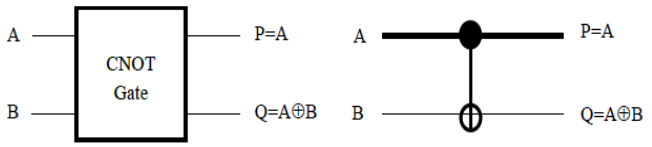
a. Feynman/CNOT Gate:

It is a 2x2 gate also called as Controlled NOT Gate.
It has a Quantum Cost equal to one and described by:

Input Vector = (A, B)

Output Vector = (P=A, Q=A⊕B)

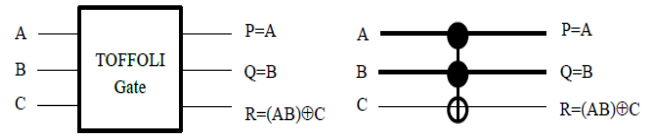


a) Block Diagram b) Quantum Implementation

Figure 1: Feynman/CNOT Gate

b. Toffoli Gate:

It is a 3x3 ReversibleGate[h)] having a Quantum Cost of five and described by:
Input Vector = (A, B, C)
Output Vector = (P=A, Q=B, R=(AB) ⊕C)

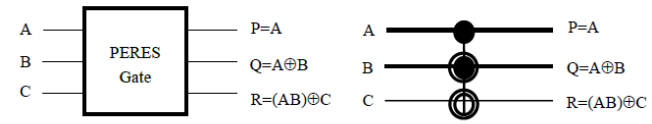


a) Block Diagram b) Quantum Implementation

Figure 2: Toffoli Gate

c. Peres Gate:

Peres Gate is a 3x3Reversible Gate, also called the New Toffoli Gate,constructed from CNOT and Toffoli Gate.It has a Quantum Cost of four and described by:
Input Vector = (A, B, C)
Output Vector = (P=A, Q=A⊕B, R=(AB) ⊕C)

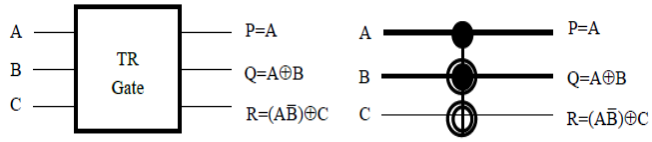


b) Block Diagram c) Quantum Implementation

Figure 3: Peres/New Toffoli Gate

d. TR Gate:

The Thapliyal-Ranganathan Gate is a 3x3 ReversibleGate[g)] having Quantum Cost of four.
The TR Gate is described by:
Input Vector = (A, B, C)
Output Vector = (P=A, Q=A⊕B, R=(AB̄) ⊕C)



a) Block Diagram b) Quantum Implementation

Figure 4: Thapliyal-Ranganathan Gate

e. BVF Gate:

The BVF Gate is a 4x4 ReversibleGate whose Quantum Cost is equal to two and described by:
Input Vector= (A,B, C, D)
Output Vector = (P=A, Q=A⊕B, R=C, S=C⊕D)

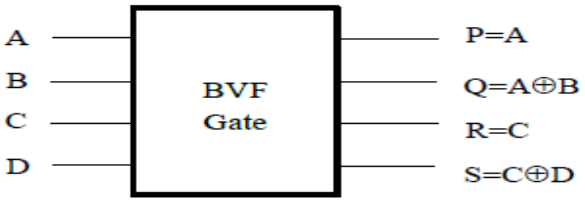


Figure 5: BVF Gate

f. BJN Gate:

Also known as the Modified Toffoli Gate,BJN is a 3x3 ReversibleGate, designed from two Controlled-V Gates and two CNOT Gates has a Quantum Cost five and a propagation delay of 5Δ, Δ being a unit delay.The MTG is describedby:
Input Vector= (A, B, C)
Output Vector = (P=A, Q=B, R=(A+B) ⊕C)

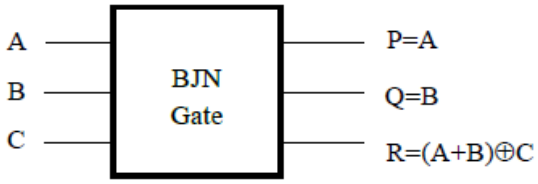


Figure 6: Modified Toffoli/BJN Gate

III. THE BJN GATE

The BJN Gate's truth table is shown in the table below:

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

Table 1: BJN Gate Truth Table

The BJN Gate can also be used as a Universal Gate. This is summarized in the table given below:

A	B	C	P	Q	R	Gate Function
A	B	0	A	A	A+B	OR
Ā	B̄	1	Ā	Ā	AB	AND
A	0	1	A	A	Ā	NOT
A	B	1	A	A	(A+B)'	NOR
Ā	B̄	0	Ā	Ā	(AB)'	NAND
0	A	B	0	0	A□B	XOR

Table 2: BJN Gate as a Universal Gate

The main points that must be kept in mind while designing the Arithmetic and Logic Units are as follows:

❖ The Quantum Cost should be kept as low as possible and must be less than the previously designedconventional Arithmetic and Logic Units.

❖ The number of Reversible Logic Gates should be used in less number to reduce complexity.

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IV. DESIGNING USING REVERSIBLE LOGIC

Some of the most common circuits using conventional Logic and their corresponding proposed ReversibleLogic are described here as under:

A) HALF ADDER

I.Conventional Logic

Half Adder's truth table and its corresponding conventional circuit are given as:

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 3: Half Adder Truth Table

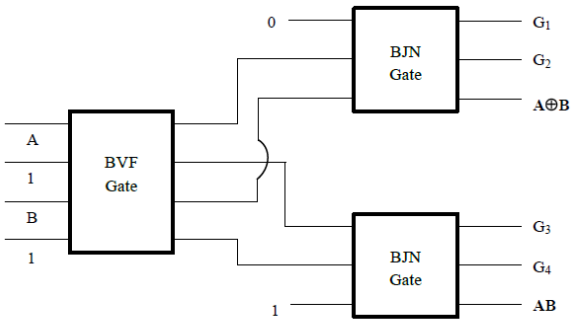

Figure 7: Half Adder Using BVF and BJN Gates

II.Proposed Reversible Logic

The Half Adder is implemented using the Peres and BJN Gate,wherein the number of Garbage Outputs being two and represented by G_1 and G_2 respectively, and a constant input Logic '0'.

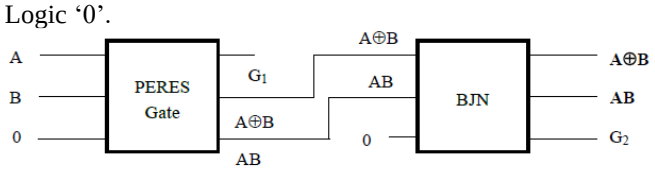

Figure 8: Half Adder using Peres and BJN Gate

B) HALF SUBTRACTER

I.Conventional Logic

Half Subtracter's truth table and its corresponding conventional circuit are given as:

INPUTS		OUTPUTS	
A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 4: Half Subtracter Truth Table

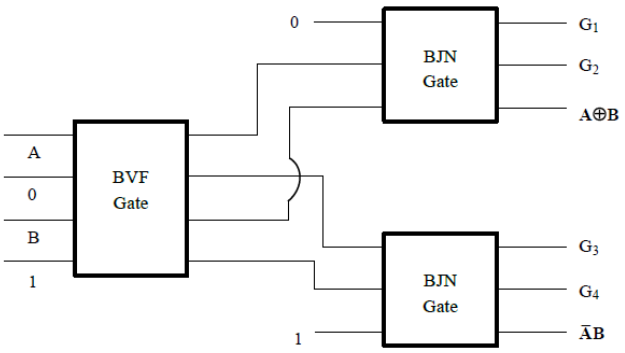

Figure 9: Half Subtracter Using BVF and BJN Gates

II.Proposed Logic

The circuitry for the proposed logic is shown in the figure given below. The circuit comprises of two CNOT Gates, one PERES Gate and one BJN Gate, thus making the Quantum Cost equal to eleven.

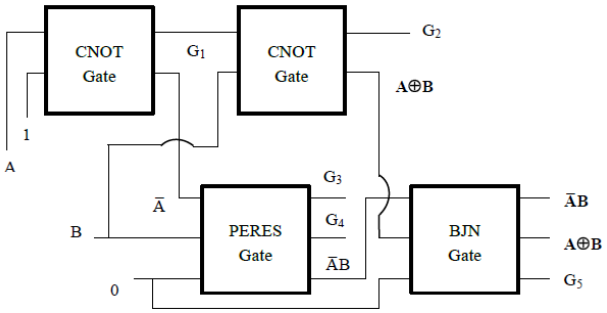

Figure 10: Half Subtracter Using CNOT, PERES and BJN Gates

C) 1-BIT COMPARATOR

I.Conventional Logic

Table 5 will clearly show that if any two of the three conditions are not satisfied, then the third one is going to be true, implying that one of the outputs can be generated from the remaining two and the logic depth of circuit reduced since computation is carried out with only one.

INPUTS		OUTPUTS		
A	B	$F_{A>B}$	$F_{A=B}$	$F_{A<B}$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Table 5: 1-Bit Comparator Truth Table

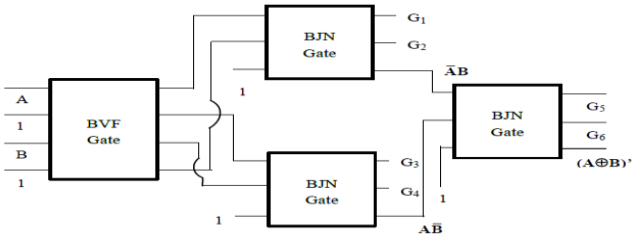

Figure 11: 1-Bit Comparator Using BVF and BJN Gates

II.Proposed Reversible Logic

In the proposed logic we have considered $F_{A>B}$ and $F_{A=B}$, and the third condition $F_{A<B}$ is generated from the first two conditions. Hence, the design expression leads to following three equations:

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$F_{A>B} = A\bar{B}$

$F_{A=B} = (A \oplus B)'$

$F_{A<B} = (A \oplus B)'. (A\bar{B})'$

The design requires one NOT Gate, one AND Gate and one Exclusive-NOR (XNOR) Gates.

The following table gives the truth table of AND, NOT and XNOR Gates.

INPUTS		OUTPUTS		
A	B	AND	NOT	XNOR
0	0	0	A=1 B=1	1
0	1	0	A=1 B=0	0
1	0	0	A=0B=1	0
1	1	1	A=0 B=0	1

Table 6: Truth Table of AND, NOT and XNOR Gates

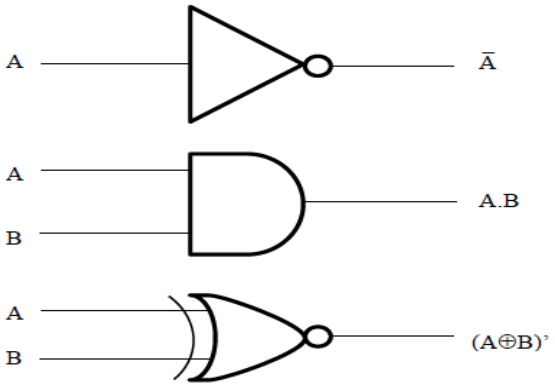

Figure 12: Representation of NOT, AND and EX-NOR Gate

Now BJN Gate is used in the last stage of the comparator to generate all the outputs of the required circuit. Using this gate in combination with the existing ReversibleGates, the number of garbage outputs, the number of gate counts and quantum cost is greatly reduced.

The representation of the proposed LogicGate is shown in the figure given below:

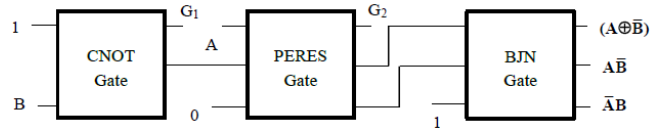

Figure 13: 1-Bit Comparator using CNOT, Peres and BJN Gate

V. CONCLUSION

The use of Reversible Logic Gates in designing the Arithmetic and Logic Circuits clearly shows areduction inQuantum Cost and the retrieval of lost information. The paper throws light on One-to-One Mapping, employed to get the desired results more efficiently than the conventional design. Using the proposed logic, the economic value &cost cutting, and use of a fewer number of Reversible Logic Gates is credible.

SERIAL NUMBER	ARITHMETIC AND LOGIC UNIT	QUANTUM COST	
		CONVENTIONAL LOGIC	PROPOSED LOGIC
1	Half Adder	12	9
2	Half Subtracter	10	11
3	1-Bit Comparator	17	12

Table 7: Comparison of Conventional & Proposed Logic

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