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A Critical Review on Photovoltaic Base Maximum Power Generation System

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Abstract: ***This paper focuses on the review of solar systems, converters and control techniques of MPPT with power generation. Photovoltaic cells provide an additional method of acquiring energy, converting sunlight directly into electricity through the use of semiconductors. Effective photovoltaic implementation is reviewed, focusing on semiconductor properties and overall photovoltaic system configuration. Solid-state switch-mode converters have reached a matured level for improving power quality reduced total harmonic distortion and precisely regulated dc output by Buck, Boost, Buck -Boost & Cuck regulators and also about the multilevel inverter topology. This paper deals with a comprehensive review of power converters and inverters unit. The photovoltaic generators have a nonlinear V-I characteristics and maximum power points which vary with the illumination level and temperature. Using maximum power point tracker (MPPT) with the intermediate converter can increase the system efficiency by matching the PV systems to the load. This paper presents a maximum power point tracker based on different control schemes for a single-phase or three-phase and multilevel inverter connected to the utility grid.***

Index Terms—Photovoltaic power systems; dc-dc converters MPPT controller, Multilevel inverters.

I. INTRODUCTION

The Conventional sources of energy are rapidly depleting. Moreover the cost of energy is rising and therefore photovoltaic system is a promising alternative. They are abundant, pollution free, distributed throughout the earth. However, the majority of the world's electrical energy came from conventional sources such as -fossil fuels, coal, natural gases and oil etc. These fuels are often term as non-renewable energy sources. Though, the available amount of these fossil fuels are extremely large, but due to decrease in level of fossil fuel and oil level day by day may be in few years it will end. Hence renewable energy based source demand increases as it is environmental friendly and pollution free and it will also reduces the greenhouse effect, but the hindrance factor is it's Therefore our aim is to increase the efficiency and quality power output of the system. It is also required that constant Voltage is supplied to the load irrespective of the variation in solar irradiance level and panel temperature. PV arrays consist of parallel and series combination of PV cells that are used to generate electrical power depending upon the atmospheric conditions (e.g. solar irradiation level, temperature and wind speed). So it is necessary to couple the PV array with dc regulators to obtain constant D.C output. Moreover our system is designed in such a way that with variation in load, the change in input voltage and power fed into the converter follows the open circuit characteristics of the PV array. Our system can be used to supply constant step D.C voltage to loads [1]. An exhaustive literature review has been carried out and presented as readymade reference for researchers in the field of photovoltaic power conditioning system. [2].

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II. POWER ELECTRONIC INTERFACE FOR GRID-CONNECTED PV SYSTEM USING CONVERTERS WITH MPPT

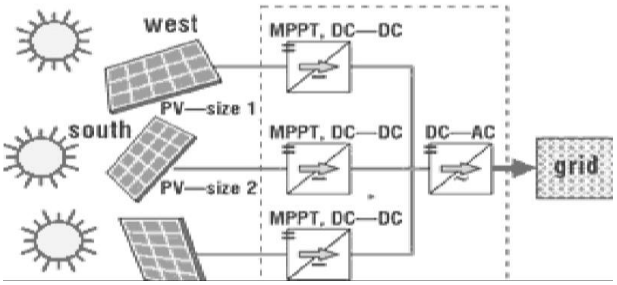

Fig. 1.0 Power Electronic Interfacing with PV system [1]

SOLAR ENERGY

It is a non-conventional type of energy. Solar energy has been harnessed by humans since ancient times using a variety of technologies. The secondary solar-powered resources such as tidal wave and wind power, hydro power and biomass, are account for most of the readily available non-conventional type of energy source on earth. But only a small fraction of the available solar energy is used [3]-[4]. Solar powered electrical generation relies on photovoltaic system and heat engines. Solar energy's uses are limited by human creativity. To harvest the solar energy, the most common way is to use photovoltaic panels which will receive photon energy from sun and convert it into electrical energy. Solar technologies are broadly classified as either passive solar or active solar energy depending on the way the solar energy may detain, convert and distributed. Active solar techniques include the use of PV panels and solar thermal collectors to strap up solar energy. Passive solar techniques include orientation and selecting materials with favourable thermal mass or light dispersing properties and design spaces that naturally circulate air [5].Solar energy has a vast area of application such as electricity generation for distribution, heating ,water pumping, lightening building, crop drying etc.

III. DISTRIBUTION OF SOLAR RADIATION

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A Figure 1.1 shows the solar radiation receives by earth is about 174 peta watts (PW) of incoming solar radiation at the upper atmosphere orbit and Approximately 30% is reflected back to space and only 89 PW is absorbed by oceans and land masses. The spectrum of solar light at the Earth's surface is generally spread across the visible and near-infrared reason with a small part in the near-ultraviolet.

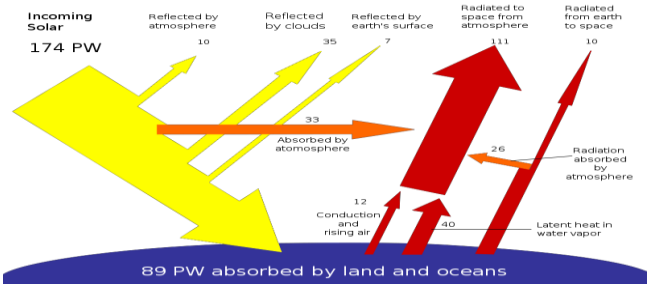

Fig.1.1Solar radiation distribution [18]

The total solar energy absorbed by Earth's atmosphere, oceans and land masses is approximately 3,850,000 EJ per year [4].

IV. PHOTOVOLTAIC CELL

In 1954 Bell labs Chopin, Fuller, Pearson fabricated PV cell with efficiency of 6%.In 1958 PV cell was used as a backup power source in satellite Vanguard-1. This extended the life of satellite for about 6 years [4].A photovoltaic cell is the basic device that converts solar radiation into electricity which is made of semiconductor materials, such as silicon. For solar cells, a thin semiconductor wafer is specially treated to form an electric field, positive on one side and negative on the other. When light energy strikes the solar cell, electrons are knocked loose from the atoms in the semiconductor material. If electrical conductors are attached to the positive and negative sides, forming an electrical circuit, the electrons can be captured in the form of an electric current - that is, electricity. This electricity can then be used to power a load [6]. A PV cell can either be circular or square in construction.

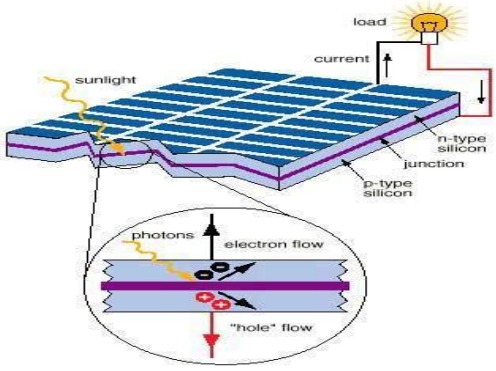

Fig.1.2 Basic Structure of PV Cell [6]

V. PHOTOVOLTAIC MODULE

Cells are arranged in a frame to form a module. The several PV cells are connected in series (for high voltage) and in parallel (for high current) to form a PV module for desired output. Separate diodes may be needed to avoid reverse currents, in case of partial or total shading, and at night. The p-n junctions of mono-crystalline silicon cells may have adequate reverse current characteristics and these are not necessary. Reverse currents waste power and can also lead to overheating of shaded cells. Solar cells become less efficient at higher temperatures and installers try to provide good ventilation behind solar panels [7].Each PV cell is rated for 0.5 –0.7 volt and a current of 30mA/cm^2. Based on the manufacturing process they are classified as:

Poly crystalline: efficiency of 12%.

Amorphous: efficiency of 6-8%

Life of crystalline cells is in the range of 25 years

Whereas for amorphous cells it is in the range of 5years

VI. PHOTOVOLTAIC ARRAY

The power that one module can produce is not sufficient to meet the requirements of home or business. Most PV arrays use an inverter to convert the DC power into alternating current that can power the motors, loads, lights etc. The modules in a PV array are usually first connected in series to obtain the desired voltages, the individual modules are then connected in parallel to allow the system to produce more current [8].

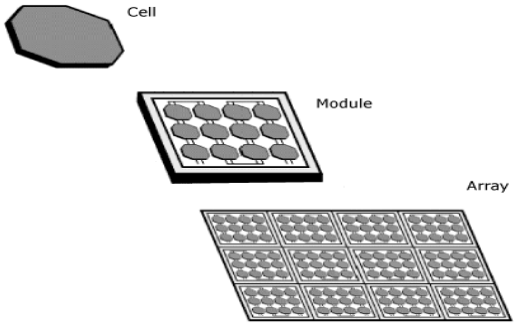

Fig.1.3 Photovoltaic systems [8]

VII. MATERIALS USED IN PV CELL

The materials used in PV cells are as follows:

Single-crystal silicon

Single-crystal silicon cells are the most common in the PV industry. The main technique for producing single-crystal silicon is the Czochralski (CZ) method. High-purity polycrystalline is melted in a quartz crucible. A single-crystal silicon seed is dipped into this molten mass of polycrystalline. As the seed is pulled slowly from the melt, a single-crystal ingot is formed. The ingots are then sawed into thin wafers about 200-400 micrometers thick (1 micrometer = 1/1,000,000 meter). The thin wafers are then polished, doped, coated, interconnected and assembled into modules and arrays [9].

Polycrystalline silicon

Consisting of small grains of single-crystal silicon, polycrystalline PV cells are less energy efficient than single-crystalline silicon PV cells. The grain boundaries in polycrystalline silicon hinder the flow of electrons and reduce the power output of the cell. A common approach to produce polycrystalline silicon PV cells is to slice thin wafers from blocks of cast polycrystalline silicon. Another more advanced approach is the “ribbon growth” method in which silicon is grown directly as thin ribbons or sheets with the approach thickness for making PV cells [9].

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Gallium Arsenide (GaAs)

A compound semiconductor made of two elements: Gallium (Ga) and Arsenic (As). GaAs has a crystal structure similar to that of silicon. An advantage of GaAs is that it has high level of light absorptivity. To absorb the same amount of sunlight, GaAs requires only a layer of few micrometers thick while crystalline silicon requires a wafer of about 200-300 micrometers thick. Also, GaAs has much higher energy conversion efficiency than crystal silicon, reaching about 25 to 30%.The only drawback of GaAs PV cells is the high cost of single crystal substrate that GaAs is grown on [9].

Cadmium Telluride (CdTe)

It is a polycrystalline compound made of cadmium and telluride with a high light absorbability capacity (i.e. a small thin layer of the compound can absorb 90% of solar irradiation).The main disadvantage of this compound is that the instability of PV cell or module performance. As it a toxic substance, the manufacturing process should be done by extra precaution [9].

Copper Indium Diselenide (CuInSe2)

It is a polycrystalline compound semiconductor made of copper, indium and selenium. It delivers high energy conversion efficiency without suffering from outdoor degradation problem. It is one of the most light-absorbent semiconductors. As it is a complex material and toxic in nature so the manufacturing process faces some problem [9].

VIII. CHARACTERISTICS OF PV CELL

An ideal is modelled by a current source in parallel with a diode. However no solar cell is ideal and thereby shunt and series resistances are added to the model as shown in the PV cell diagram above. R_S is the intrinsic series resistance whose value is very small. R_P is the equivalent shunt resistance which has a very high value [10].

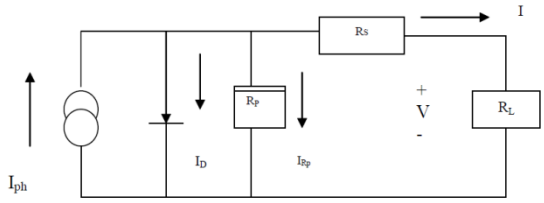

Fig.1.4 Equivalent circuit of a PV cell

Applying Kirchhoff's law to the node where I_{Ph}, diode, R_P and R_S meet, we get

$$I_{Ph} = I_D + I.R_P + I \quad \ldots\ldots\ldots\ldots\ldots (1.1)$$

We get the following equation for the photovoltaic Current:

$$I = I_{Ph} - I.R_P - I_D \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.2)$$

$$I = I_{Ph} - I_o [\exp (V+I.R_s)/V_T) - 1] - [V + I.R_s)/R_P] \ldots\ldots. (1.3)$$

Here, I_{Ph} is the insolation current, I is the Cell current, I_o is the Reverse saturation current, V is the Cell voltage, R_S is the Series resistance, R_P is the Parallel resistance, V_T is the Thermal voltage (K.T/q), K is the Boltzmann constant, T is the Temperature in Kelvin, q is the Charge of an electron The short circuit current (I_{SC}) equal to the cell current(I) depends on I_{ph}, the insolation current Mathematically we can write:

$$I_{SC} \propto I_{ph}$$

Open circuit voltage is the voltage at which the cell current is zero

➢ The expression for the open circuit voltage can be obtained by substituting I = 0 in equation 1.3 and after simplifying it we obtain the following expression

$$V_{OC} = V_T \text{ In } [(I_{ph} / I_O) - (V_{OC} / I_O.R_P) + 1]$$

IX. EFFICIENCY OF PV CELL

The efficiency of a PV cell is defined as the ratio of peak power to input solar power.

$$\eta = (V_{mp.} I_{mp}) / I \text{ (KW/m}^2\text{) A (m}^2\text{)} \ldots\ldots\ldots (1.4)$$

Where, V_{mp} is the voltage at peak power, I_{mp} is the current at peak power, I is the solar intensity per square metre, A is the area on which solar radiation fall. The efficiency will be maximum if we track the maximum power from the PV system at different environmental condition such as solar irradiance and temperature by using different methods for maximum power point tracking

X. PV ARRAY CHARACTERISTIC CURVES

The current to voltage characteristic of a solar array is Non-linear, which makes it difficult to determine the MPP the Fig 1.51 given below gives the V-I characteristic and P-V curve for fixed level of solar irradiation and temperature

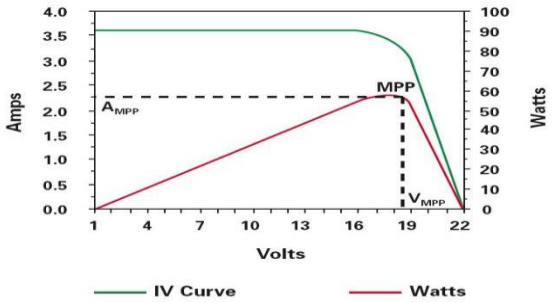

Fig. 1.5 I-V and P-V curve characteristics of solar cell [11]

The V-I and P-V curves for various irradiance beta fixed temperature (25^0C) are shown below in Fig (1.6) & (1.7)

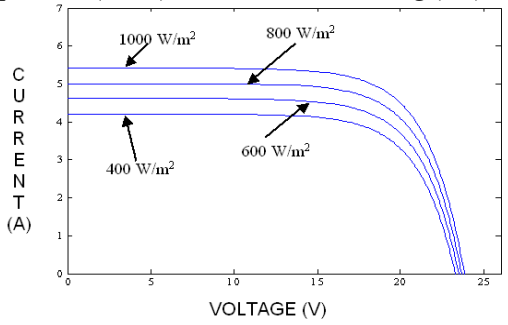

Fig. 1.6 I-V characteristic of a solar array for a fixed temperature but varying irradiance. [11]

The I-V characteristic curve tells that there are two regions, since the curve one is the current source region and another is the voltage Source region. In the voltage source region (in the right side of the curve), the internal impedance is low and in the current source region (in the left side of the curve), the impedance is high. Irradiance temperature plays an important role in predicting the I-V characteristic, and effects of both factors have to be considered while designing the P-V system. Whereas the irradiance affects the output, temperature mainly affects the terminal voltage.

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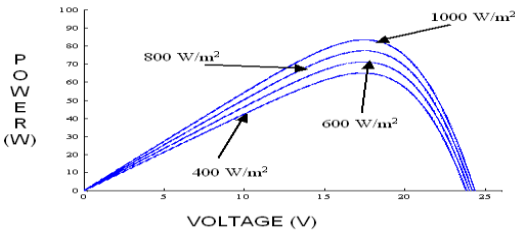

Fig. 1.7 P-V characteristic of a solar array for a fixed temperature but varying irradiance [11]

XI. QUALITY OF CELL

Now knowing all the four quantities, V_{OC}, I_{SC}, V_{mp} and I_{mp}, the quality of the cell called Fill Factor (*FF*) can be calculated as follows:

$$FF = (V_{mp}.I_{mp}) / V_{oc}.I_{sc}) \quad \ldots\ldots\ldots\ldots (1.5)$$

- Ideally, the fill factor should be 1 or 100%. However, the actual value of FF is about 0.8 or 80%.
- Typical commercial solar panels have a fill factor > 0.70, while grade B solar panels have a fill factor range from 0.4 to 0.7. A higher fill factor solar panel has less loss due to the series and parallel resistances within the cells themselves.
- The variation of Fill Factor with reverse saturation current Io is shown in Fig 1.8 & 1.9 Curves (a) & (b) are for Rs equal to 1.41 & 1.92Ω, respectively. Curve (c) shows the variation of fill factor, taking into account the operating current dependence of series resistance.

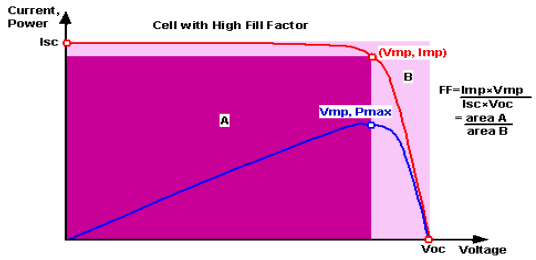

Fig.1.8. Ideally I-V Characteristics of PV cell for MPPT.

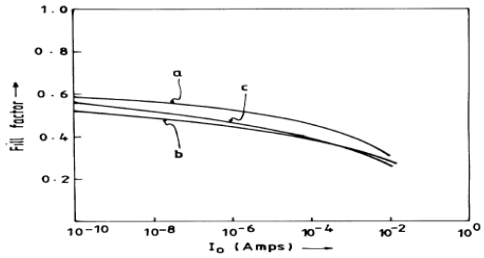

Fig.1.9 Variation of Fill Factor with Isolation [12]

XII. SERIES AND PARALLEL COMBINATION OF CELLS CELLS IN SERIES

When two identical cells are connected in series, the short circuit current of the system would remain same but the open circuit voltage would be twice as shown in the following Fig 1.10 & 1.11 and if the cells are identical

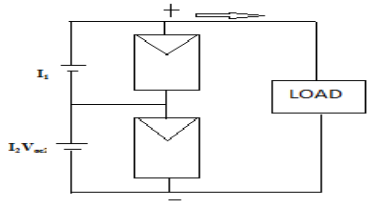

Fig. 1.10 Typical series combination of cells [12]

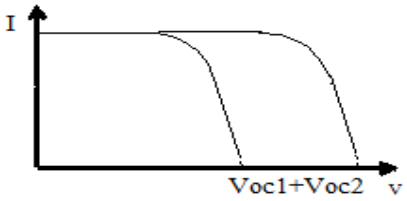

Fig. 1.11The typical I-V characteristics of series connected solar cells. [12].

$$I_1 = I_2 = I \quad \ldots (1.6)$$

$$V_{oc1} + V_{oc2} = 2V_{oc} \quad \ldots (1.7)$$

Unfortunately, it is very difficult to get two identical cells in reality. Hence, the need to analyses the situation little more closely. Let I_{sc1} be the short circuit current and V_{oc1} be the open circuit voltage of first cell and I_{sc2} and V_{oc2} be the short circuit current and open circuit voltage of the second cell and connect in series then V-I characteristics is as:

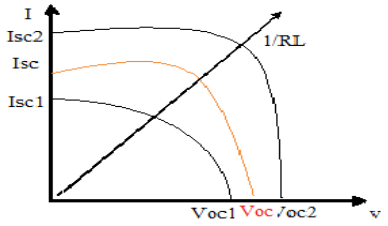

Fig 1.12 Typical I-V characteristics dissimilar series connected cells. [12]

From the above Fig1.12 the I-V characteristics when we connect two dissimilar cells in series, their open circuit voltages add up but the net short circuit current takes a value in between I_{sc1} and I_{sc2} shown by red colour curve.

To the left of the operating point, the weaker cell will behave like a sink [12].Hence, if a diode is connected in parallel, the weaker cell is bypassed, once the current exceeds the short circuit current of the weaker cell. The whole system would look as if a single cell is connected across the load. The diode is called a series protection diode.

XIII. CELLS IN PARALLEL

Figure 1.13 shows when two cells are connected in parallel. The open circuit voltage of the system would remain same as open circuit voltage of a single cell. But the short circuit current of the system would be twice as much as of a single cell.

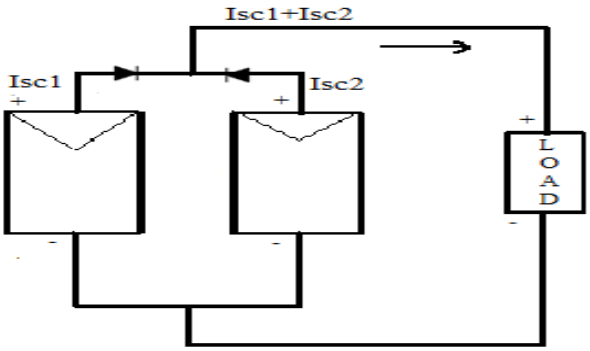

Fig. 1.13 Typically parallel connected cells. [12]

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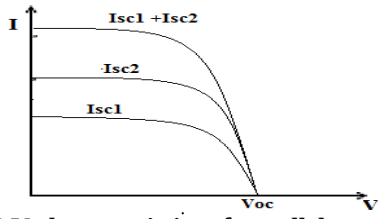

Fig. 1.14 I-V characteristics of parallel connected cells

From the Figs 1.13 & 1.14, if the cells are identical then

$$I_{sc1} + I_{sc2} = 2I_{sc} \quad \ldots (1.8)$$

$$V_{oc1} = V_{oc2} = V_{oc} \quad \ldots (1.9)$$

However, we rarely find two identical cells. Hence, let us see what happens if two dissimilar cells are connected in parallel. So I-V characteristics of cells as in Fig.1.15

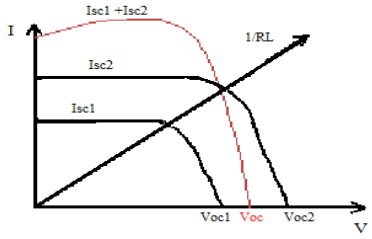

Fig. 1.15 The I-V characteristics of dissimilar parallel connected cells

From the Fig. 1.15 we can infer that, when two dissimilar solar cells are connected in parallel, the short circuit currents add up but the open circuit voltage lies between $V_{oc1}$and V_{oc2} represented by V_{oc} this voltage actually refers to a negative current of the weaker cell. This results in the reduction of net current out of the system. This situation can be avoided by adding a diode in series of each cell as shown earlier. Once the cell is operating to the right of the operating point, the weaker cell's diode gets reverse biased, cutting to from the system and hence follows the characteristic curve of the stronger cell.

XIV. MAXIMUM POWER POINT TRACKING

It is seen that the quality of cell can determined by open circuit voltage (V_{OC}) & short circuit current (I_{SC}) and voltage and current at maximum power point [13, 14, 15]. It is a two-step procedure to get maximum power point.

- First step is to plot 'voltage' *Vs* 'power' graph of the cell.
- The second step is to go to the V-I characteristics of the cell and locate the current corresponding to the voltage at maximum power point. This current is called the current at maximum power point.

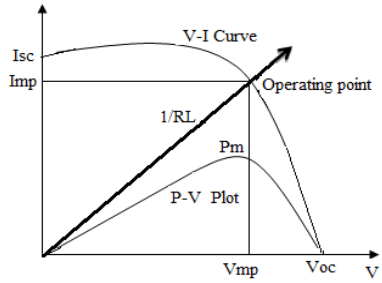

Fig. 3.1 V-I characteristics of cells for MPPT

- The point at which I_{mp} and V_{mp} meet is the point at which maximum power is available from the PV cell.
- If the 'load line' crosses this point precisely, then the maximum power can be transferred to this load.
- The value of this load resistant would be given by:

$$R_{mp} = V_{mp} / I_{mp} \quad \ldots (3.1)$$

To obtain the maximum power from a photovoltaic array, a maximum power point tracker (MPPT) is used. The Perturbation and observation is one of the most commonly used MPPT methods for its simplicity and ease of implementation. The P&O works well when the irradiance level change slowly but it presents drawbacks such as slow response speed, oscillation around the MPP in steady state, and even tracking in not working properly under rapidly changing atmospheric conditions. There are various methods for obtaining maximum power tracking for PV cell discussed as below [16]

XV. PERTURB AND OBSERVE METHOD

The P&O method is based on an adaptive algorithm which automatically adjusts the reference voltage step size to achieve dynamic response and search MPP under rapidly changing conditions by exploiting networks capabilities [17]. The perturb and observe (P&O) best operation conditions are investigated in order to identify the edge efficiency performances of this most popular maximum power point tracking (MPPT) technique for PV applications. P&O may guarantee top-level efficiency, provided that a proper predictive (by means of a parabolic interpolation of the last three operating points) and adaptive (based on the measure of the actual power) hill climbing strategy is adopted [18]. The characteristic slop during a perturbation cycle provide the best information concerning how much the operating point is far from the MPP in steady state, but when a variation occur suddenly , this information will alter the behaviour of the algorithm and cause it divergence by moving the operating point far from the MPP.

This problem can be solved if the algorithm acquires a skill which allows the detection of the working conditions variations and its extents also. It is well known that any atmospheric condition variation induce a proportional PV array output power variation. [19]

XVI. PARASITIC CAPACITANCE METHOD

The parasitic capacitance algorithm is similar to incremental conductance, except that the effect of the solar cells 'parasitic junction capacitance C_P, which models charge storage in the p–n junctions of the solar cells, is included. By adding this capacitance to the lighted diode equation, Equation, and representing the capacitance using

$$I_{(t)} = C\,(dV/dt) \quad \ldots (3.2)$$

$$I = I_L - I_O\,[\exp\,(V_P + I.R_S)/a) - 1] - C_P\,(dV_P/dt) \quad \ldots (3.3)$$

$$I = F\,(V_P) + C_P + C_P\,(dV/dt) \quad \ldots (3.4)$$

On the far right of Equation, the equation is rewritten to show the two components of I, a function of voltage F (V_P) and the current in the parasitic capacitance. Using this notation, the incremental conductance of the array g_p can be defined as dF (V_P)/dV_P and the instantaneous conductance of the array, g_L can be defined as F (V_P) =V_P. The MPP is located at the point where dP/dV_P= 0. Multiplying Equation by the array voltage V_P to obtain array power and differentiating the result, the equation for

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the array power at the MPP is obtained. Array voltage V_P to obtain array power and differentiating the result, the equation for the array power at the MPP is obtained by

$[dF (V_P)/dV_P] + C_P [(dV/V) + (d^2V/V)] + [F (V_P)/V_P] = 0$ … (3.5)

The three terms in Equation represent the instantaneous conductance, the incremental conductance, and the induced ripple from the parasitic capacitance. The first and second derivatives of the array voltage take into account the AC ripple components generated by the converter. The reader will note that if CP is equal to zero, this equation simplifies to that used for the incremental conductance algorithm. Since the parasitic capacitance is modelled as a capacitor connected in parallel with the individual solar cells, connecting the cells in parallel will increase the effective capacitance seen by the MPPT. [20] From this, the difference in MPPT efficiency between the parasitic capacitance and incremental conductance algorithms should be at a maximum in a high-power solar array with many parallel modules.

VOLTAGE BASED PEAK POWER TRACKING METHOD

The basis for the constant voltage (CV) algorithm is the observation from I–V curves that the ratio of the array‘s maximum power voltage V_{MPP}, to its open-circuit voltage, V_{OC}, is approximately constant. In other words $(V_{mpp}/V_{oc}) < 1$ the constant voltage algorithm can be implemented using the flowchart. The solar array is temporarily isolated from the MPPT, and a V_{OC} measurement is taken.

Next, the MPPT calculates the correct operating point using Equation and the present value of K, and adjusts the array‘s voltage until the calculated V_{MPP} is reached. This operation is repeated periodically to track the position of the MPP. Constant voltage control can be easily implemented with analogy hardware [21].However; its MPPT tracking efficiency is low relative to those of other algorithms. Reasons for this include the aforementioned error in the value of K, and the fact that measuring the V_{OC} requires a momentary interruption of P-V power. It is possible to dynamically adjust the value of K, but that requires a search algorithm and essentially ends up being the same as P&O.

INCREMENTAL CONDUCTANCE METHOD

The incremental conductance method consists in using the slope of the derivative of the current with respect to the voltage in order to reach the maximum power point. To obtain this point, dV/dI must be equal to –I/V as shown in Fig 3.3. [22, 23].For any solar panel, the output power is function of the temperature and the sunshine values of the site where the panel is placed. This power can decrease or increase as result of any temperature and/or shining variations In Solar panels, output power is not constant. To maximize this power and maintain it constant at high values, it is necessary to define the Maximum Power Point Tracking (MPPT) methods, and apply these methods to controlled dc-dc converters (choppers) [24].Now, see the incremental conductance & solar panel modulation Modelling of a solar panel In the obscurity, a semiconductor presents a high resistance. When it is strongly illuminated, its resistance decreases. If the energy of the photons that constitutes the luminous ray is sufficient, these photons will be able to excite electrons blocked in the valence layer to jump to the conduction layer. It is the phenomenon of photo conductibility. The expression of the diode current is described by the following equation:

$$I_P = I_{CC} - I_d = I_S [\exp (e . V_P / K.T) - 1] \quad \text{..... (3.6)}$$

Where, I_P and V_P are the current and voltage of PV cell, the saturation current (I_s), the short-circuit (I_{CC})and direct currents I_d , k is the Boltzmann constant (equal to 8, 62.10-5eV/°K),T is the absolute temperature in °C and e is the electron charge (1.602×10^{-19} C). This equation corresponds to a current generator, which models the sunshine, and a diode is connected in parallel, which represents the PN junction. The equivalent circuit of the ideal photovoltaic is given in Fig. 3.3 to draw the real model of photovoltaic cell shown in Fig. 3.3, it is necessary to take in account the losses due to the manufacture. Therefore, two resistances should be

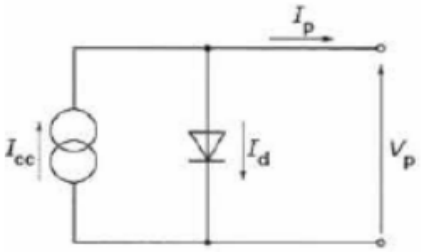

Fig. 3.3 Ideal photovoltaic cell [5]

added to the ideal model, one placed in series and the other in parallel. In fact, the resistance R_S represents the losses due to the contacts and the connections. The parallel resistance R_{sh} represents the leakage currents in the diode. The characteristic equation becomes then:

$$I_P = I_{CC} - I_d - [V/ R_{Sh}] \quad \text{..... (3.7)}$$

In fact, applying a variation on the voltage toward the biggest or the smallest value, its influence appears on the power value. If the power increases, one continues varying the voltage in the same direction, if not, one continues in the inverse direction. In addition, by using the power formula P=V.I, its derivative by

$$dP = V\, dI + I.dV \quad \text{.....(3.8)}$$

The duty cycle (Dn) of the used chopper (dc-dc converter) is calculated by the following expression,

$$Dn = Dn - 1 \pm \Delta D \quad \text{..... (3.9)}$$

Where ΔD is the duty cycle step

XVII. DC-DCCONVERTERS

DC-DC converters can be used as switching mode regulators to convert an unregulated dc voltage to a regulated dc output voltage. The regulation is normally achieved by PWM at a fixed frequency and the switching device is generally BJT, MOSFET or IGBT. The minimum oscillator frequency should be about 100 times longer than the transistor switching time to maximize efficiency. This limitation is due to the switching loss in the transistor. The transistor switching loss increases with the switching frequency and therefore efficiency decreases. The core loss of the inductors limits the high frequency operation. Control voltage V_C is obtained by comparing the output voltage with its desired value.

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Then the output voltage can be compared with its desired value to obtain the control voltage V_{cr}. The PWM control signal for the dc converter is generated by comparing V_{cr} with a saw tooth voltage V_r. [25]. There are four topologies for the switching regulators: Buck Converter, Boost Converter, Buck-Boost converter and Cuk converter

BUCK CONVERTER

This is a converter whose output voltage is smaller than the input voltage and output current is larger than the input current.[27] The conversion ratio is given by the following expression:

$$(V_o/V_{in}) = (I_{in} / I_o) = D \quad \text{..... (4.1)}$$

Where D is the duty cycle and given by

$$V_{in} = V_o / D \quad \text{..... (4.2)}$$

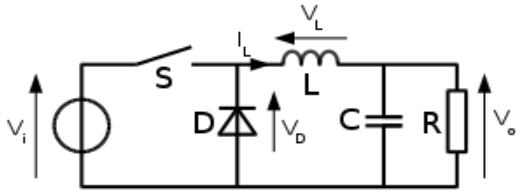

Fig. 4.1 Buck converter circuit diagram [27]

$$I_{in} = I_o D \quad \text{..... (4.3)}$$

The input resistance of the converter is given by

$$R_{in} = (V_{in} / I_{in}) = (V_o / D) / (I_o D)$$

$$R_{in} = (V_o / I_o) / D^2 = R_O / D^2 \quad \text{..... (4.4)}$$

Where R_o is the output resistance or load resistance of the converter

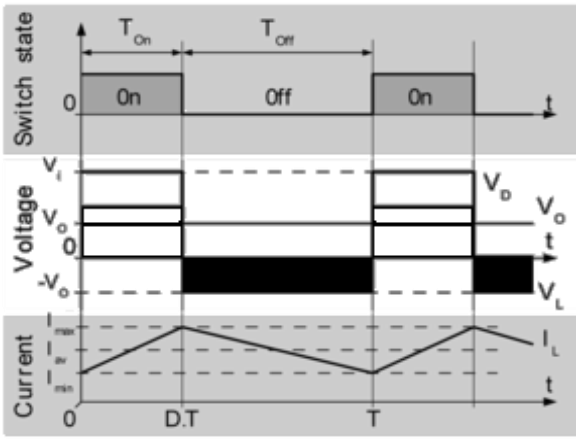

Fig. 4.2 Evolution of the voltages and currents with time in an ideal buck converter operating in continuous mode [28]

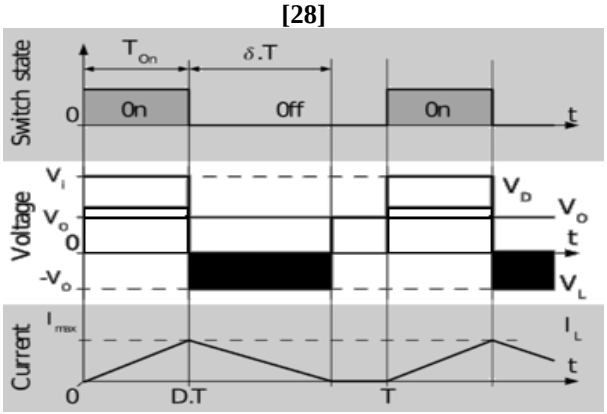

Fig. 4.3 Evolution of the voltages and currents with time in an ideal buck converter operating in discontinuous mode [28]

BOOST CONVERTER

This is a converter whose output voltage is greater than the input voltage and output current is smaller than the input current. The conversion ratio is given by the following expression:[29]

$$(V_o/V_{in}) = (I_{in} / I_o) = 1/ (1-D) \quad \text{..... (4.5)}$$

Where D is the duty cycle and given as

$$V_{in} = V_O (1-D) \quad \text{..... (4.6)}$$

$$I_{in} = I_O/ (1-D) \quad \text{..... (4.7)}$$

The input resistance of the converter is

$$\text{Rin} = V_{in}/I_{in} = [V_O (1-D)] / [I_O/ (1-D)] = [V_O/I_O] (1-D)^2 \quad \text{... (4.8)}$$

Here, R_{in} varies from Ro to 0 as D varies from 0 to 1 correspondingly.

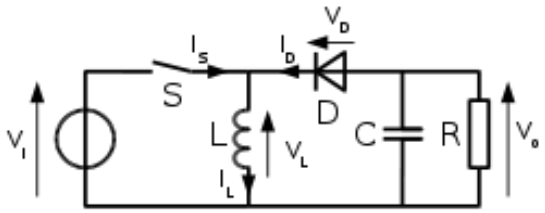

Fig. 4.4 Boost converter schematic diagram [29]

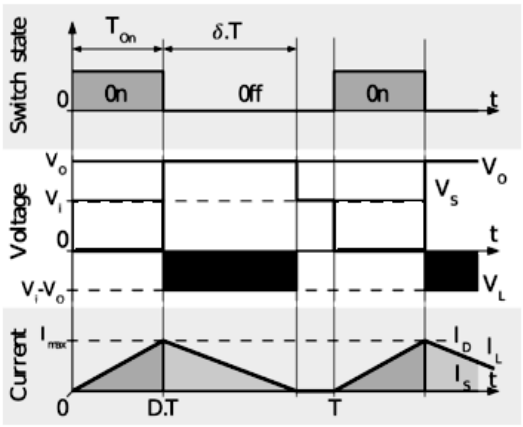

Fig. 4.5 Waveforms of current and voltage in a boost converter operating in continuous mode [29]

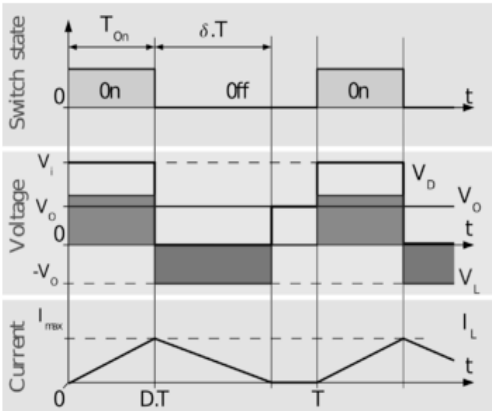

Fig. 4.6: Waveforms of current and voltage in a boost converter operating in discontinuous mode [29]

The Dynamic model of PV source, DC/DC boost power converter with resistance-inductance load are shown in Fig. 4.7.[29] Assuming that the PV source represents a single string topology, the output of the source is considered as a dc input voltage for the converter.

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As a result, the dynamic model of the system, which is adequate for control analysis [6, 10], is given using the average model of the converter as follows:

$$Li = (1-D)\,V + V_{pv} \quad \ldots (4.9)$$

$$CV = (1-D)\,I - I_L \quad \ldots (4.10)$$

$$L_L I_L = V - R_L I_L \quad \ldots (4.11)$$

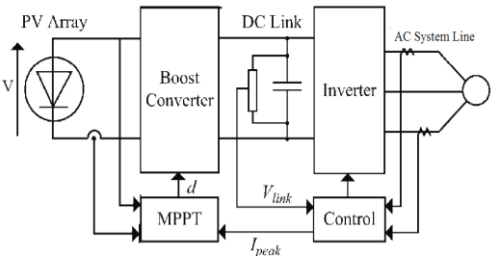

Fig. 4.7 Schematic diagram of the PV, DC/DC boost converter and resistance-inductance load [29]

Where I is the converter inductance current, V is the dc bus Voltage, I_L is the load inductance current, i.e. the state vector is described by $x = [I\ V\ I_L]^T$ and D is the duty ratio representing the switching cycle ratio in a period. Furthermore, is the converter inductance, while C is the capacitance, R_L s the load resistance, L_L is the load inductance and V_{PV} is the PV source dc voltage. It should be noticed that since D represents the duty ratio of the PWM circuit control, it is a continuous function that ranges in (0, 1).

BUCK- BOOST CONVERTER

The buck–boost converter is a type of DC-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude [30] to [36]. It is a switch mode power supply with a similar circuit topology to the boost converter and the buck converter. The output voltage is adjustable based on the duty cycle of the switching transistor. One possible drawback of this converter is that the switch does not have a terminal at ground this complicates the driving circuitry. Also, the polarity of the output voltage is opposite the input voltage. Neither drawback is of any consequence if the power supply is isolated from the load circuit (if, for example, the supply is a battery) as the supply and diode polarity can simply be reversed. The switch can be on either the ground side or the supply side.

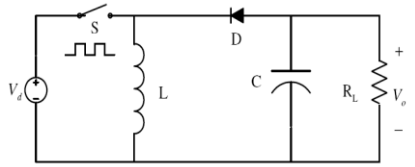

Fig 4.8 Schematic of a buck–boost converter [30]

The basic principle of the buck–boost converter is fairly simple in Fig.4.8.andThe conversion ratio given by

$$(V_o/V_{in}) = (I_{in}/I_o) = D/(1-D) \ldots\ldots\ldots\ldots\ldots (4.12)$$

Where, D is the duty cycle.

The input resistance of the converter

$$R_{in}=V_{in}/I_{in}= (V_o/I_o)\,((1-D)^2/D^2) = R_o\,((1-D)^2/D^2) \ldots (4.13)$$

Here, R_{in} varies from ∞to 0 as D varies from 0 to 1 correspondingly.

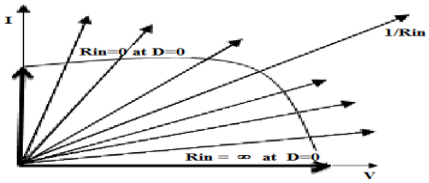

Fig. 4.9 The I-V characteristics of cells with buck boost converter

➢ While in the On-state, the input voltage source is directly connected to the inductor (L). This results in accumulating energy in L. In this stage, the capacitor supplies energy to the output load.

➢ While in the Off-state, the inductor is connected to the output load and capacitor, so energy is transferred from L to C and R.

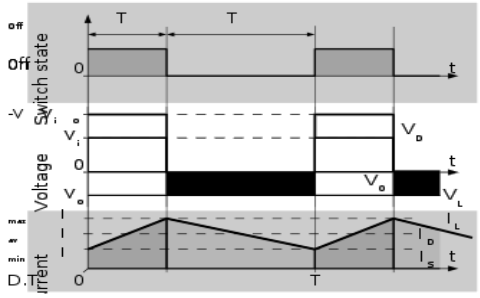

Fig. 4.10 Waveforms of current and voltage in a buck–boost converter operating in continuous mode [33]

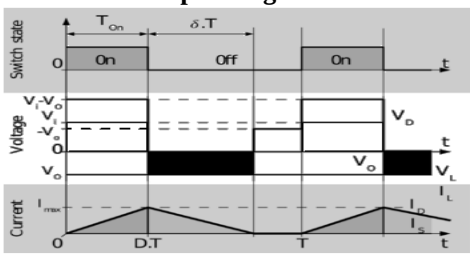

Fig. 4.11 Waveforms of current and voltage in a buck–boost converter operating in discontinuous mode [33]

CUCK CONVERTER

The Ćuk converter is a type of DC-DC converter where a negative polarity output may be desired with respect to the common terminals of the input voltage and the average output is either higher or lower than the dc input voltage [37]. The typical schematic circuit for the Cuk Converter is as shown in Fig. 4.12 the capacitor C1acts as a primary means to store and transfer the power from input to output. The voltagevc1 is always greater than either input or output voltage. The average output to input relations are similar to that of a buck-boost converter circuit. The output voltage is controlled by controlling the switch-duty cycle. The ratio of output voltage to input voltage is given by:

$$(V_o/V_{in}) = (I_{in}/I_o) = D/(1-D) \ldots\ldots\ldots\ldots (4.14)$$

Where, Vo and Vin are the output and input voltages, respectively. The term Io and I_{in} are the outputs and input currents, respectively.

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The term D is the duty ratio and defined as the ratio of the on time of the switch to the total switching period.

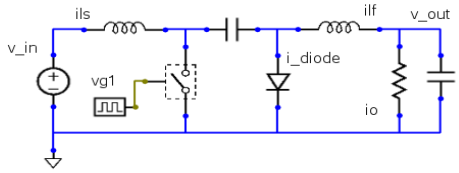

Fig. 4.12The Schematic circuit for the cuk converter [37]

CUK CONVERTER INTERFACES THE PV ARRAY WITH THE LOAD

The PV array feeds the DC–DC Cuk converter. The Cuk converter serves as an interface between the PV array and the load as shown in fig. 4.13. [38]A feedback controller with a proportional, integral and derivative (PID) controller for regulating the converter voltage is preferred. Besides reducing losses and stress due to the bandwidth-limited regulation of the duty cycle, the presence of PID controller improves the transient response on the input voltage of the Cuk converter and avoids oscillation and overshoot, making easier the functioning of MPPT methods.

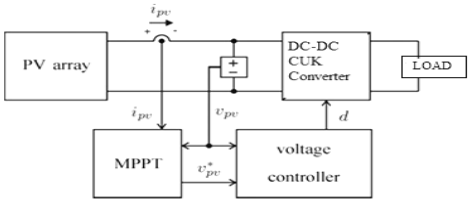

Fig. 4.13Input-regulated converter interfaces the PV array with the load [38]

VII. THE PROPOSED MULTILEVEL INVERTER TOPOLOGY FOR PV SYSTEMS

There are many ways to implement multilevel inverter topologies. Usually, to the modules which consist of a photovoltaic array categorized by different PV cell configurations and a DC to DC converter controlled by a MPPT algorithm and after that, the outputs of the DC/DC converters becomes nearly constant and then converted to AC by means of an inverter types topologies which are able to generate better output quality, while operating at lower switching frequency [39]. This implies lower switching dissipation and higher efficiency. Moreover, this topology utilizes switches with lower breakdown voltage; therefore, it can be used in higher power applications at lower cost. It is worth mentioning that although the number of switches in this approach is higher than other two level topologies, for a sufficient high number of levels, the output filter can be avoided which means less weight, cost and space. On the other hand, even with the same size of filter at the output, the switching frequency can be decreased which means higher efficiency. In general, a greater number of switches in multilevel converters can be justified since the semiconductor cost decreases at a much greater rate than the filter components cost. Therefore the total cost of multilevel converters to be comparable or even lower than that of two-level converters. Among various multilevel topologies, the most important ones are [40, 41]: Current multilevel (CML) inverter, Cascaded Multilevel Inverters (CMI), Diode-Clamped Multilevel Inverter (DCMI) [42] and Flying Capacitors Multilevel Inverters (FCMI) and

CURRENT MULTILEVEL (CML) INVERTER

The current-multilevel (CML) technique on PV systems shown in Fig. 5.1[43] in addition to the proposition of a novel CML single-phase inverter topology. CML converters have the advantage of reducing the current rating needs for the semiconductor devices, since the main current is shared by a number of paralleled cells.

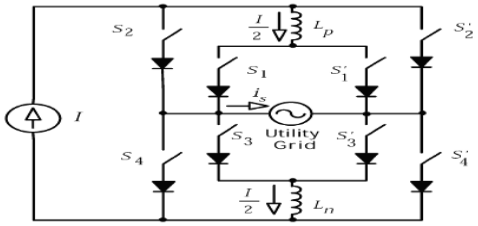

Fig 5.1 CML current–source inverter [43]

This benefit is useful for high power applications. The CML technique has been applied to dc-to-dc converters, rectifiers and current-source inverters [44]–[47]. A single-phase CML current- source inverter has been proposed some years ago, and is shown in Fig. 1 [44]. This topology employs two CML cells [43] and can synthesize an output current waveform with up to five levels employing line-frequency switching Fig.5.1(a) or up to three levels employing sinusoidal pulse width modulation (PWM) switching Fig.5.1(b)

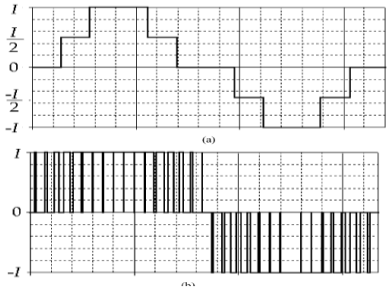

Fig 5.1 CML current-source inverter output current waveform employing :(a) line-frequency switching and (b) Sinusoidal PWM switching.

CASCADED MULTILEVEL INVERTERS (CMI)

The structure of single phase cascaded nine level inverter is shown in Fig 5.3(a) [48]-[54]. Each bridge is energized by separate DC sources which may be obtained from batteries, fuel cells, solar cells or ultra capacitors. Now by connecting the different full-bridge inverter in series such that the synthesize output voltage waveform is the resultant sum of the inverter ac output and the cascaded inverter output phase voltage is defined as n=2S+1, where 'S' is the number of PV

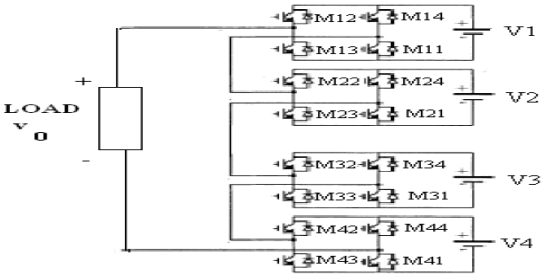

Fig 5.3(a) Structure of single phase cascaded nine level Multilevel Inverter [48]

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cell based separate dc source and the maximum output V_{max} of this cascaded multilevel inverter is V_{max} .An example of a 9-level cascaded H-bridge inverter with 9(SCDS) and 9 full bridge inverter is shown in Fig5.3.(b).The phase voltage $V_0 = V_{1+} V_{2+} V_{3+} V_4$ With enough levels and an appropriate switching algorithm, the multilevel inverter results in an output voltage that is near sinusoidal.

METHOD OF WORKING

The output voltage of nine- level cascaded multi-level inverter is shown in Fig 5.3(b). The steps to synthesize the nine level voltages are as follows

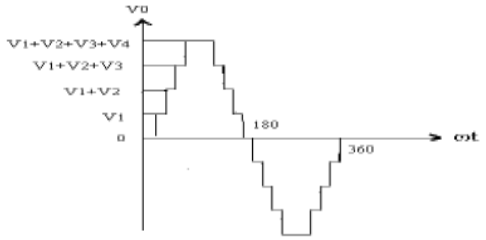

Fig 5.3(b) Output voltage of single phase cascaded nine-level inverter

1For an output voltage level V0 = V1, the switches M11, M12, M22, M32 and M42 are turned on.

2. For an output voltage level V0 = V1+V2, all the switches as mentioned in step 1 and M21 are turned on.

3. For an output voltage level V0 = V1+V2+V3, all the switches as mentioned in step 2 and M31 are made on.

4. For an output voltage level V0 = V1+V2+V3+V4, all the switches as mentioned in step 3 and M41are kept on

DIODE-CLAMPED MULTILEVEL INVERTER

The DCMLI stand-alone PV power system configuration with a six-level DCMLI system powered by five PV panels drives for a three-phase Load is shown in Fig5.4 but in actual implementation, several storage units (such as battery, ultra capacitor) would be in parallel with the PV panels in order to maintain energy storage capability for continuous operation of the PV system. An *m*-level diode-clamped multilevel inverter typically consists of (*m* – 1) power supplies on the dc bus and produces *m* levels of the phase voltage [55]. Five series PV modules connected on the dc bus with a three-phase six-level structure of the DCMLI is shown in Fig. 5.4(a) Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five PV panels into six levels. The voltage across each PV module is *Vdc*, and the voltage stress across each switching device is limited to *Vdc* through the clamping diodes. Each phase has

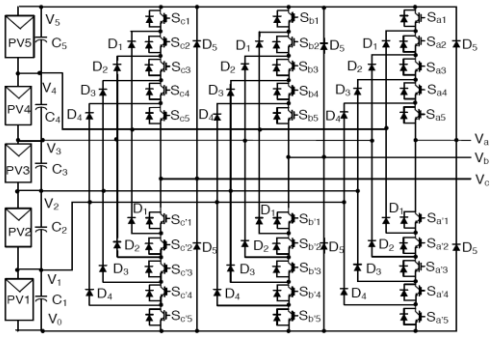

Fig 5.4(a) PV-connected to a three-phase six-level diode-clamped multilevel inverter topology [55]

Five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg *a* are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), and (S_{a5}, $S_{a'5}$). Fig 5.4(b) shows one of the three line-neutral voltage waveforms for a six-level DCMLI. The line voltage V_{ab} consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is an 11-level staircase waveform. This means that an *m*-level diode-clamped inverter has an *m* level output phase voltage and a (2*m*-1)-level output line voltage [56]. The simplest way to control a multilevel converter is to use a fundamental frequency switching control where the switching devices generate an *m*-level staircase waveform that tracks a sinusoidal waveform. In this control, each switching device only needs to switch one time per fundamental cycle, which results in low switching losses and low electromagnetic interference. Considering the symmetry of the waveform, there are only two switching angles (θ_1 and θ_2) that need to be determined in this control strategy, as shown in Fig 5.4(b).Since there is no neutral connection of the dc side of the six level DCMLI and in order to create balanced line voltage at the output of the inverter, phase voltage switching angles (θ_1 and θ_2) must be selected with a value less than 45 degrees as shown in Fig 5.4(b).

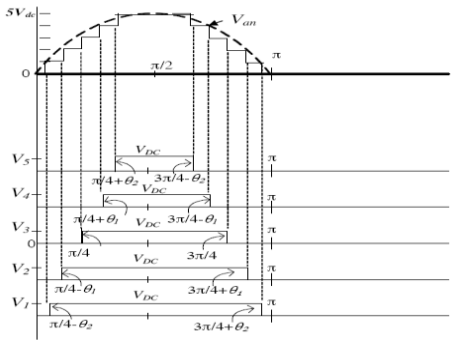

Fig. 5.4(b) Line-neutral voltage waveform for a six-level DCMLI. FLYING CAPACITOR MULTILEVEL INVERTER

This inverter uses capacitors to limit the voltage of the power devices. The configuration of the flying capacitor multilevel inverter is like a diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is V_{dc}.

5-level flying capacitor multilevel inverters

For a 5-level flying capacitor multilevel inverter:

n=5

Therefore: Number of switches=8

Number of capacitors= 10

Fig5.5 (a) shows a five level flying capacitor multilevel inverter. The switching states in this inverter are like in the diode clamped multilevel inverter. It means that for each output voltage level 4 switches should be on. The switching states for a 5-level flying capacitor clamped multilevel inverter [57]. The output voltage of flying capacitor multilevel inverter was shown in Fig 5.5(b) .The switching angles like the diode clamped multilevel inverter should be calculated in such a way that the THD of the output voltage becomes as low as possible. The method is the same as the diode clamped inverter.

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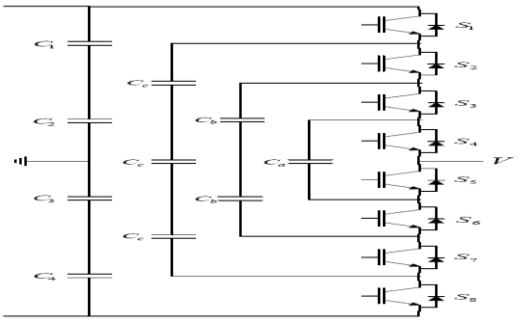

Fig 5.5(a) One phase of a 5-level Flying capacitor multilevel inverter

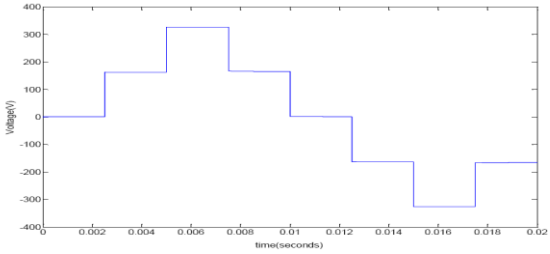

Fig 5.5(b) Output voltage of a 5-level multilevel inverter

IX. CONCLUSION

PV cells are approving environmentally friendly source of power that will continue to further photovoltaic research. Because presently PV systems are still highly inefficient and uncommon, they are not yet cost competitive with fossil fuel-based power generation, and it is used only where there is no nearby power supply source. Photovoltaic advancements in the fields of thin film and nano-crystalline materials will continue to flourish and soon increase PV efficiency to over 35%. As efficiency increases, PV technology will attract a greater number of people, resulting in reduced cost. Because the sun delivers ten thousand times more energy than people currently consume, the proposed multilevel inverter topology has been applied in a three-phase as well as single phase stand-alone photovoltaic system and presents several promising advantages. First, it can convert power for ac utility from relatively low dc voltage sources by itself. Second, it increases output voltage levels without any transformer so that it has higher efficiency and lower weight for the overall system. Third, in case of a multilevel inverter, it does not require an output filter because high-order harmonics are effectively filtered off, owing to the reactance of the load; therefore, it can produce a staircase voltage waveform with lower

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