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Performance Optimization of Logic Circuits based on Hybrid CMOS and CNFET Design

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Abstract*: *There is a pressing need to explore circuit design ideas in new emerging technologies in deep-submicron in order to exploit their full potential during the early stages of their development. Carbon nanotube (CNT) based technology has significant potential to replace silicon technology sometimes in the future. Single-walled carbon nanotubes are investigated for applications in logic and sensing circuits due to their superior transport properties. CMOS (complementary metal oxide semiconductor) technology is better in switching speed specially for NMOS. In this work we take advantage of the high mobility transport in p-type CNTFETs and combine them with high-performance conventional n-type MOSFETs, thereby achieving the best overall performance in a hybrid configuration. This paper presents a detailed simulation based assessment of circuit performance of this technology and compares it with 32nm CMOS and 32nm CNFET technologies. It is shown that the performance of the hybrid PCNFET-NMOS configuration is better than that of the pure CMOS in terms of noise margin (32.8% higher) and power consumption (60% lower) and therefore (2.5% lower)in PDP. The performance of PCNFET-NMOS is the same of pure CNFET for noise margin, 65% lower in power consumption and 2% lower in PDP. Also this integration of a carbon nanotube on an underlying CMOS circuit achieves a large saving in area that is amenable to future nanoscale device integration.

Index Terms*: *CNFET, CMOS technology, hybrid Design, noise margin, power delay product.

I. INTRODUCTION

The bulk CMOS technology is facing enormous challenges at channel lengths below 10nm, such as source to drain tunneling, device mismatch, random dopant fluctuations, mobility degradation, etc. While multiple gate transistors, strained silicon overcome some of the bulk CMOS problems, it is sensible to look for revolutionary new materials and devices to replace silicon. It is clear that future technology materials should exhibit higher mobility, better channel electrostatics, scalability and robustness against process variations. Carbon nanotube based technology is very promising because it has most of the desired features. It can also be easily clubbed with the bulk CMOS technology and utilizes the same infrastructure, thus shows potential to sustain the Moore's Law in the future. The Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising devices among emerging technologies. The CNFET offers many potential advantages with respect to silicon-based technology. Its electrical properties of greater mobility and high current carrying capability offer the potential for evolving to the next stage of devices and circuits. CNFET has been applied to a simple circuit design such as digital logic circuits, Full adder SRAM, etc [1]-[2]-[3]. Its operation principles and device structure are similar to CMOS, and therefore the mature design infrastructure of this latter technology can be utilized, together with its fabrication process. The carbon nanotube technology can be easily clubbed with the bulk CMOS technology on a single chip [4].

This paper investigates the performance of hybrid (Inverter, NAND, and NOR) which are obtained by the combination of CMOS and CNFET technologies. The paper also compared their performance with that of the conventional CMOS and Pure CNFET technology. In the circuit simulation, we use a 32nm CNFET HSPICE model that includes non-ideal effects for the CNFET [5]-[6] and the 32nm BSIM PTM (predictive technology model) for the Si MOSFET [7]. It is a first attempt to the best of our knowledge to explore the potential of this hybrid technology in designing high performance digital circuits. The paper begins with optimal device design followed by basic circuit configuration, device design specifications and optimal analysis and subsequently, the hybrid inverter design for optimum performance is presented. Finally the comparison of simulation results between logic circuits based on hybridization at 32nm technology node is presented before concluding this paper.

II. OPTIMAL DEVICE DESIGN

CNFETs as shown in Fig.1 are generally designed in terms of number of CNTs in the channel (N), center-center distance between two consecutive tubes known as Inter-CNT Pitch (S) and the Diameter of CNT (D_{CNT}). D_{CNT} can be calculated from Eq. (1) that the threshold voltage of the CNFET is an inverse function of the diameter of CNT [8] which is calculated by Eq. (2). Where n_1, n_2 the chiral number.

In this paper, for a CNFET with the chiral numbers (n1, n2) = (19, 0), D_{CNT} is 1.487nm and subsequently its threshold voltages is 0.293V.

$$D_{CNT} = \frac{a\times\sqrt{n_1^2+n_2^2+n_1n_2}}{\pi} \approx 0.0783 \times \sqrt{n_1^2+n_2^2+n_1n_2} \quad (1)$$

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT(nm)}} \quad (2)$$

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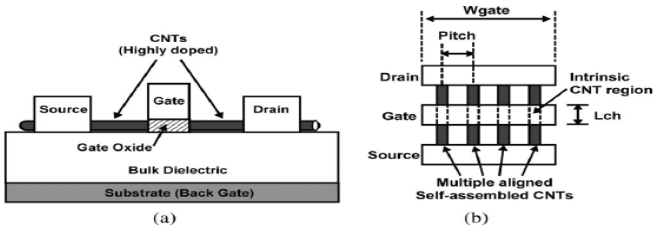

Fig. 1 CNFET structure (a) Cross-sectional view, (b) Top view

Variation of the drive current, i.e. Ids, with the increasing number of CNTs is illustrated in Fig. 2. This figure shows that the drive current increases as the number of CNTs increases. This is due to the fact that parallel CNTs increases the driving capability of the device but the individual nanotube I_{ON} current (operating current of the device) remains constant due to non-varying pitch (~20 uA, center to center distance of CNTs) [9].

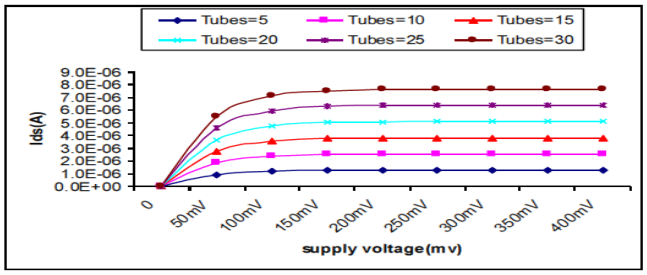

Fig. 2 I_{DS} vs. supply voltage for varying no. of CNTs

III. HYBRID DESIGN USING CNFET AND CMOS

The inverter is the fundamental logic gate for digital circuit design. Many of the basic principles employed in the design and analysis of an inverter can be also applied to complex logic gates/circuits such as NOR, NAND, XOR, and Full adder. We have designed an inverter circuit as shown in Fig. 3. This configuration is obtained by substituting PMOS with PCNFET and leaving the NMOS transistor unaltered as shown in Fig. 3(a). MOSFET–like CNFET has been chosen over SB-controlled FET as the reference for carrying out the analysis. The main advantage of MOSFET-like CNFET versus SB-CNFET is that its source-channel junction has no Schottky Barrier and hence, it has significantly higher ON current. As a result, MOSFET-like CNFETs are very suitable for ultra-high-performance digital applications [11]. Similar to previous treatment of another possible choice of hybridization is as shown in Fig. 3(b).

To compare the performance of CMOS, CNFET and hybrid configurations, the P transistor/N-transistor ratio of the MOSFET and CNFET inverters should be established. In general for Si CMOS, a PMOS/NMOS ratio of 2 or 3 is used because the NMOS mobility is about 2 or 3 times higher than that of the PMOS transistor. A 2:1 (PMOS:NMOS) ratio is used in this simulation because at this value, the voltage transfer characteristic (VTC) of the MOSFET inverter shows a more symmetrical shape for the 32nm technology as shown in Fig. 4. However for CNFETs, a PCNFET/NCNFET ratio of 1 is used because the NCNFET and PCNFET have the

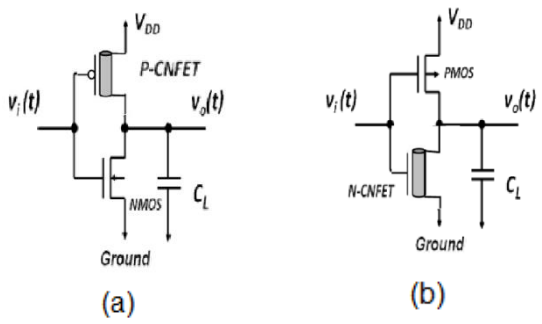

Fig. 3 Hybrid inverter configuration schematics (a) PCNFET-NMOS, (b) PMOS-NCNFET

same current driving capabilities with same transistor geometry. In CMOS design, the width of the MOSFET is adjusted to change the PMOS/NMOS ratio. However in a CNFET, the number of tubes is the design parameter (such as the W/L ratio in conventional design) for changing the current and resistance. Therefore, when the width of the CNFET is increased, the number of tubes is increased.

IV. PERFORMANCE COMPARISON OF HYBRID WITH PURE TECHNOLOGY DESIGN

In this section, we report our analysis and compare the proposed hybrid inverter with Bulk MOSFET and CNFET. The HSPICE circuit simulator has been used to simulate both CMOS and CNFET based circuits. The MOSFET circuits are simulated using a 32n technology.

A compact model of CNFETs presented in [12] and [13] has been used for CNFET based circuit simulation. The circuits are simulated at room temperature and the supply voltage is 0.9V for all of the circuits. For all circuits a 10fF load capacitor has been used.

The Voltage Transfer Characteristic (VTC) curves of the 32nm MOSFET, Hybrid1 (PCNFET –NMOS) and Hybrid2 (PMOS-NCNFET) are shown in Fig. 4, for minimum size MOSFET and CNFET inverters functionality. The curve is symmetric and the logic threshold voltage (Vinv) is in the center (Vinv=Vout =Vin=VDD/2). Even though the amount of current of a CNFET is smaller than for the minimum sized MOSFET at 32nm [14], the hybrid1 configuration has a steeper curve in the transition region. This is due to achievement of high speed by NMOS and offering better device characteristics (higher output current, higher on/off ratio, better sub-threshold swing, etc.) by p-type CNFETs rather than their n-type counterpart [15]. This contributes to a 32.8% improvement in noise margin. This improvement in performance is still preserved at a reduced power supply voltage.

The static power, the dynamic power dissipation and the power delay product (PDP) for the inverter gate of classical MOSFET, CNFET and two novel CNFET based hybridization are calculated and given in Table I.

As it can be seen from table I, Hybrid1 (PCNFET-NMOS) achieves 25% improvement in noise margin compared to pure 32nm MOSFET and Hybrid2 (PMOS-NCNFET) respectively.

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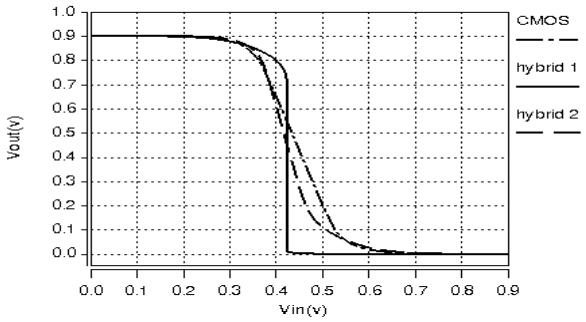

Fig. 4 Voltage Transfer Characteristic (VTC) for 32nm CMOS and hybrid1 (NMOS- PCNFET) and hybrid2 (PMOS-NCNFET)

In Hybrid1, we take advantage of the high mobility transport in p-type CNTFETs and combine them with high-performance and large savings in area conventional n-type MOSFETs, thereby achieving the best overall performance in a hybrid .

The Hybrid1 (PCNFET-NMOS) shows excellent reduction in dynamic power consumption. It consumes less power than the three other designs. It consumes 58.7%, 59.8% and 66%% power less than Hybrid2 (PMOS-NCNFET), MOSFET and CNFET kinds, respectively. Therefore its PDP is better than the three others. Simulation results have shown that Hybrid1 (PCNFET-NMOS) is much superior than conventional CMOS and Pure CNFET.

TABLE I
THE PERFORMANCE OF INVERTERS WITH DIFFERENT TECHNOLOGY

Optimum parameters of Inverter at CL=10fF	Pure CNFET with N=10, S=20nm, D_{CNT}=1.43nm	Hybrid1 PCNFET-NMOS With N=10, ,S=20nm	Hybrid2 PMOS-NCNFET With N=10 ,S=20nm	Pure 32nm Bulk MOSFET
Average power ($\times 10^{-7}$W)	68.8	23.4	56.7	58.3
Leakage Static power ($\times 10^{-9}$W)	0.38	8.6	0.39	8.6
PDP ($\times 10^{-16}$ J)	40.1	39.3	40.2	40.3

V. BASIC GATES SIMULATION RESULTS

In this section, we present performance evaluation for two-input NAND gate and two-input NOR gate which are designed using conventional CMOS, pure CNFET and hybrid configurations. Schematic of hybrid configurations for 2-input NAND gate and 2-input NOR gate are shown in Fig. 5 and Fig. 6.

The results of propagation delay, average leakage power and PDP for 32nm MOSFET, CNFET and hybrid gates are given in Table II. For logic gates specially for 2-input NAND gate, the average leakage power of the MOSFET is 1.6% and 4.6% times larger than the CNFET based gates and hybrid

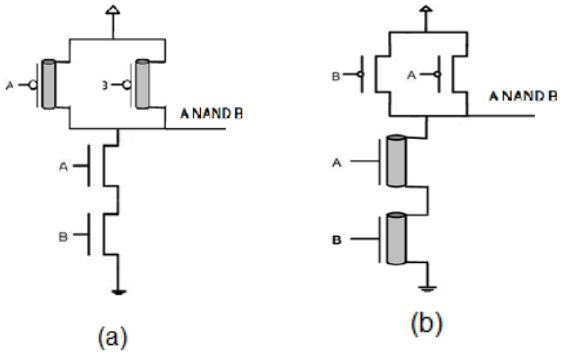

Fig. 5 Schematic configuration for 2 input NAND (a) Hybrid1, (b)Hybrid2

based gates respectively. Therefore, these results reflect improvement in the PDP for Hybrid1 configuration. For 2-input NOR gate the average leakage power of the MOSFET is 3.6% and 4.2% times larger than the CNFET based gates and hybrid based gates respectively.

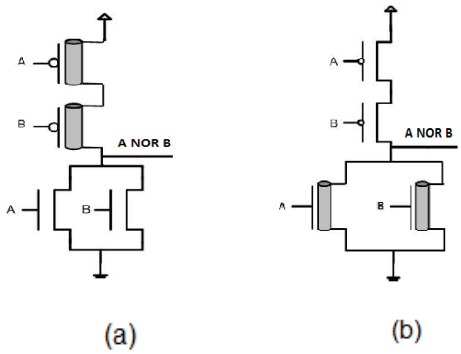

Fig. 6 Schematic view of 2-input NOR gate (a) Hybrid1, b) Hybrid2

TABLE II
THE DELAY, AVERAGE POWER AND PDP FOR 32NM MOSFET AND 32NM CNFET AND HYBRID BASED LOGIC GATES AT V_{DD}=0.9V

At Vdd=0.9 v	Two input NAND			Two input NOR		
	Delay ($\times 10^{-9}$ s)	Power ($\times 10^{-6}$ J/s)	PDP ($\times 10^{-15}$J)	Delay ($\times 10^{-9}$ s)	Power ($\times 10^{-6}$ J/s)	PDP ($\times 10^{-15}$J)
Pure 32nm MOSET	2.10	1.93	4.05	2.10	1.92	4.03
Pure CNFET N=10	2.13	1.90	4.05	2.18	1.85	4.03
Hybrid 1 PCNFET-NMOS	2.19	1.84	4.03	2.19	1.84	4.02
Hybrid 2 PMOS-NCNFET	2.08	1.95	4.06	2.10	1.93	4.05

In order to compare more precisely, these designs are also simulated in 0.8V, 0.7V and 0.6V supply voltages. The dynamic power consumption for NAND and NOR gates are shown in Table III and Table IV. These tables show that the average leakage power of the gate is reduced as the supply voltage decreases.

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The results show that the Hybrid1 (PCNFET-NMOS) basic gates have better performance in all situations.

TABLE III. THE DYNAMIC POWER CONSUMPTION FOR TWO-INPUT NAND GATE IN (µW)

Type of technology	Two-input NAND gate			
	Vdd=0.9	Vdd=0.8	Vdd=07	Vdd=0.6
Pure 32nm MOSFET	1.93	1.48	1.09	0.76
Pure CNFET N=10	1.90	1.45	1.10	0.78
Hybrid 1 PCNFET-NMOS	1.84	1.42	1.12	0.75
Hybrid 2 PMOS-NCNFET	1.95	1.52	1.14	0.80

TABLE IV. THE DYNAMIC POWER CONSUMPTION FOR TWO-INPUT NOR GATE IN (µW)

Type of technology	Two-input NOR gate			
	Vdd=0.9	Vdd=0.8	Vdd=0.7	Vdd=0.6
Pure 32nm MOSFET	1.92	1.49	1.09	0.77
Pure CNFET N=10	1.85	1.48	1.09	0.80
Hybrid 1 PCNFET-NMOS	1.84	1.46	1.07	0.76
Hybrid 2 PMOS-NCNFET	1.93	1.5	1.12	0.79

VI. CONCLUSION

In this paper, an attempt has been made to compare the performance of basic logic gates using CMOS and pure CNFET with hybrid configurations. It is observed that Hybrid1 design (PCNFET-NMOS) outperforms the pure CNFET design in switching speed but it is better than CMOS, pure CNFET and Hybrid2 configuration in dynamic power consumption. Using NMOS in Hybrid1 achieves area saving rather than PMOS in Hybrid 2. Therefore, the proposed Hybrid1 has the best overall performance in designing logic circuits. Our merging of these two technologies creates a new path for future integration of MOS technology with novel electronic devices.

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