

# Advance NOC Router with LOW Latency & Low Power Consumption by Wormhole Switching

Rajesh Nema, Teena Raikwar, Prerna Suryavanshi

**Abstract:** Network on Chip (NoC) is an approach to designing communication subsystem between intelligent property (IP) cores in a system on chip (SoC). Packet switched networks are being proposed as a global communication architecture for future system-on-chip (SoC) designs. In this project, we propose a design with low latency and low power consumption and implement a wormhole router supporting multicast for Network-on-chip. Wormhole routing is a network flow control mechanism which decomposes a packet into smaller flits and delivers the flits in a pipelined fashion. It has good performance and small buffering requirements. We proposed different power consumption with different frequency with different temperature.

**Keywords:** (NoC), (SoC), (IP).

## I. INTRODUCTION

NoCs are critical for supporting hundreds of functional units. Needs high performance, low energy consumption and reliable data transfer. Design of NoCs with performance, energy and fault tolerance is challenging with limited silicon budget in deep sub-micron technology. Prior work mostly considered performance and energy issues. Networks-on-Chips (NoC) is a bridge concept from Systems on-Chip (SoCs) into Multiprocessor System-on-Chip (MPSoC). A SoC design approach uses sometimes more than one processing element (PE) to implement an integrated circuit for a certain system application. The PEs send messages to other PEs for sharing computational processes to complete tasks. A sophisticated communication structure is needed for inter-processor data exchange. Rather than using a bus for single communication among PEs, or using point-to-point communication, a concept of shared segmented communication infrastructures is proposed to support application-scalability.

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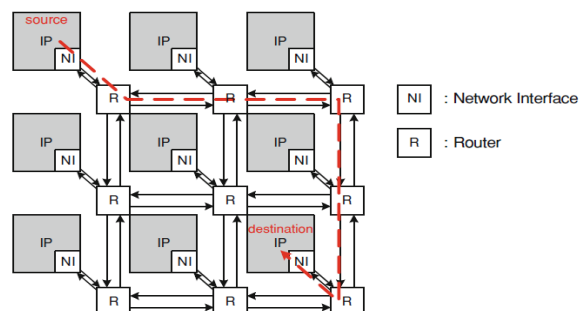
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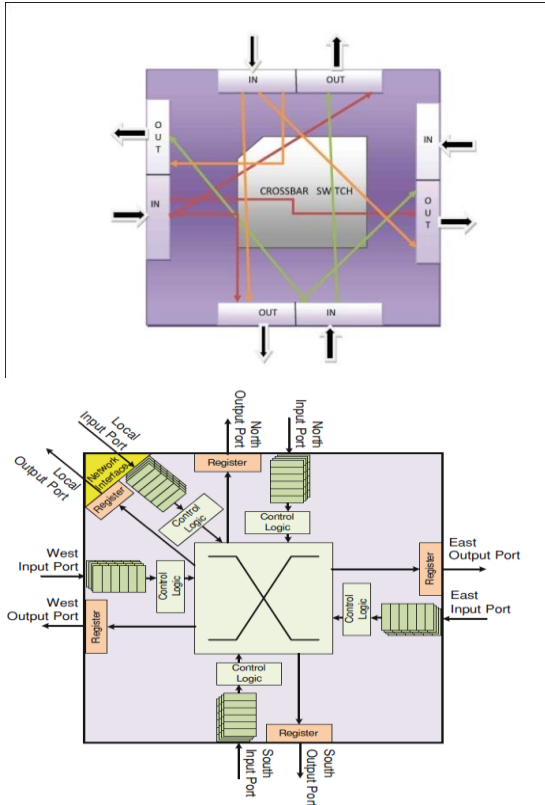


## II. RELATED WORK

- [1] This paper presents an advance router design using enhanced buffer. The design provide advantages of both buffer and buffer less network for that two cross bar switches are used but with the cost of increased latency and complexity.
- [2] Proposed NoC architecture a reconfigurable wormhole router architecture is used, which increase latency, low complexity and high buffer utilization, but less efficiency.
- [3] Proposed the router architecture optimization by utilizing the idle buffers instead of increasing the number and size of buffers for desired throughput.
- [4] Propose an SCAC-TMR(selected crosstalk avoidance code - triple modular redundancy) for message transmission and preserves state and controlling registers of routers . This scheme can avoid large crosstalk-induced delay in GHz circuits ,with high power consumption.
- [5] Proposes a feasible, efficient and fast programmable NoC router for these FPGA-based multi-cluster NoCs. With high power consumption.
- [6] Proposes a parameterized NoC router demonstrated 97%increase in throughput 76% decreases in latency which make router design expensive.
- [7] Proposes an average of 36% area savings (maximum of 47.5%) on XC2V P30 FPGA and significant performance gain (30% average compared to single-local port version) with a multi-local port router.

## III. PROPOSED METHODOLOGY

The router implemented using wormhole is Generic NoC router shown in Figure 1. It has five inputs and output ports, each of which is for local processing element (PE) and four directions: North, South, West, and East. Each router also has five components: Routing Computation (RC) Unit, Virtual Channel Allocator (VA), Switch Allocator (SA), flit Buffers (BUF), and Crossbar Switch.



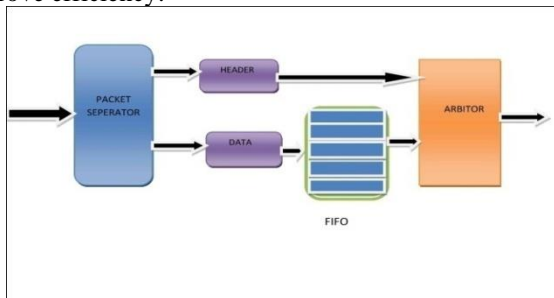
On-Clip Network Feature Characteristic:-

A. Two-Level Priority Message Delivery Service

The early prototype of our NoC has provided only a single priority with Best-Effort (BE) service. This Paper proposes a new prototype with additional Services for different level of priority. Therefore new modules i.e., a HP FIFO buffer.

1) **Low Priority Message Service (LP):** Our proposed LP service guarantees lossless packet completion and in-order message delivery, but provides no commitment to latency bound or data throughput because the messages are sent with a packet-based approach. The LP packets are routed using a minimal west-first adaptive routing algorithm, where the packets will not be routed away from their target nodes. The routing is made on flit-by flit basis, where different packets from different input ports share the link wires using wormhole switching, and can be interleaved in the FIFO. The incoming packet flits, which require the same link, are selected by an arbiter unit using fair round robin arbitration.

2) **Packet separator :** We propose a packet separator which carry data and header separately ,this reduce latency and improve efficiency.

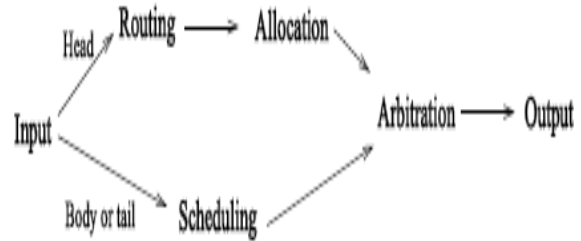


IV. GENERIC LOW LATENCY ROUTER COMPONENTS

For the proposed NoC architecture a reconfigurable wormhole router architecture is used, the details of which are presented below.

- ▶ Input Channel
- ▶ Switch Arbiter
- ▶ FSM
- ▶ Packet Formation

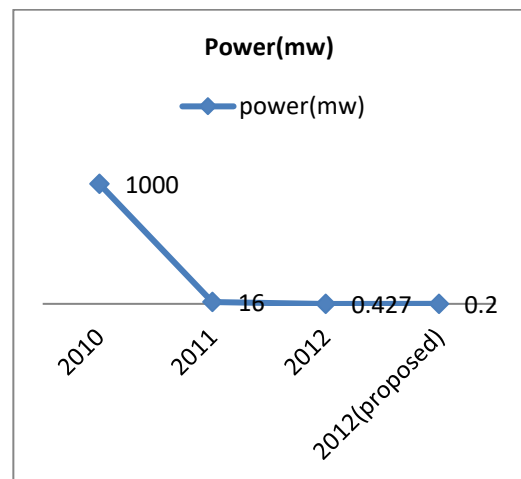
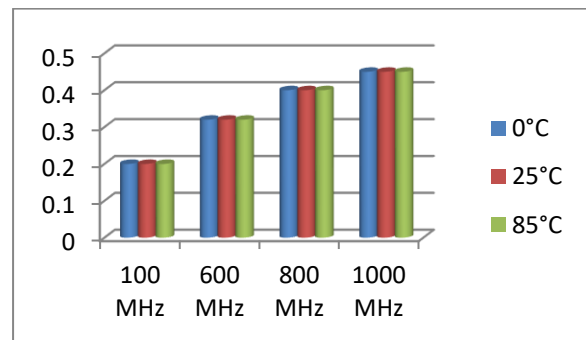
The router mainly comprises input channel, switch arbiters, Finite State Machines (FSM) and the packet formation. This comprises a head flit, a body flit and a tail flit. Here the packet length is unfixed and longer packets can be formed by adding more data flits between the head and the tail. The Output Channel (OC) field stores the output channel used by the packet. This is pre-computed using look ahead routing, one hop ahead. The width of the address field and output channel field both vary with network size. The router is fully pipelined allowing flits to pass through it in this manner.

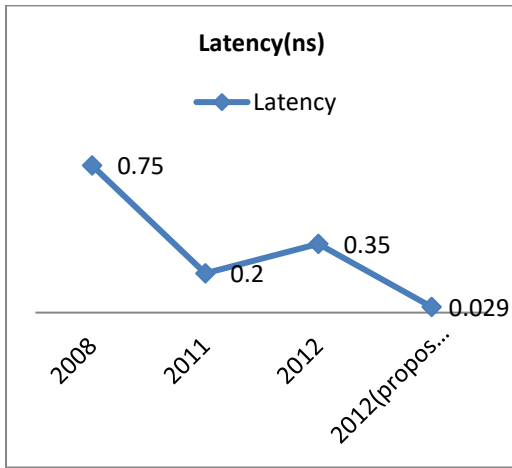


V. RESULT

The delay and average power of generic router is maximum, which are significantly reduced using virtual channel router and FIFO. In proposed design both the quantities .Reduced as we can also see in figure.

1] Optimization of Power with Frequency POWER (mw):-

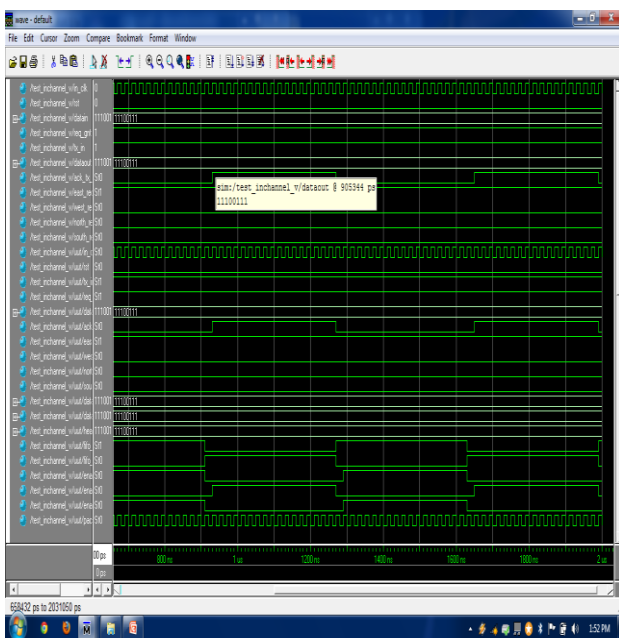




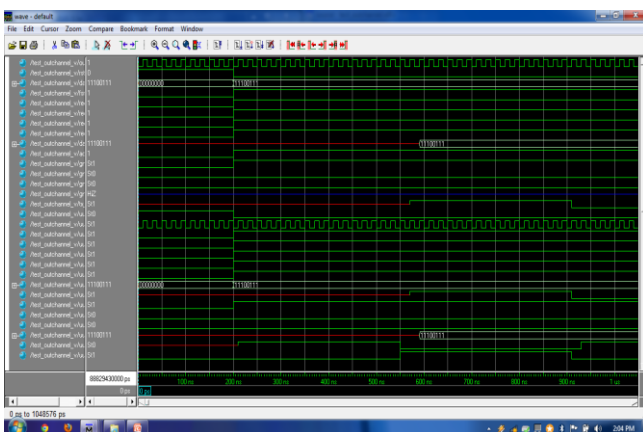
2] PROPOSED PARAMETER:-

Parameter	Value
Required Memory	124Mb
Power consumption	.2mw
Latency	.06ns
Frequency	257MHz

3] IN CHANNEL:-



4] OUT CHANNEL:-



VI. CONCLUSION

In proposed design the advantage of both FIFO and packet separator is achieved. Proposed a FIFO to enhance the overall performance. Average latency can be minimized about 0.06ns. Reduce power consumption about .2mw.

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